8255A

Programmable Peripheral Interface
Advanced MOS/LSI

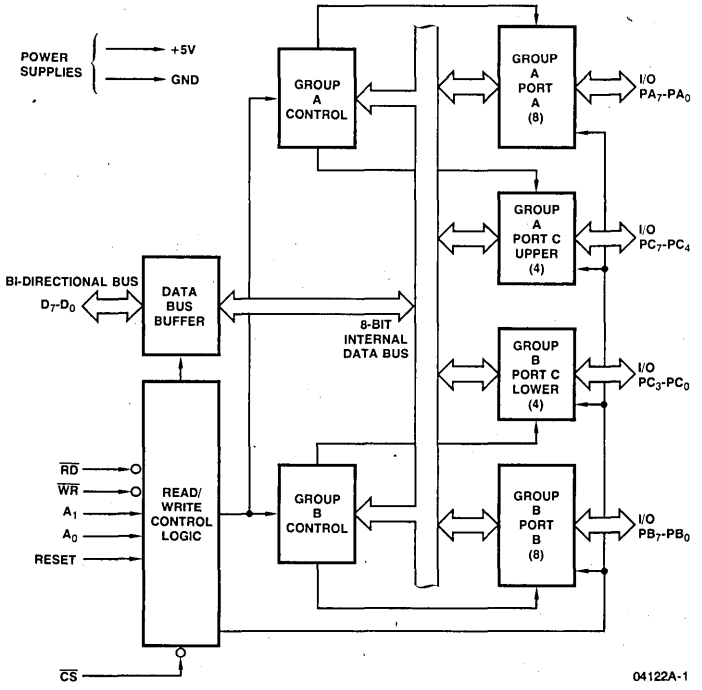
DISTINCTIVE CHARACTERISTICS

- Direct bit set/reset capability easing control application interface
- Reduces system package count
- Improved DC driving capability
- 24 programmable I/O pins
- Completely TTL compatible
- Fully compatible with 8080A and 8085A microprocessor families
- Improved timing characteristics
- Military version available

GENERAL DESCRIPTION

The 8255A is a general purpose programmable I/O device designed for use with 8080A and 8085A microprocessors. It has 24 I/O pins which may be individually programmed in two groups of twelve and used in three major modes of operation. In the first mode, each group of twelve I/O pins may be programmed in sets of 4 and 8 to be input or output. In Mode 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining four pins three are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a bidirectional bus mode which uses eight lines for a bidirectional bus, and five lines, borrowing one from the other group, for handshaking.

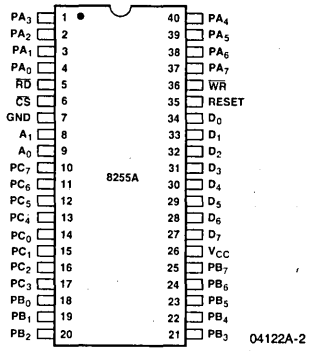
8255A BLOCK DIAGRAM



ORDERING INFORMATION

Package Type	Ambient Temperature Specification	Order Numbers	
		t_{WW} = 400ns	t_{WW} = 300ns
Molded DIP	$0°C \leq T_A \leq 70°C$	P8255A	P8255A-5
Hermetic DIP		D8255A	D8255A-5
Hermetic DIP	$-40°C \leq T_A \leq 85°C$	ID8255A	ID8255A-5
Hermetic DIP	$-55°C \leq T_A \leq 125°C$	MD8255AB	

CONNECTION DIAGRAM – Top View
D-40-1, P-40-1



04122A-2

PIN NAMES

D_7-D_0	Data Bus (Bi-Directional)
Reset	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0, A_1	Port Address
PA_7-PA_0	Port A (Bit)
PB_7-PB_0	Port B (Bit)
PC_7-PC_0	Port C (Bit)
V_{CC}	+5 Volts
GND	0 Volts

MAXIMUM RATINGS above which useful life may be impaired

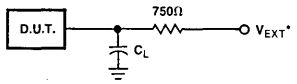
Storage Temperature	−65 to +150°C
V_{CC} with Respect to V_{SS}	−0.5 to +7.0V
All Signal Voltages with Respect to V_{SS}	−0.5 to +7.0V
Power Dissipation	1.0W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

CAPACITANCE T_A = 25°C; V_{CC} = GND = 0V

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	fc = 1MHz			10	pF
$C_{I/O}$	I/O Capacitance	Unmeasured pins returned to GND			20	pF

TEST LOAD CIRCUIT (FOR DATA BUS)



*V_{EXT} is set at various voltages during testing to guarantee the specification.

OPERATING RANGE

Part Number	Ambient Temperature	V_{CC}	V_{SS}
D8255A, P8255A D8255A-5, P8255A-5	0°C ≤ T_A ≤ 70°C	5V ±5%	0V
ID8255A ID8255A-5	−40°C ≤ T_A ≤ 85°C	5V ±10%	0V
MD8255AB	−55°C ≤ T_A ≤ 125°C	5V ±10%	0V

DC CHARACTERISTICS over operating range

Parameters	Description	Test Conditions	Min	Max	Units
V_{IL}	Input Low Voltage		−0.5	0.8	Volts
V_{IH}	Input High Voltage		2.0	V_{CC}	Volts
V_{OL}(DB)	Output Low Voltage (Data Bus)	I_{OL} = 2.5mA		0.45	Volts
V_{OL}(PER)	Output Low Voltage (Peripheral Port)	I_{OL} = 1.7mA		0.45	Volts
V_{OH}(DB)	Output High Voltage (Data Bus)	I_{OH} = −400μA	2.4		Volts
V_{OH}(PER)	Output High Voltage (Peripheral Port)	I_{OH} = −200μA	2.4		Volts
I_{DAR} (Note 1)	Darlington Drive Current	R_{EXT} = 750Ω; V_{EXT} = 1.5V	−1.0	−4.0	mA
I_{CC}	Power Supply Current			120	mA
I_{IL}	Input Load Current	V_{IN} = V_{CC} to 0V		±10	μA
I_{OFL}	Output Float Leakage	V_{OUT} = V_{CC} to 0V		±10	μA

Note 1: Available on any 8 pins from Port B and C.

AC CHARACTERISTICS Over Operating Range

BUS PARAMETERS:

Read:

Parameter	Description	8255A ID8255A Min.	8255A ID8255A Max.	8255A-5 ID8255A-5 Min.	8255A-5 ID8255A-5 Max.	MD8255AB Min.	MD8255AB Max.	Unit
t_{AR}	Address Stable Before READ	0		0		0		ns
t_{RA}	Address Stable After READ	0		0		0		ns
t_{RR}	READ Pulse Width	300		300		300		ns
t_{RD}	Data Valid From READ (Note 1)		250		200		250	ns
t_{DF}	Data Float After READ	10	150	10	100	10	150	ns
t_{RV}	Time Between READs and/or WRITEs	850		850		850		ns

Write:

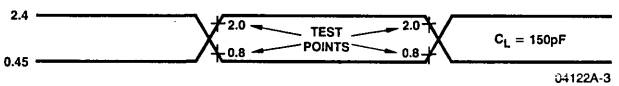
Parameter	Description	8255A ID8255A Min.	8255A ID8255A Max.	8255A-5 ID8255A-5 Min.	8255A-5 ID8255A-5 Max.	MD8255AB Min.	MD8255AB Max.	Unit
t_{AW}	Address Stable Before WRITE	0		0		0		ns
t_{WA}	Address Stable After WRITE	20		20		20		ns
t_{WW}	WRITE Pulse Width	400		300		400		ns
t_{DW}	Data Valid to WRITE (T.E.)	100		100		100		ns
t_{WD}	Data Valid After WRITE	30		30		30		ns

Other Timings:

Parameter	Description	8255A ID8255A Min.	8255A ID8255A Max.	8255A-5 ID8255A-5 Min.	8255A-5 ID8255A-5 Max.	MD8255AB Min.	MD8255AB Max.	Unit
t_{WB}	WR = 1 to Output (Note 1)		350		350		350	ns
t_{IR}	Peripheral Data Before RD	0		0		0		ns
t_{HR}	Peripheral Data After RD	0		0		0		ns
t_{AK}	ACK Pulse Width	300		300		300		ns
t_{ST}	STB Pulse Width	500		500		500		ns
t_{PS}	Per. Data Before T.E. of STB	0		0		0		ns
t_{PH}	Per. Data After T.E. of STB	180		180		180		ns
t_{AD}	ACK = 0 to Output (Note 1)		300		300		300	ns
t_{KD}	ACK = 1 to Output Float	20	250	20	250	20	250	ns
t_{WOB}	WR = 1 to OBF = 0 (Note 1)		650		650		650	ns
t_{AOB}	ACK = 0 to OBF = 1 (Note 1)		350		350		350	ns
t_{SIB}	STB = 0 to IBF = 1 (Note 1)		300		300		300	ns
t_{RIB}	RD = 1 to IBF = 0 (Note 1)		300		300		300	ns
t_{RIT}	RD = 0 to INTR = 0 (Note 1)		400		400		400	ns
t_{SIT}	STB = 1 to INTR = 1 (Note 1)		300		300		300	ns
t_{AIT}	ACK = 1 to INTR = 1 (Note 1)		350		350		350	ns
t_{WIT}	WR = 1 to INTR = 0 (Note 1, 3)		450		450		450	ns

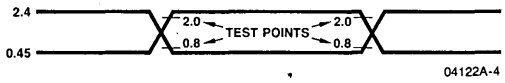
Notes: 1. Test Conditions: 8255A/ID8255A/MD8255AB: C_L = 100pF; 8255A-5: C_L = 150pF.
2. Period of Reset pulse must be at least 50μs during or after power on. Subsequent Reset pulse can be 500ns min.
3. INTR ↑ may occur as early as WR ↓.

AC TESTING INPUT, OUTPUT WAVEFORM

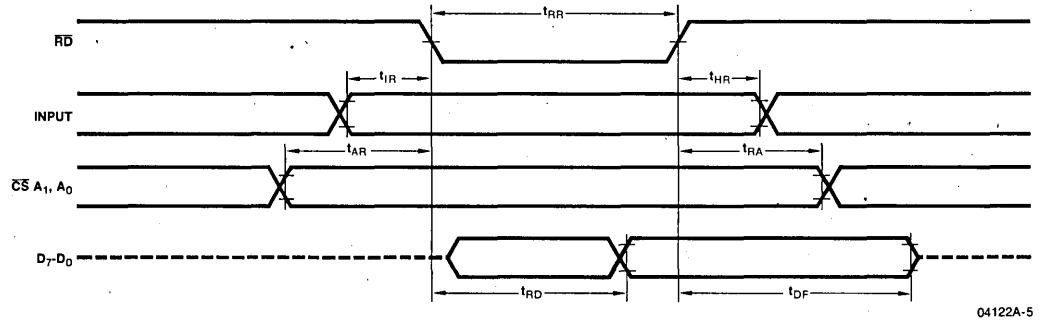


AC testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0."
Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0."

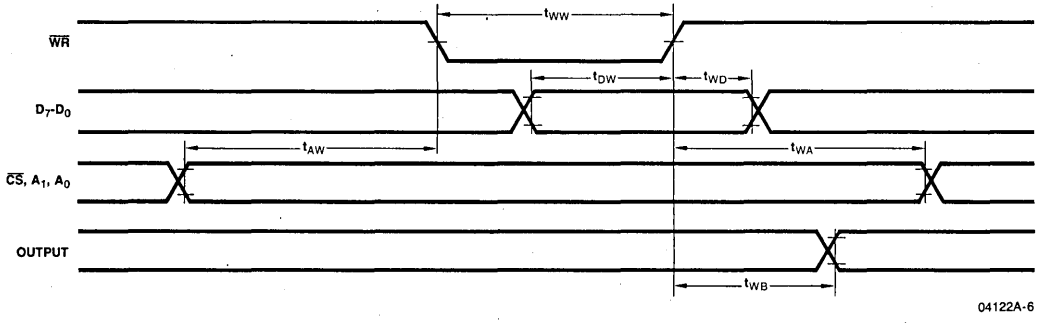
WAVEFORMS



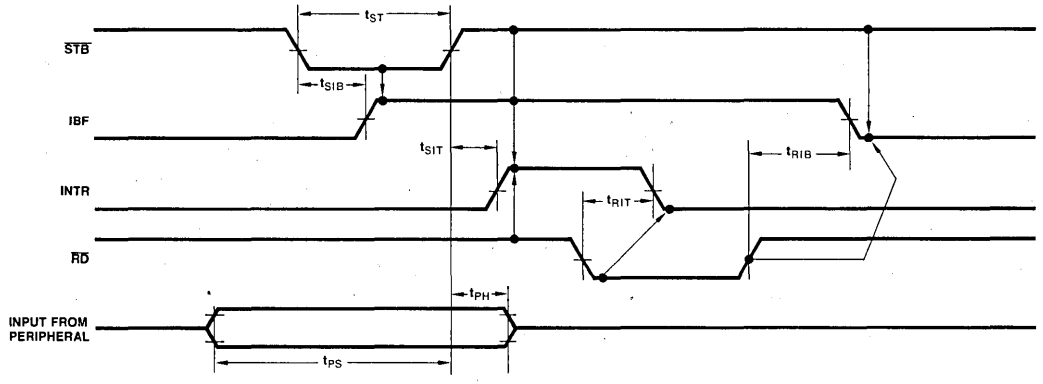
Input Waveforms For A.C. Tests



Mode 0 (Basic Input)

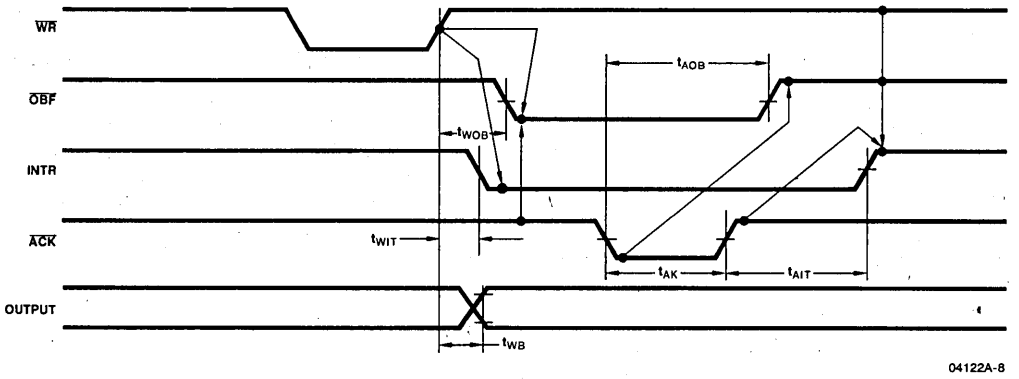


Mode 0 (Basic Output)

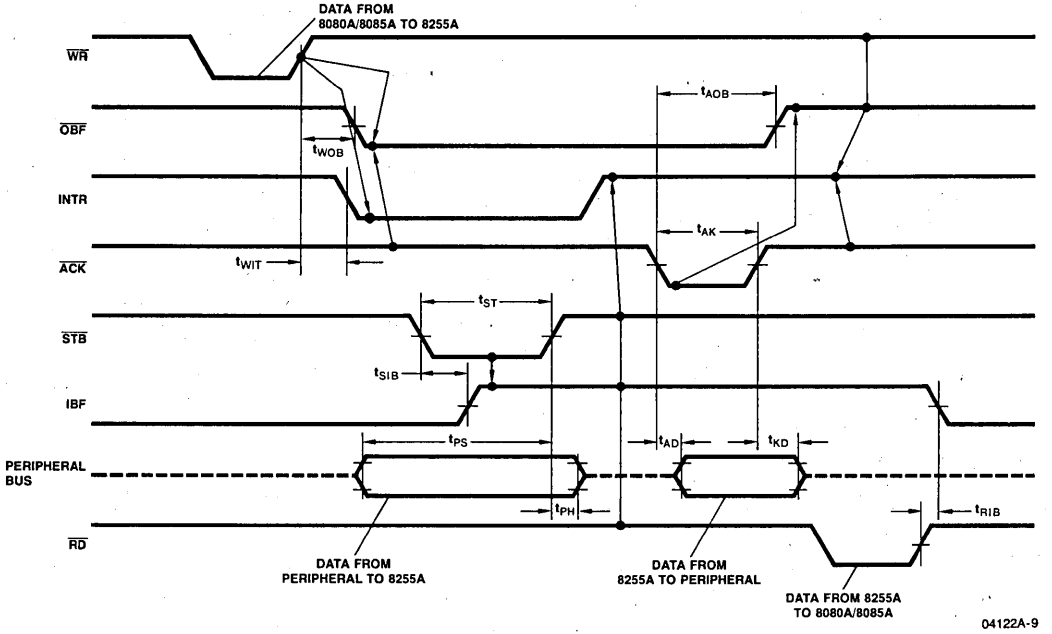


Mode 1 (Strobed Input)

WAVEFORMS (Cont.)



Mode 1 (Strobed Output)



Note: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF • $\overline{MASK}$ • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • $\overline{MASK}$ • $\overline{ACK}$ • $\overline{WR}$)

Mode 2 (Bi-directional)