Features

- **Pin Compatible with NMOS 8255A**
- **24 Programmable I/O Pins**
- **Fully TTL Compatible**
- **High Speed, No "Wait State" Operation with 5MHz 80C86 and 8MHz 80C88**
- **Direct Bit Set/Reset Capability**
- **Enhanced Control Word Read Capability**
- **L7 Process**
- **2.5mA Drive Capability on All I/O Ports**
- **Low Standby Power (ICCSB) 10μA**

Description

The WS82C55A is a high performance CMOS version of the industry standard 8255A and is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). It is a general purpose programmable I/O device which may be used with many different microprocessors. There are 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The high performance and industry standard configuration of the WS82C55A make it compatible with the 80C86, and other microprocessors.

Static CMOS circuit design insures low operating power. TTL compatibility over the full military temperature range and bus hold circuitry eliminate the need for pull-up resistors. The advanced SAJI process results in performance equal to or greater than existing functionally equivalent products at a fraction of the power.

Ordering Information

| PART NUMBERS	SPEED	PART NUMBERS	SPEED	TEMPERATURE RANGE	PKG.
WS82C55A-5P	5MHz	WS82C55AP	8MHz	0° C to 70° C	40DIP
WS82C55A-5C	5MHz	WS82C55AC	8MHz	0° C to 70° C	44 PLCC
WS82C55A-5Q	5MHz	WS82C55AQ	8MHz	0° C to 70° C	44 QFP

Pinouts
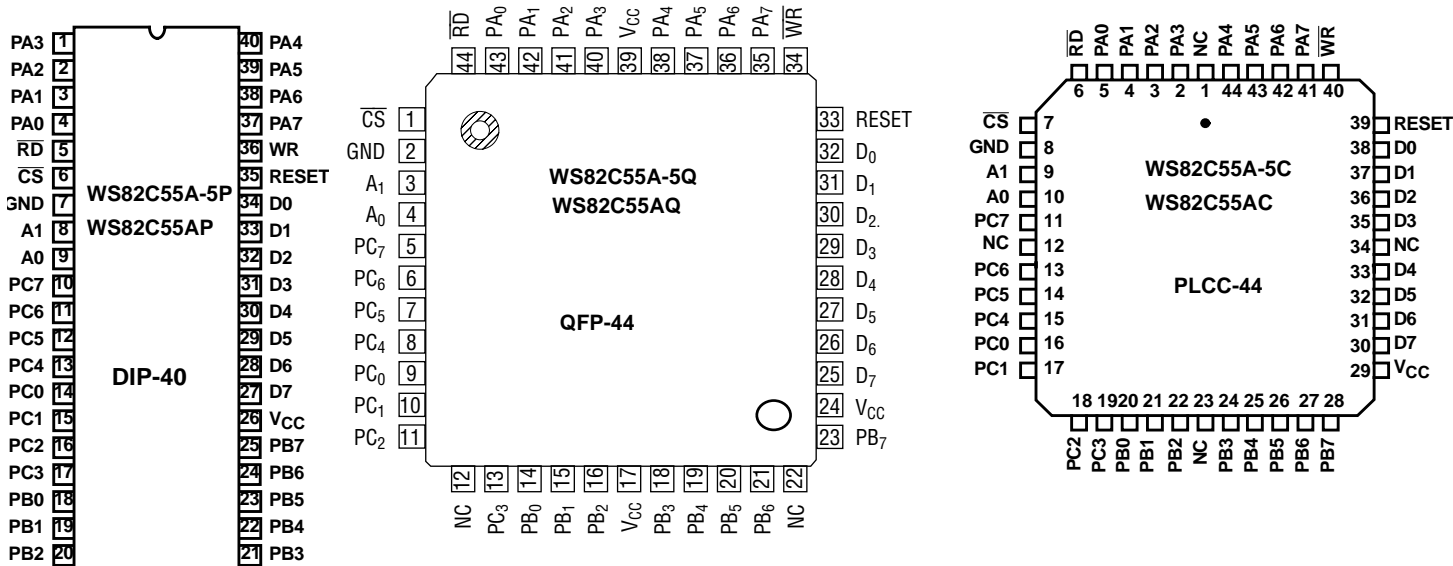
CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

Pin Description (For DIP-40)

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	26		V_{CC}: The +5V power supply pin. A 0.1μF capacitor between pins 26 and 7 is recommended for decoupling.
GND	7		GROUND
D0-D7	27-34	I/O	DATA BUS: The Data Bus lines are bidirectional three-state pins connected to the system data bus.
RESET	35	I	RESET: A high on this input clears the control register and all ports (A, B, C) are set to the input mode with the "Bus Hold" circuitry turned on.
$\overline{CS}$	6	I	CHIP SELECT: Chip select is an active low input used to enable the 82C55A onto the Data Bus for CPU communications.
$\overline{RD}$	5	I	READ: Read is an active low input control signal used by the CPU to read status information or data via the data bus.
$\overline{WR}$	36	I	WRITE: Write is an active low input control signal used by the CPU to load control words and data into the 82C55A.
A0-A1	8, 9	I	ADDRESS: These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word register. A0 and A1 are normally connected to the least significant bits of the Address Bus A0, A1.
PA0-PA7	1-4, 37-40	I/O	PORT A: 8-bit input and output port. Both bus hold high and bus hold low circuitry are present on this port.
PB0-PB7	18-25	I/O	PORT B: 8-bit input and output port. Bus hold high circuitry is present on this port.
PC0-PC7	10-17	I/O	PORT C: 8-bit input and output port. Bus hold circuitry is present on this port.

Functional Diagram
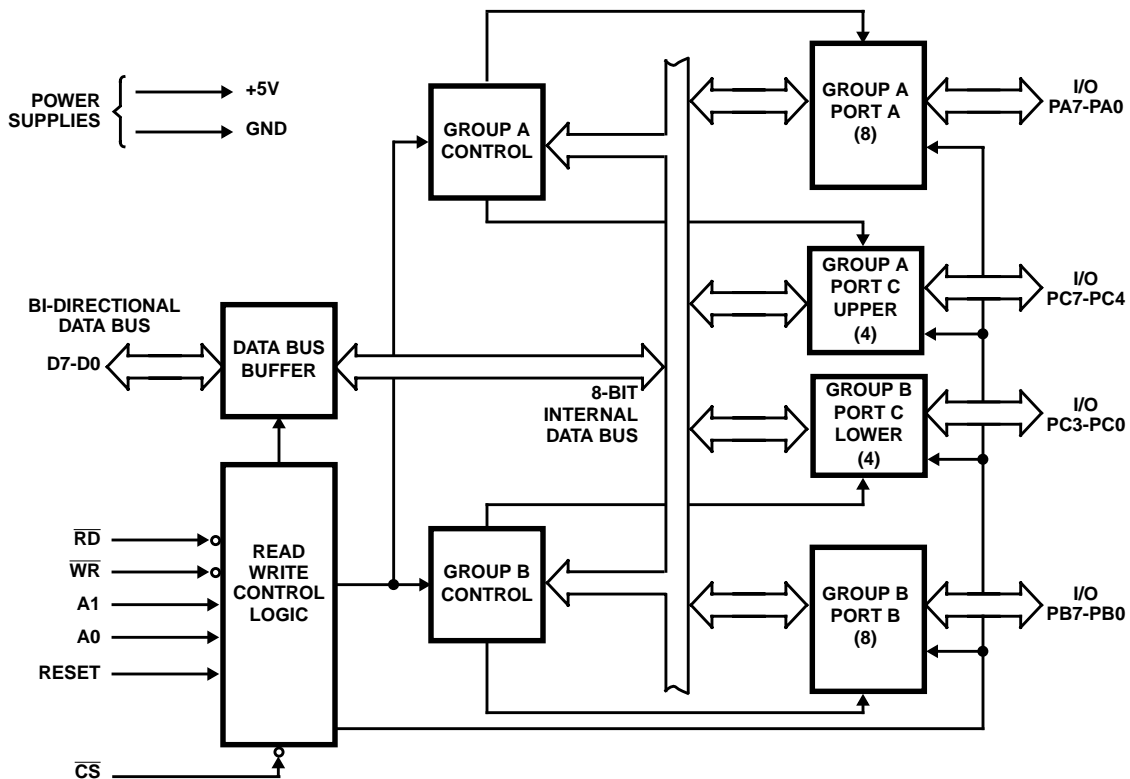
Functional Description

Data Bus Buffer

This three-state bi-directional 8-bit buffer is used to interface WS82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

(CS) Chip Select. A "low" on this input pin enables the communcation between the WS82C55A and the CPU

(RD) Read. A "low" on this input pin enables 82C55A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the WS82C55A

(WR) Write. A "low" on this input pin enables the CPU to write data or control words into the WS82C55A

(A0 and A1) Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word register. They are normally connected to the least significant bits of the address bus (A0 and A1).
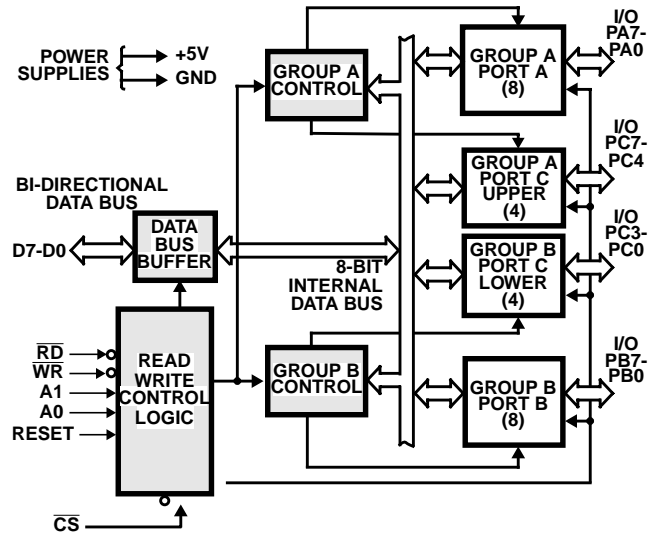

GURE 1. 82C55A BLOCK DIAGRAM. DATA BUS BUFFER, READ/WRITE, GROUP A & B CONTROL LOGIC FUNCTIONS

(RESET) Reset. A "high" on this input initializes the control register to 9Bh and all ports (A, B, C) are set to the input mode. "Bus hold" devices internal to the 82C55A will hold the I/O port inputs to a logic "1" state with a maximum hold current of 400μA.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the WS82C55A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the WS82C55A

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A and Port C upper (C7 - C4)

Control Group B - Port B and Port C lower (C3 - C0)

The control word register can be both written and read as shown in the "Basic Operation" table. Figure 4 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic "1", as this implies control word mode information.

WS **82C55A BASIC OPERATION**

A1	A0	RD	WR	CS	INPUT OPERATION (READ)
0	0	0	1	0	Port A → Data Bus
0	1	0	1	0	Port B → Data Bus
1	0	0	1	0	Port C → Data Bus
1	1	0	1	0	Control Word → Data Bus
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	Data Bus → Port A
0	1	1	0	0	Data Bus → Port B
1	0	1	0	0	Data Bus → Port C
1	1	1	0	0	Data Bus → Control
					DISABLE FUNCTION
X	X	X	X	1	Data Bus → Three-State
X	X	1	1	0	Data Bus → Three-State

Ports A, B, and C

The WS82C55A contains three 8-bit ports (A, B, and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the WS82C55A

Port A One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus-hold devices are present on Port A. See Figure 2A.

Port B One 8-bit data input/output latch/buffer and one 8-bit data input buffer. See Figure 2B.

Port C One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal output and status signal inputs in conjunction with ports A and B. See Figure 2B.
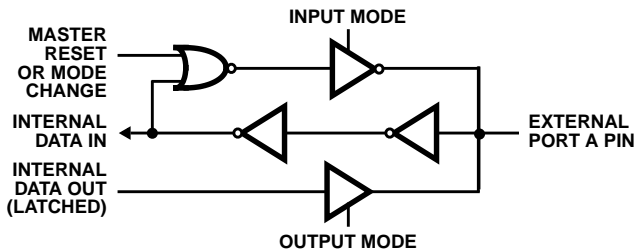

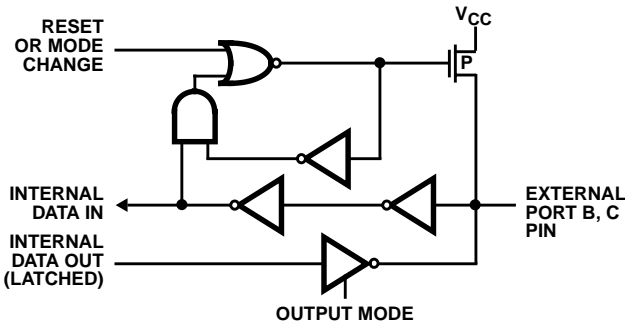**FIGURE 2A. PORT A BUS-HOLD CONFIGURATION**

FIGURE 2B. PORT B AND C BUS-HOLD CONFIGURATION

FIGURE 2. BUS-HOLD CONFIGURATION

Operational Description

Mode Selection

There are three basic modes of operation than can be selected by the system software:

    Mode 0 - Basic Input/Output
    Mode 1 - Strobed Input/Output
    Mode 2 - Bi-directional Bus

When the reset input goes "high", all ports will be set to the input mode with all 24 port lines held at a logic "one" level by internal bus hold devices. After the reset is removed, the WS82C55A can remain in the input mode with no additional initialization required. This eliminates the need to pullup or pull-down resistors in all-CMOS designs. The control word

register will contain 9Bh. During the execution of the system program, any of the other modes may be selected using a single output instruction. This allows a single 82C55A to service a variety of peripheral devices with a simple software maintenance routine. Any port programmed as an output port is initialized to all zeros when the control word is written.
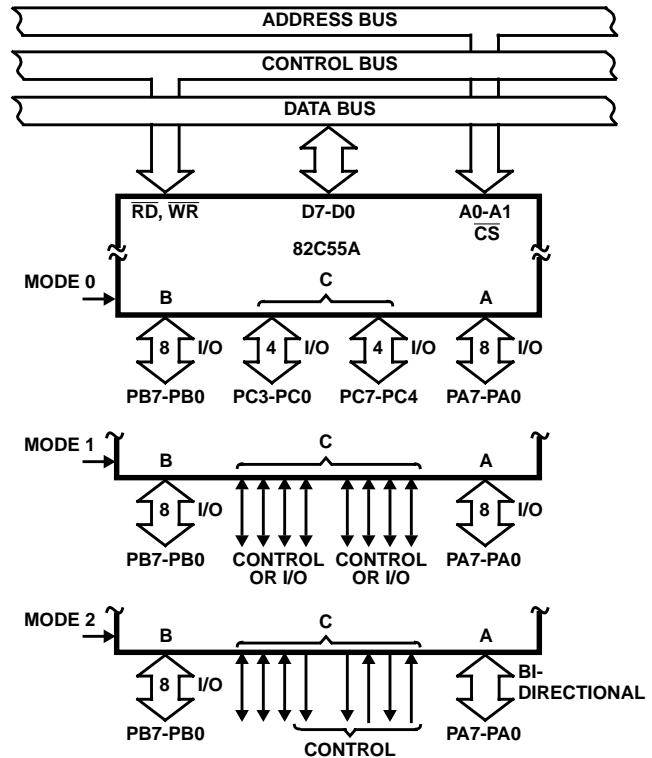

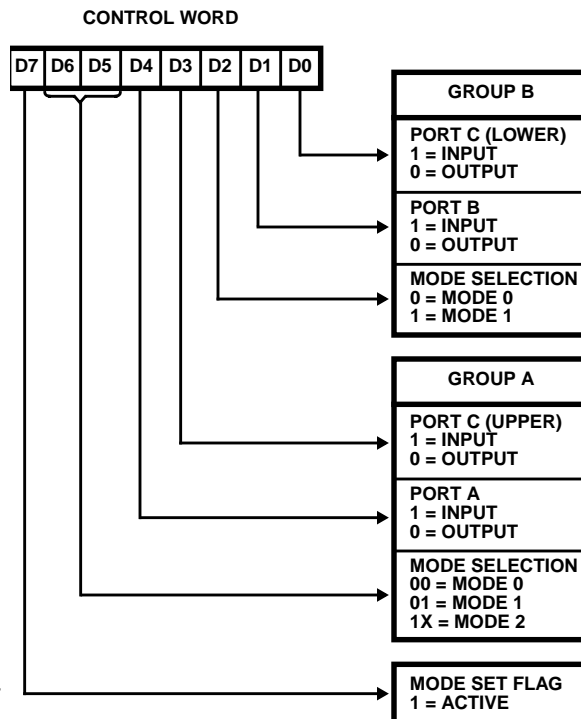**FIGURE 3. BASIC MODE DEFINITIONS AND BUS INTERFACE**

FIGURE 4. MODE DEFINITION FORMAT

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance: Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

The mode definitions and possible mode combinations may seem confusing at first, but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 82C55A has taken into account things such as efficient PC board layout, control signal definition vs. PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature (Figure 5)

Any of the eight bits of Port C can be Set or Reset using a single Output instruction. This feature reduces software requirements in control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were output ports.
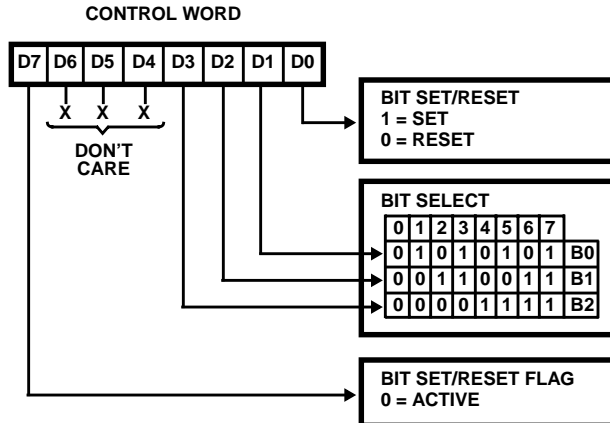

FIGURE 5. BIT SET/RESET FORMAT

Interrupt Control Functions

When WS82C55A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the programmer to enable or disable a CPU interrupt by a specific I/O device without affecting any other device in the interrupt structure.

INTE Flip-Flop Definition

(BIT-SET)-INTE is SET - Interrupt Enable

(BIT-RESET)-INTE is Reset - Interrupt Disable

NOTE: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

Mode 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No handshaking is required, data is simply written to or read from a specific port.

Mode 0 Basic Functional Definitions:

• Two 8-bit ports and two 4-bit ports

• Any Port can be input or output

• Outputs are latched

• Input are not latched

• 16 different Input/Output configurations possible

MODE 0 PORT DEFINITION

A		B		GROUP A			GROUP B	
D4	D3	D1	D0	PORT A	PORT C (Upper)	#	PORT B	PORT C (Lower)
0	0	0	0	Output	Output	0	Output	Output
0	0	0	1	Output	Output	1	Output	Input
0	0	1	0	Output	Output	2	Input	Output
0	0	1	1	Output	Output	3	Input	Input
0	1	0	0	Output	Input	4	Output	Output
0	1	0	1	Output	Input	5	Output	Input
0	1	1	0	Output	Input	6	Input	Output
0	1	1	1	Output	Input	7	Input	Input
1	0	0	0	Input	Output	8	Output	Output
1	0	0	1	Input	Output	9	Output	Input
1	0	1	0	Input	Output	10	Input	Output
1	0	1	1	Input	Output	11	Input	Input
1	1	0	0	Input	Input	12	Output	Output
1	1	0	1	Input	Input	13	Output	Input
1	1	1	0	Input	Input	14	Input	Output
1	1	1	1	Input	Input	15	Input	Input

Mode 0 (Basic Input)
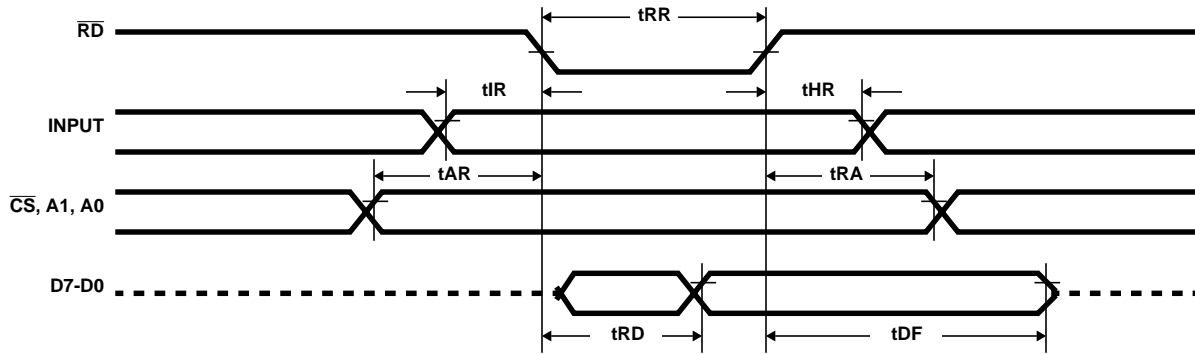
Mode 0 (Basic Output)
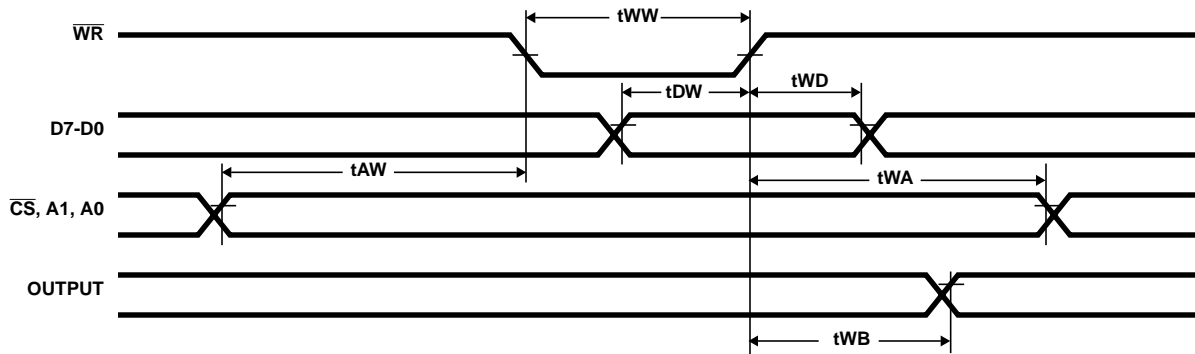
Mode 0 Configurations

CONTROL WORD #0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0
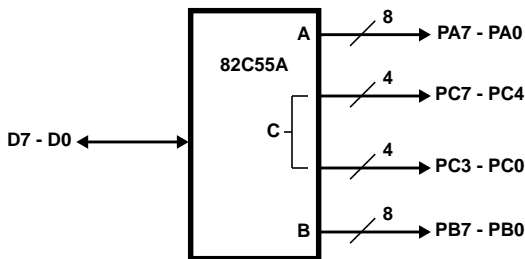
CONTROL WORD #2

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	0
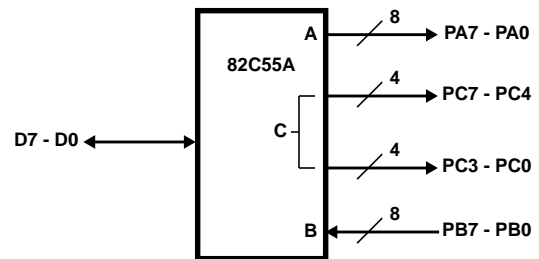
CONTROL WORD #1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	1
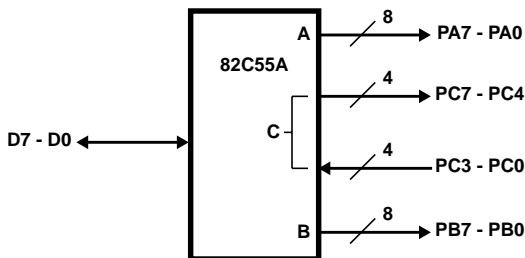
CONTROL WORD #3

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	1
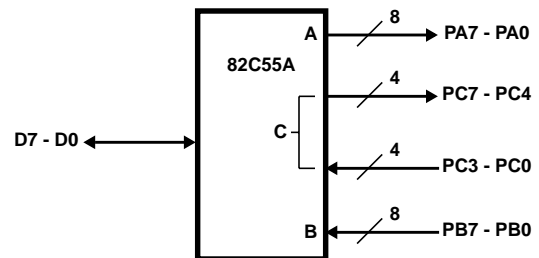
Mode 0 Configurations (Continued)

CONTROL WORD #4

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	0

82C55A

D7 - D0

A → 8 → PA7 - PA0
C ← 4 → PC7 - PC4
C → 4 → PC3 - PC0
B → 8 → PB7 - PB0

CONTROL WORD #5

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	1

82C55A

D7 - D0

A → 8 → PA7 - PA0
C ← 4 → PC7 - PC4
C → 4 → PC3 - PC0
B → 8 → PB7 - PB0

CONTROL WORD #6

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	0

82C55A

D7 - D0

A → 8 → PA7 - PA0
C ← 4 → PC7 - PC4
C → 4 → PC3 - PC0
B ← 8 → PB7 - PB0

CONTROL WORD #7

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	1

82C55A

D7 - D0

A → 8 → PA7 - PA0
C ← 4 → PC7 - PC4
C → 4 → PC3 - PC0
B ← 8 → PB7 - PB0
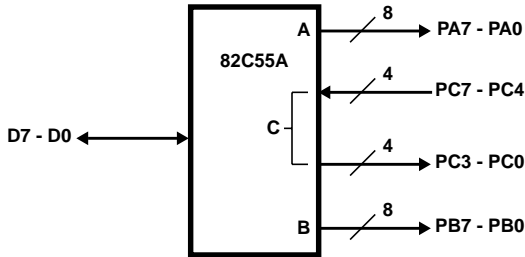
CONTROL WORD #8

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	0

82C55A

D7 - D0

A ← 8 → PA7 - PA0
C → 4 → PC7 - PC4
C → 4 → PC3 - PC0
B → 8 → PB7 - PB0
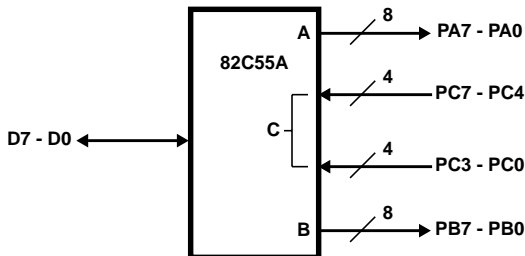
CONTROL WORD #9

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	1

82C55A

D7 - D0

A ← 8 → PA7 - PA0
C → 4 → PC7 - PC4
C ← 4 → PC3 - PC0
B → 8 → PB7 - PB0
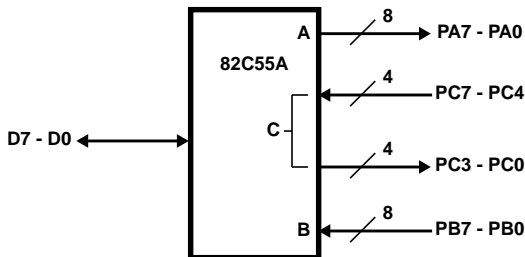
CONTROL WORD #10

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	1	0

82C55A

D7 - D0

A ← 8 → PA7 - PA0
C → 4 → PC7 - PC4
C → 4 → PC3 - PC0
B ← 8 → PB7 - PB0
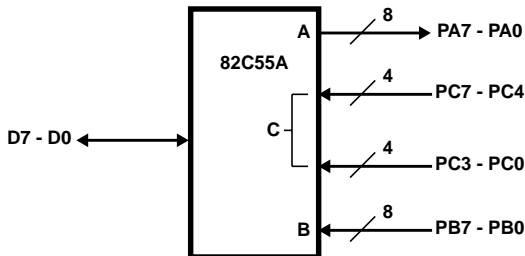
CONTROL WORD #11

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	1	1

82C55A

D7 - D0

A ← 8 → PA7 - PA0
C → 4 → PC7 - PC4
C ← 4 → PC3 - PC0
B ← 8 → PB7 - PB0
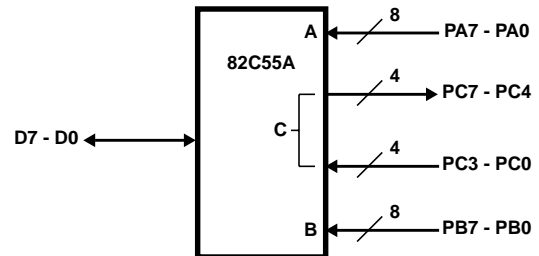
Mode 0 Configurations (Continued)

CONTROL WORD #12

D7	D6	D5	D4	D3	D2	D1	D0
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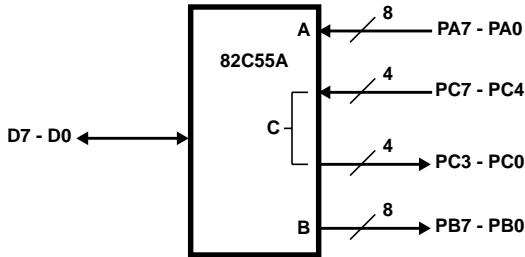
CONTROL WORD #14

D7	D6	D5	D4	D3	D2	D1	D0
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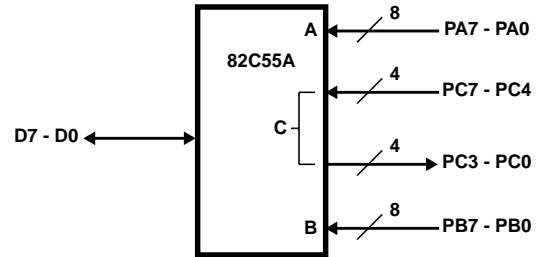
CONTROL WORD #13

D7	D6	D5	D4	D3	D2	D1	D0
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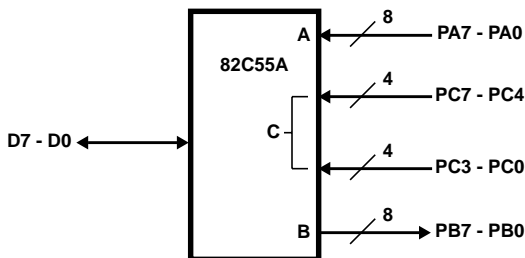
CONTROL WORD #15

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	1	1
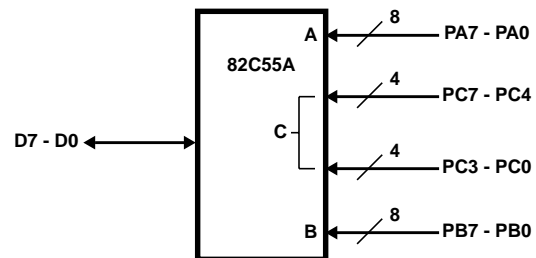
Operating Modes

Mode 1 - (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "hand shaking" signals. In mode 1, port A and port B use the lines on port C to generate or accept these "hand shaking" signals.

Mode 1 Basic Function Definitions:

• Two Groups (Group A and Group B)

• Each group contains one 8-bit port and one 4-bit control/data port

• The 8-bit data port can be either input or output. Both inputs and outputs are latched.

• The 4-bit port is used for control and status of the 8-bit port.

Input Control Signal Definition

(Figures 6 and 7)

STB (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch: in essence, and acknowledgment. IBF is set by $\overline{STB}$ input being low and is reset by the rising edge of the $\overline{RD}$ input.

CONTROL WORD

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	1/0			

PC6, PC7
1 = INPUT
0 = OUTPUT

CONTROL WORD

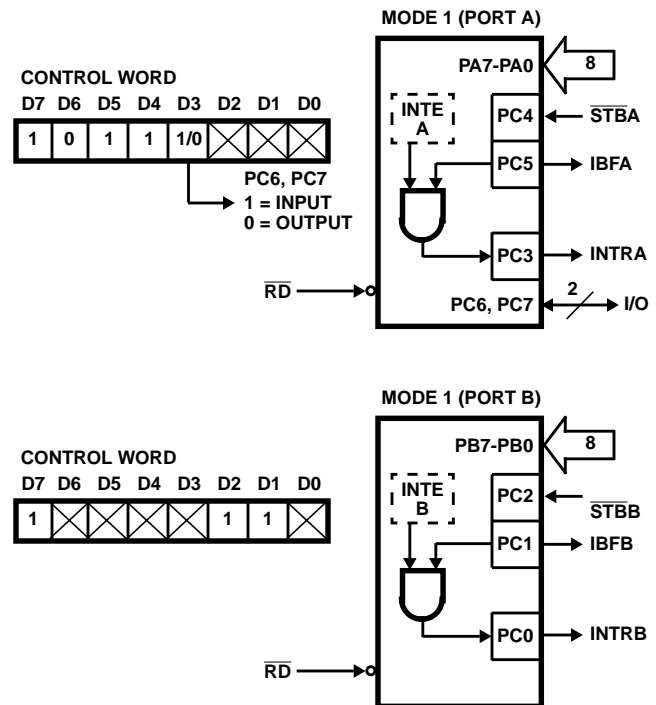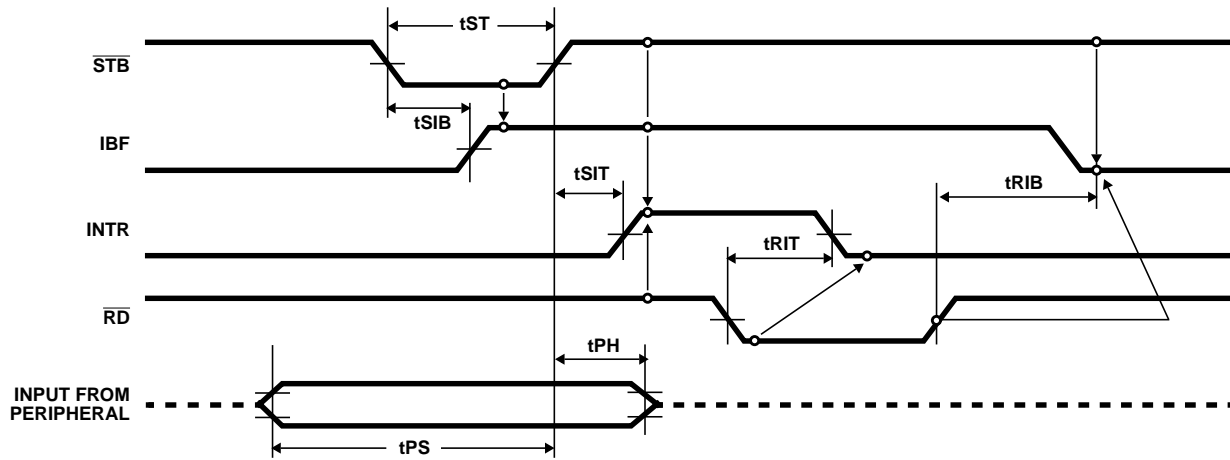| D7	D6	D5	D4	D3	D2	D1	D0
1					1	1	

FIGURE 6. MODE 1 INPUT

FIGURE 7. MODE 1 (STROBED INPUT)

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when and input device is requesting service. INTR is set by the condition: $\overline{STB}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC4.

INTE B

Controlled by bit set/reset of PC2.

Output Control Signal Definition

(Figure 8 and 9)

$\overline{OBF}$ - Output Buffer Full F/F). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to be specified port. This does not mean valid data is sent out of the part at this time since $\overline{OBF}$ can go true before data is available. Data is guaranteed valid at the rising edge of $\overline{OBF}$, (See Note 1). The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by $\overline{ACK}$ input being low.

$\overline{ACK}$ - Acknowledge Input). A "low" on this input informs the 82C55A that the data from Port A or Port B is ready to be accepted. In essence, a response from the peripheral device indicating that it is ready to accept data, (See Note 1).

INTR - (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a "one", OBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.

INTE A

Controlled by Bit Set/Reset of PC6.

INTE B

Controlled by Bit Set/Reset of PC2.

NOTE:

1. To strobe data into the peripheral device, the user must operate the strobe line in a hand shaking mode. The user needs to send $\overline{OBF}$ to the peripheral device, generates an $\overline{ACK}$ from the peripheral device and then latch data into the peripheral device on the rising edge of $\overline{OBF}$.
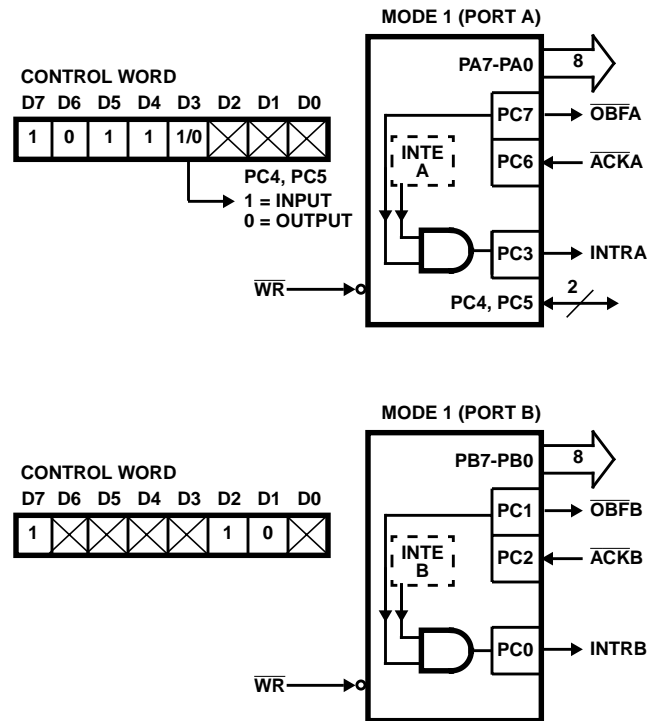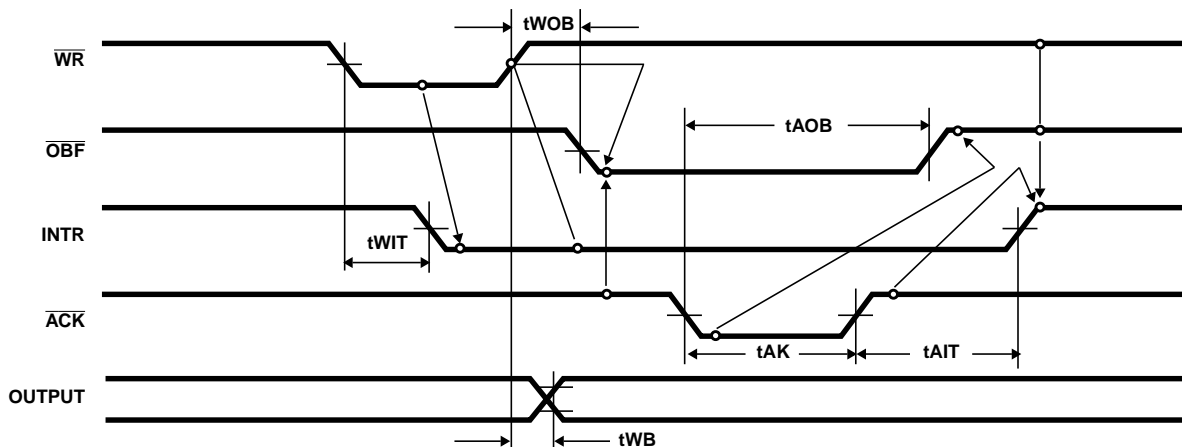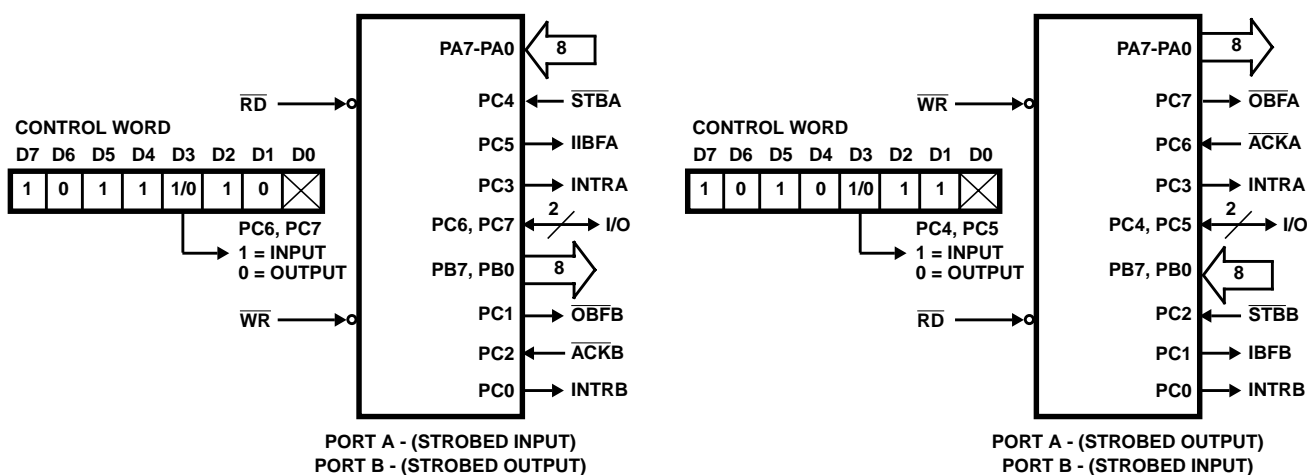

FIGURE 8. MODE 1 OUTPUT

FIGURE 9. MODE 1 (STROBED OUTPUT)

Combinations of Mode 1: Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

FIGURE 10. COMBINATIONS OF MODE 1

Operating Modes

Mode 2 (Strobed Bi-Directional Bus I/O)

The functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bi-directional bus I/O). "Hand shaking" signals are provided to maintain proper bus flow discipline similar to Mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:

• Used in Group A only
• One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C)
• Both inputs and outputs are latched
• The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A)

Bi-Directional Bus I/O Control Signal Definition

(Figures 11, 12, 13, 14)

INTR - (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ - (Output Buffer Full). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to port A.

$\overline{ACK}$ - (Acknowledge). A "low" on this input enables the three-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 - (The INTE flip-flop associated with $\overline{OBF}$). Controlled by bit set/reset of PC4.

Input Operations

$\overline{STB}$ - (Strobe Input). A "low" on this input loads data into the input latch.

IBF - (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 - (The INTE flip-flop associated with IBF). Controlled by bit set/reset of PC4.

CONTROL WORD

D7	D6	D5	D4	D3	D2	D1	D0
1	1	░	░	░	1/0	1/0	1/0

PC2-PC0
1 = INPUT
0 = OUTPUT

PORT B
1 = INPUT
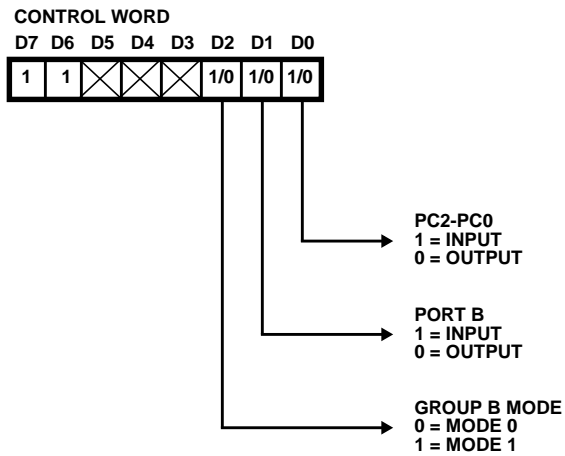0 = OUTPUT

GROUP B MODE
0 = MODE 0
1 = MODE 1

FIGURE 11. MODE CONTROL WORD
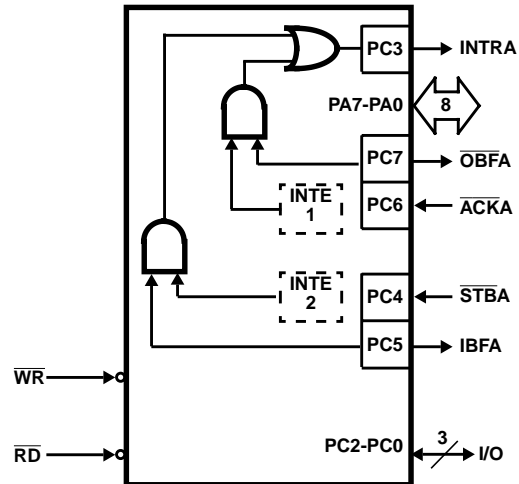
FIGURE 12. MODE 2
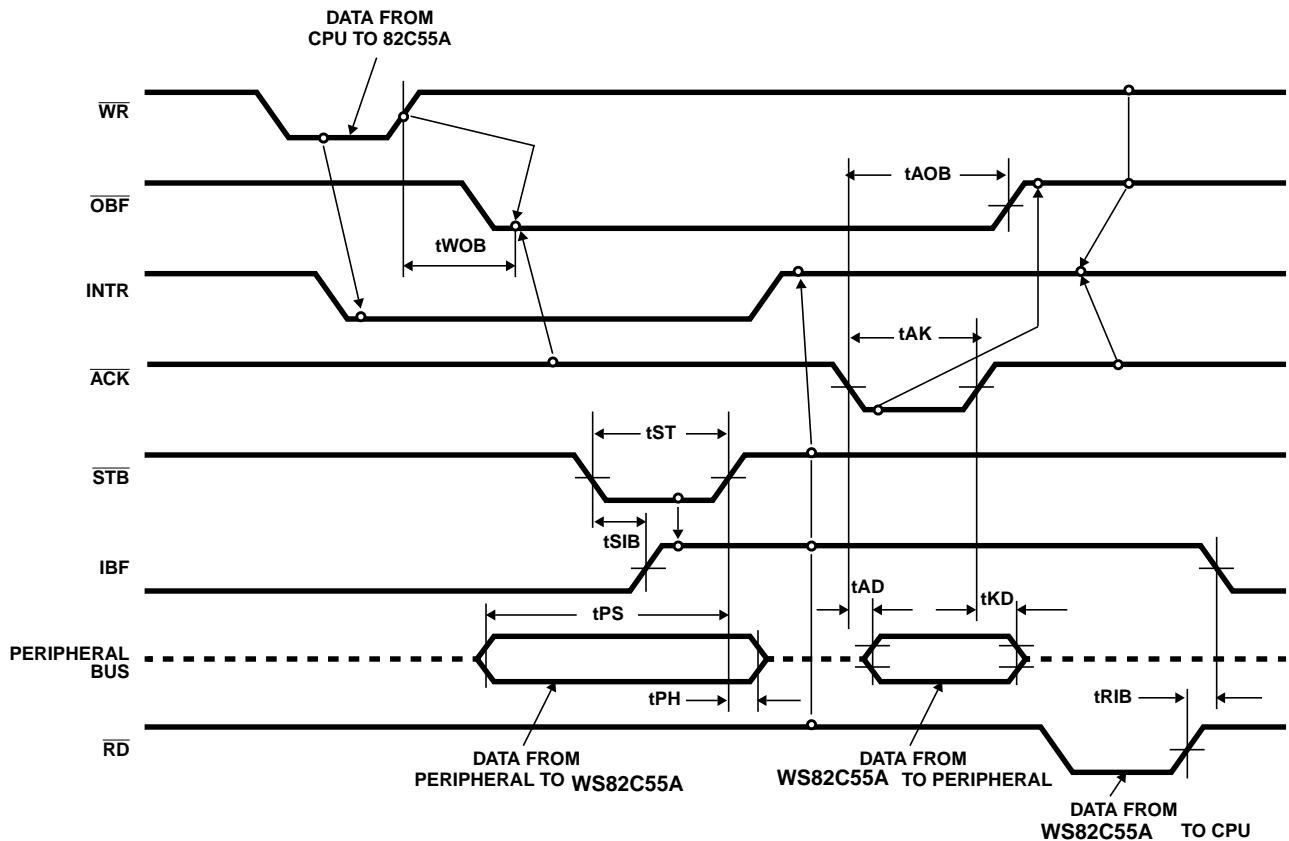
FIGURE 13. MODE 2 (BI-DIRECTIONAL)

NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before RD is permissible. (INTR = IBF • MASK • $\overline{STB}$ • $\overline{RD}$ ÷ $\overline{OBF}$ • MASK • $\overline{ACK}$ • $\overline{WR}$)

MODE 2 AND MODE 0 (INPUT)

CONTROL WORD

D7	D6	D5	D4	D3	D2	D1	D0
1	1	✕	✕	✕	0	1	1/0

PC2-PC0
1 = INPUT
0 = OUTPUT

$\overline{RD}$

$\overline{WR}$

PC3 → INTRA
PA7-PA0 ⟷ 8
PC7 → $\overline{OBFA}$
PC6 ← $\overline{ACKA}$
PC4 ← $\overline{STBA}$
PC5 → IBFA
PC2-PC0 3 → I/O
PB7-PB0 ← 8

MODE 2 AND MODE 0 (OUTPUT)

CONTROL WORD

D7	D6	D5	D4	D3	D2	D1	D0
1	1	✕	✕	✕	0	0	1/0

PC2-PC0
1 = INPUT
0 = OUTPUT

$\overline{RD}$

$\overline{WR}$

PC3 → INTRA
PA7-PA0 ⟷ 8
PC7 → $\overline{OBFA}$
PC6 ← $\overline{ACKA}$
PC4 ← $\overline{STBA}$
PC5 → IBFA
PC2-PC0 3 → I/O
PB7, PB0 → 8

MODE 2 AND MODE 1 (OUTPUT)

CONTROL WORD

D7	D6	D5	D4	D3	D2	D1	D0
1	1	✕	✕	✕	1	0	✕

$\overline{RD}$

$\overline{WR}$

PC3 → INTRA
PA7-PA0 ⟷ 8
PC7 → $\overline{OBFA}$
PC6 ← $\overline{ACKA}$
PC4 ← $\overline{STBA}$
PC5 → IBFA
PB7-PB0 → 8
PC1 → $\overline{OBFB}$
PC2 ← $\overline{ACKB}$
PC0 → INTRB

MODE 2 AND MODE 1 (INPUT)

CONTROL WORD

D7	D6	D5	D4	D3	D2	D1	D0
1	1	✕	✕	✕	1	1	✕

$\overline{RD}$

$\overline{WR}$

PC3 → INTRA
PA7-PA0 ⟷ 8
PC7 → $\overline{OBFA}$
PC6 ← $\overline{ACKA}$
PC4 ← $\overline{STBA}$
PC5 → IBFA
PB7-PB0 ← 8
PC2 ← $\overline{STBB}$
PC1 → IBFB
PC0 → INTRB

FIGURE 14. MODE 2 COMBINATIONS

MODE DEFINITION SUMMARY

	MODE 0		MODE 1		MODE 2
	IN	**OUT**	**IN**	**OUT**	**GROUP A ONLY**
PA0	In	Out	In	Out	←——————→
PA1	In	Out	In	Out	←——————→
PA2	In	Out	In	Out	←——————→
PA3	In	Out	In	Out	←——————→
PA4	In	Out	In	Out	←——————→
PA5	In	Out	In	Out	←——————→
PA6	In	Out	In	Out	←——————→
PA7	In	Out	In	Out	←——————→
PB0	In	Out	In	Out	
PB1	In	Out	In	Out	
PB2	In	Out	In	Out	
PB3	In	Out	In	Out	Mode 0
PB4	In	Out	In	Out	or Mode 1
PB5	In	Out	In	Out	Only
PB6	In	Out	In	Out	
PB7	In	Out	In	Out	
PC0	In	Out	INTRB	INTRB	I/O
PC1	In	Out	IBFB	$\overline{OBFB}$	I/O
PC2	In	Out	$\overline{STBB}$	$\overline{ACKB}$	I/O
PC3	In	Out	INTRA	INTRA	INTRA
PC4	In	Out	$\overline{STBA}$	I/O	$\overline{STBA}$
PC5	In	Out	IBFA	I/O	IBFA
PC6	In	Out	I/O	$\overline{ACKA}$	$\overline{ACKA}$
PC7	In	Out	I/O	$\overline{OBFA}$	$\overline{OBFA}$

Special Mode Combination Considerations

There are several combinations of modes possible. For any combination, some or all of Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "Set Mode" command.
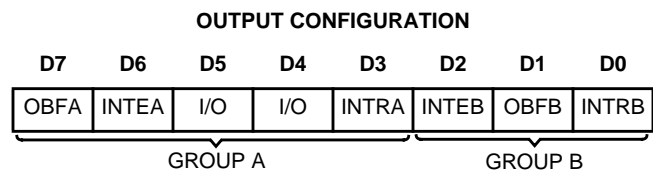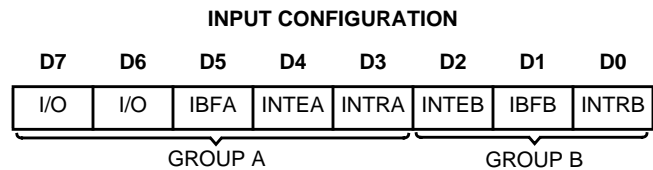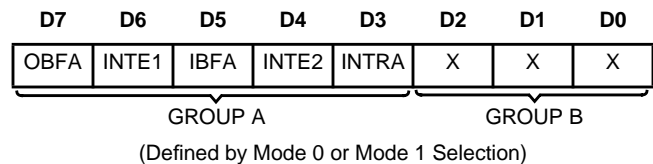
During a read of Port C, the state of all the Port C lines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 17.

Through a "Write Port C" command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a "Write Port C" command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in Mode 1 group or to change an interrupt enable flag, the "Set/Reset Port C Bit" command must be used.

With a "Set/Reset Port Cea Bit" command, any Port C line programmed as an output (including IBF and $\overline{OBF}$) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, associated with Port C fare not affected by a "Set/Reset Port C Bit" command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the "Set Reset Port C Bit" command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 17.

INPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
I/O	I/O	IBFA	INTEA	INTRA	INTEB	IBFB	INTRB
GROUP A					GROUP B		

OUTPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
OBFA	INTEA	I/O	I/O	INTRA	INTEB	OBFB	INTRB
GROUP A					GROUP B		

FIGURE 15. MODE 1 STATUS WORD FORMAT

D7	D6	D5	D4	D3	D2	D1	D0
OBFA	INTE1	IBFA	INTE2	INTRA	X	X	X
GROUP A					GROUP B		

(Defined by Mode 0 or Mode 1 Selection)

FIGURE 16. MODE 2 STATUS WORD FORMAT

Current Drive Capability

Any output on Port A, B or C can sink or source 2.5mA. This feature allows the 82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status (Figures 15 and 16)

In Mode 0, Port C transfers data to or from the peripheral device. When the 82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts "hand shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is not special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

INTERRUPT ENABLE FLAG	POSITION	ALTERNATE PORT C PIN SIGNAL (MODE)
INTE B	PC2	$\overline{ACKB}$ (Output Mode 1) or $\overline{STBB}$ (Input Mode 1)
INTE A2	PC4	$\overline{STBA}$ (Input Mode 1 or Mode 2)
INTE A1	PC6	$\overline{ACKA}$ (Output Mode 1 or Mode 2)

FIGURE 17. INTERRUPT ENABLE FLAGS IN MODES 1 AND 2

Applications of the WS82C55A-5

WS82C55A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and flexible enough to inter-face almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the WS82C55A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the WS82C55A to exactly "fit" the application. Figures 18 through 24 present a few examples of typical applications of the WS82C55A
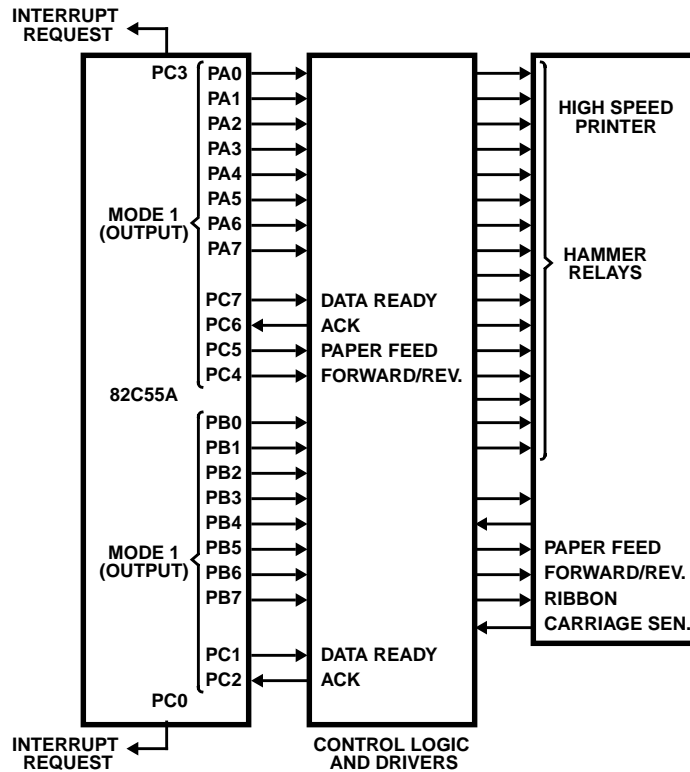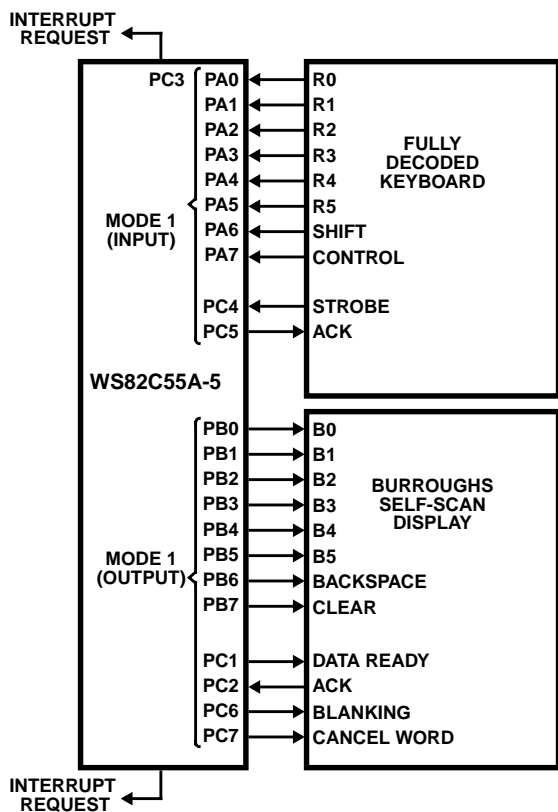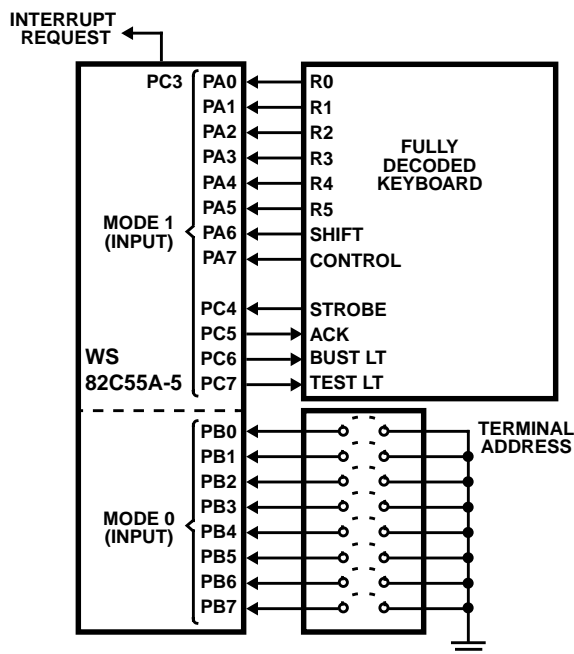

FIGURE 18. PRINTER INTERFACE

INTERRUPT
REQUEST

PC3 — PA0 ← R0
PA1 ← R1
PA2 ← R2
PA3 ← R3 FULLY
PA4 ← R4 DECODED
PA5 ← R5 KEYBOARD
MODE 1 PA6 ← SHIFT
(INPUT) PA7 ← CONTROL

PC4 ← STROBE
PC5 ← ACK

WS82C55A-5

PB0 → B0
PB1 → B1
PB2 → B2
PB3 → B3 BURROUGHS
PB4 → B4 SELF-SCAN
MODE 1 PB5 → B5 DISPLAY
(OUTPUT) PB6 → BACKSPACE
PB7 → CLEAR

PC1 → DATA READY
PC2 ← ACK
PC6 → BLANKING
PC7 → CANCEL WORD

INTERRUPT
REQUEST

FIGURE 19. KEYBOARD AND DISPLAY INTERFACE

INTERRUPT
REQUEST

PC3 — PA0 ← R0
PA1 ← R1
PA2 ← R2
PA3 ← R3 FULLY
PA4 ← R4 DECODED
PA5 ← R5 KEYBOARD
MODE 1 PA6 ← SHIFT
(INPUT) PA7 ← CONTROL

PC4 ← STROBE
PC5 ← ACK
WS PC6 → BUST LT
82C55A-5 PC7 → TEST LT

PB0 ←
PB1 ←
PB2 ←
PB3 ← TERMINAL
PB4 ← ADDRESS
MODE 0 PB5 ←
(INPUT) PB6 ←
PB7 ←

**FIGURE 20. KEYBOARD AND TERMINAL ADDRESS
INTERFACE**

PA0 → LSB
PA1 →
PA2 →
PA3 →
PA4 → 12-BIT
MODE 0 PA5 → A/D
(OUTPUT) PA6 → CONVERTER
PA7 → (DAC) ANALOG
PC4 → OUTPUT
PC5 →
PC6 →
PC7 →

WS82C55A-5

PC0 → STB DATA
PC1 →
BIT
SET/RESET PC2 → SAMPLE EN
PC3 → STB

PB0 ← LSB
PB1 ←
PB2 ← 8-BIT
MODE 0 PB3 ← D/A
(INPUT) PC4 ← CONVERTER ANALOG
PC5 ← (ADC) INPUT
PC6 ←
PC7 ← MAB
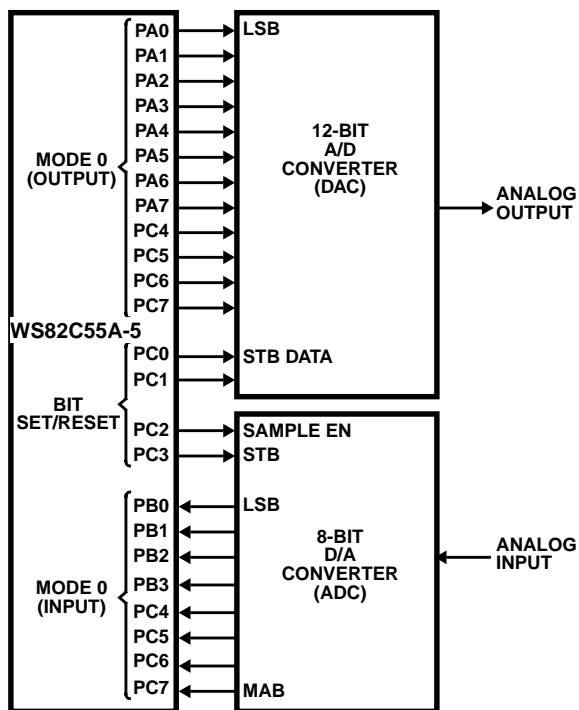
FIGURE 21. DIGITAL TO ANALOG, ANALOG TO DIGITAL

INTERRUPT
REQUEST

PC3 — PA0 → R0
PA1 → R1
PA2 → R2 CRT CONTROLLER
PA3 → R3 • CHARACTER GEN.
PA4 → R4 • REFRESH BUFFER
PA5 → R5 • CURSOR CONTROL
MODE 1 PA6 → SHIFT
(OUTPUT) PA7 → CONTROL

PC7 → DATA READY
PC6 ← ACK
PC5 → BLANKED
PC4 → BLACK/WHITE

WS82C55A-5

PC2 → ROW STB
PC1 → COLUMN STB
PC0 → CURSOR H/V STB

PB0 →
PB1 →
MODE 0 PB2 →
(OUTPUT) PB3 → CURSOR/ROW/COLUMN
PB4 → ADDRESS
PB5 → H&V
PB6 →
PB7 →
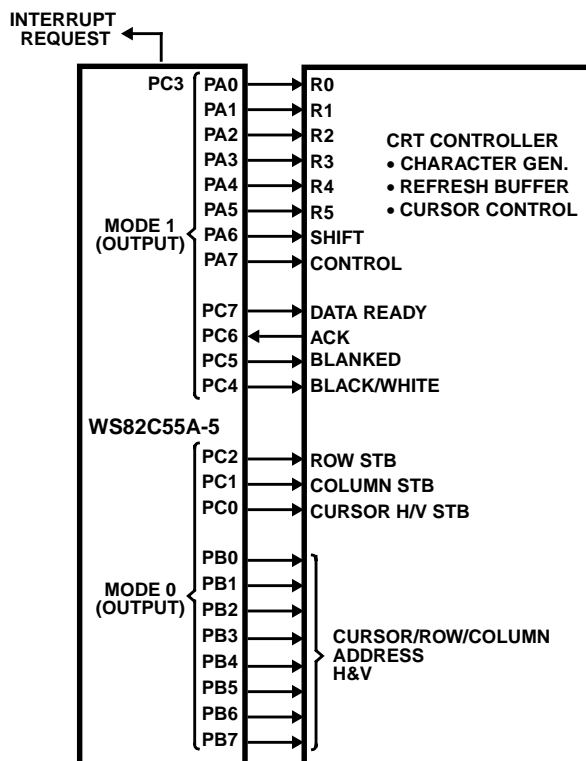
FIGURE 22. BASIC CRT CONTROLLER INTERFACE

INTERRUPT
REQUEST

PC3

WS82C55A-5		FLOPPY DISK CONTROLLER AND DRIVE
MODE 2	PA0	D0
	PA1	D1
	PA2	D2
	PA3	D3
	PA4	D4
	PA5	D5
	PA6	D6
	PA7	D7
	PC4	DATA STB
	PC5	ACK (IN)
	PC7	DATA READY
	PC6	ACK (OUT)
	PC2	TRACK "0" SENSOR
	PC1	SYNC READY
	PC0	INDEX
MODE 0 (OUTPUT)	PB0	ENGAGE HEAD
	PB1	FORWARD/REV.
	PB2	READ ENABLE
	PB3	WRITE ENABLE
	PB4	DISC SELECT
	PB5	ENABLE CRC
	PB6	TEST
	PB7	BUSY LT
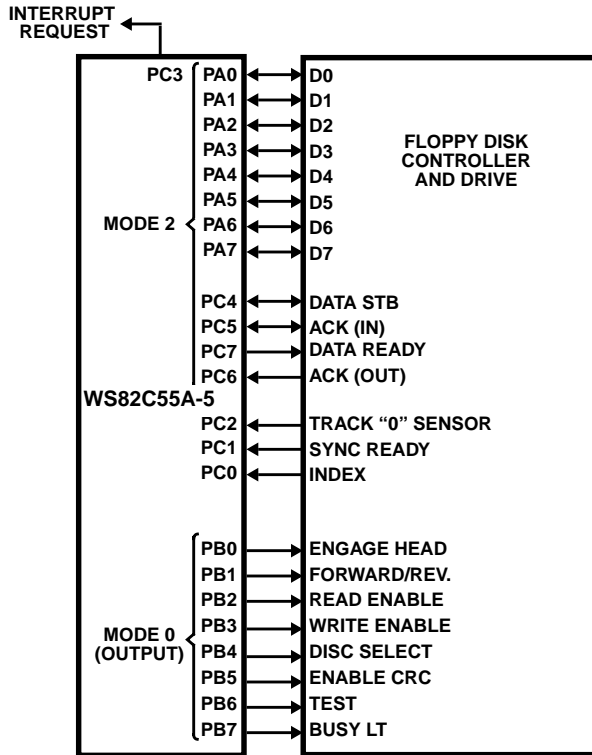
FIGURE 23. BASIC FLOPPY DISC INTERFACE

INTERRUPT
REQUEST

PC3

WS82C55A-5		B LEVEL PAPER TAPE READER
MODE 1 (INPUT)	PA0	R0
	PA1	R1
	PA2	R2
	PA3	R3
	PA4	R4
	PA5	R5
	PA6	R6
	PA7	R7
	PC4	$\overline{STB}$
	PC5	$\overline{ACK}$
	PC6	STOP/GO

MACHINE TOOL

MODE 0 (INPUT)	PC0	START/STOP
	PC1	LIMIT SENSOR (H/V)
	PC2	OUT OF FLUID
MODE 0 (OUTPUT)	PB0	CHANGE TOOL
	PB1	LEFT/RIGHT
	PB2	UP/DOWN
	PB3	HOR. STEP STROBE
	PB4	VERT. STEP STROBE
	PB5	SLEW/STEP
	PB6	FLUID ENABLE
	PB7	EMERGENCY STOP

FIGURE 24. MACHINE TOOL CONTROLLER INTERFACE

16

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage . . . .+8.0V
Input, Output or I/O Voltage . . . . GND-0.5V to V_{CC}+0.5V
ESD Classification . . . . Class 1

Operating Conditions

Voltage Range . . . . +4.5V to 5.5V
Operating Temperature Range
 WS82C55A ·$.0^oC$ to 70^oC

Thermal Information

	θ_{JA}	θ_{JC}
Thermal Resistance (Typical, Note 1)		
PDIP Package	50^oC/W	N/A

Maximum Storage Temperature Range . . . .-65^oC to 150^oC
Maximum Junction Temperature

 PDIP Package . . . . 150^oC

Die Characteristics

Gate Count . . . . 1000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

 1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V_{CC} = 5.0V ±10%; $T_A = 0^oC$ to +70^oC (WS82C55A-5);

| SYMBOL | PARAMETER | LIMITS | | UNITS | TEST CONDITIONS |
		MIN	MAX		
V_{IH}	Logical One Input Voltage	2.0 2.2	-	V	
V_{IL}	Logical Zero Input Voltage	-	0.8	V	
V_{OH}	Logical One Output Voltage	3.0 V_{CC} -0.4	-	V	I_{OH} = -2.5mA, I_{OH} = -100µA
V_{OL}	Logical Zero Output Voltage	-	0.4	V	I_{OL} +2.5mA
I_I	Input Leakage Current	-1.0	+1.0	µA	V_{IN} = V_{CC} or GND, DIP Pins: 5, 6, 8, 9, 35, 36
IO	I/O Pin Leakage Current	-10	+10	µA	VO = V_{CC} or GND DIP Pins: 27 - 34
IBHH	Bus Hold High Current	-50	-400	µA	VO = 3.0V. Ports A, B, C
IBHL	Bus Hold Low Current	50	400	µA	VO = 1.0V. Port A ONLY
IDAR	Darlington Drive Current	-2.5	Note 2, 4	mA	Ports A, B, C. Test Condition 3
ICCSB	Standby Power Supply Current	-	10	µA	V_{CC} = 5.5V, V_{IN} = V_{CC} or GND. Output Open
ICCOP	Operating Power Supply Current	-	1	mA/MHz	T_A = +25^oC, V_{CC} = 5.0V, Typical (See Note 3)

NOTES:

 2. No internal current limiting exists on Port Outputs. A resistor must be added externally to limit the current.

 3. ICCOP = 1mA/MHz of Peripheral Read/Write cycle time. (Example: 1.0µs I/O Read/Write cycle time = 1mA).

 4. Tested as V_{OH} at -2.5mA.

Capacitance $T_A = 25^oC$

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CIN	Input Capacitance	10	pF	FREQ = 1MHz, All Measurements are referenced to device GND
CI/O	I/O Capacitance	20	pF	

AC Electrical Specifications V_{CC} = +5V± 10%, GND = 0V; T_A =0°C to 70°C

SYMBOL	PARAMETER	WS82C55A*5		WS-XX82C55A		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
READ TIMING							
(1) tAR	Address Stable Before $\overline{RD}$	0	-	0	-	ns	
(2) tRA	Address Stable After $\overline{RD}$	0	-	0	-	ns	
(3) tRR	$\overline{RD}$ Pulse Width	250	-	150	-	ns	
(4) tRD	Data Valid From $\overline{RD}$	-	200	-	120	ns	1
(5) tDF	Data Float After $\overline{RD}$	10	75	10	75	ns	2
(6) tRV	Time Between $\overline{RD}$s and/or $\overline{WR}$s	300	-	300	-	ns	
WRITE TIMING							
(7) tAW	Address Stable Before $\overline{WR}$	0	-	0	-	ns	
(8) tWA	Address Stable After $\overline{WR}$	20	-	20	-	ns	
(9) tWW	$\overline{WR}$ Pulse Width	100	-	100	-	ns	
(10) tDW	Data Valid to $\overline{WR}$ High	100	-	100	-	ns	
(11) tWD	Data Valid After $\overline{WR}$ High	30	-	30	-	ns	
OTHER TIMING							
(12) tWB	$\overline{WR}$ = 1 to Output	-	350	-	350	ns	1
(13) tIR	Peripheral Data Before $\overline{RD}$	0	-	0	-	ns	
(14) tHR	Peripheral Data After $\overline{RD}$	0	-	0	-	ns	
(15) tAK	ACK Pulse Width	200	-	200	-	ns	
(16) tST	STB Pulse Width	100	-	100	-	ns	
(17) tPS	Peripheral Data Before STB High	20	-	20	-	ns	
(18) tPH	Peripheral Data After STB High	50	-	50	-	ns	
(19) tAD	ACK = 0 to Output	-	175	-	175	ns	1
(20) tKD	ACK = 1 to Output Float	20	250	20	250	ns	2
(21) tWOB	$\overline{WR}$ = 1 to OBF = 0	-	150	-	150	ns	1
(22) tAOB	ACK = 0 to OBF = 1	-	150	-	150	ns	1
(23) tSIB	STB = 0 to IBF = 1	-	150	-	150	ns	1
(24) tRIB	$\overline{RD}$ = 1 to IBF = 0	-	150	-	150	ns	1
(25) tRIT	$\overline{RD}$ = 0 to INTR = 0	-	200	-	200	ns	1
(26) tSIT	STB = 1 to INTR = 1	-	150	-	150	ns	1
(27) tAIT	ACK = 1 to INTR = 1	-	150	-	150	ns	1
(28) tWIT	$\overline{WR}$ = 0 to INTR = 0	-	200	-	200	ns	1
(29) tRES	Reset Pulse Width	500	-	500	-	ns	1,(Note)

NOTE: Period of initial Reset pulse after power-on must be at least 50μsec. Subsequent Reset pulses may be 500ns minimum.
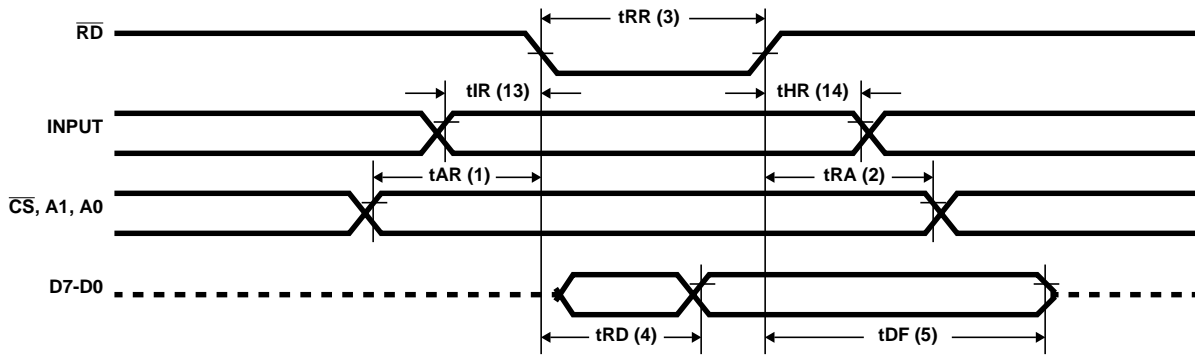
Timing Waveforms
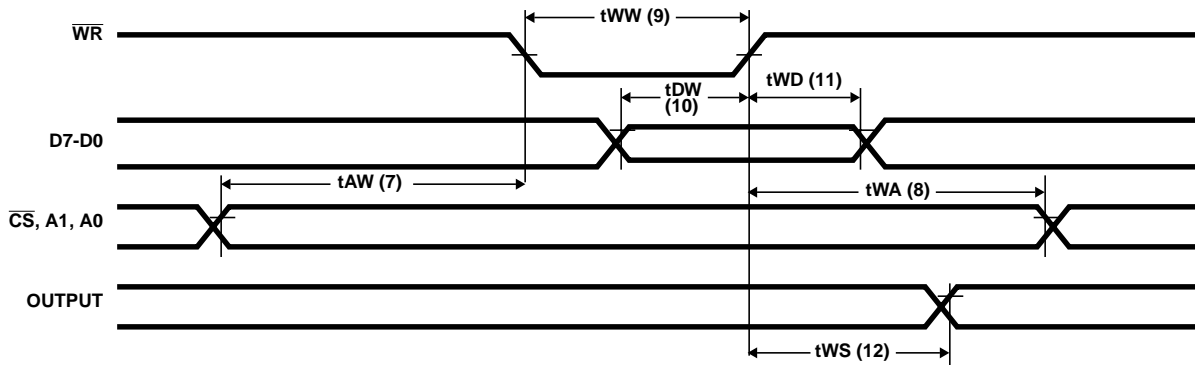

FIGURE 25. MODE 0 (BASIC INPUT)
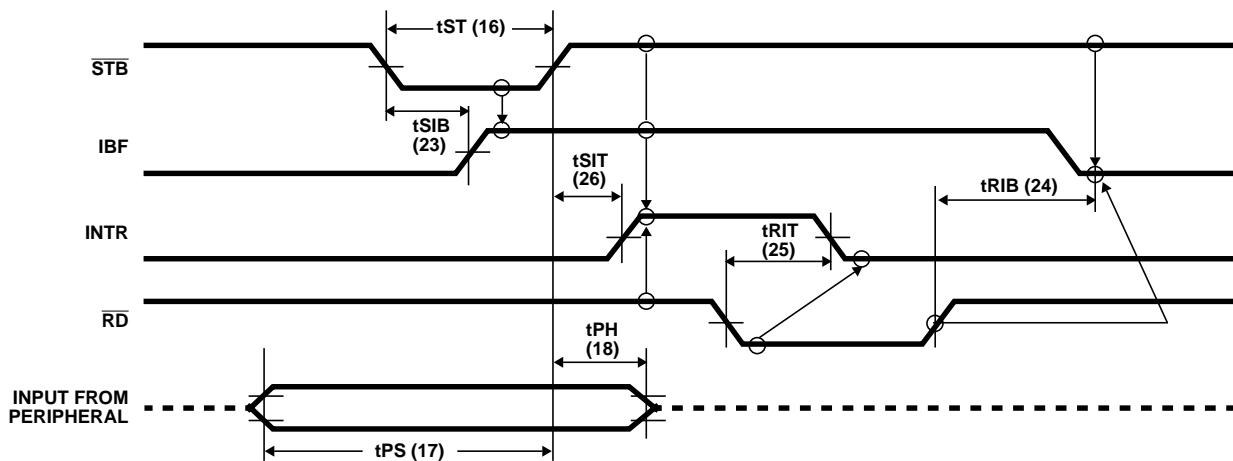

FIGURE 26. MODE 0 (BASIC OUTPUT)

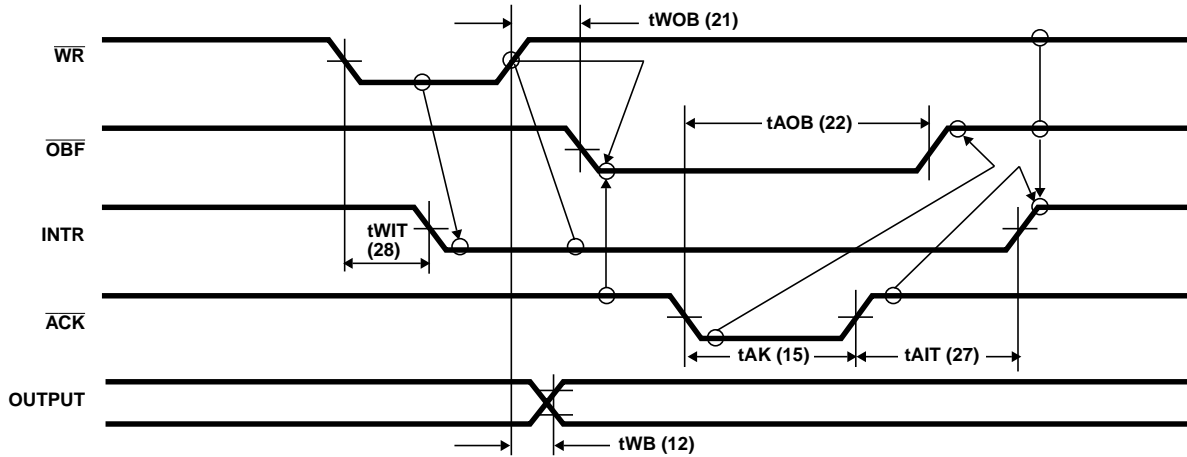**FIGURE 27. MODE 1 (STROBED INPUT)**

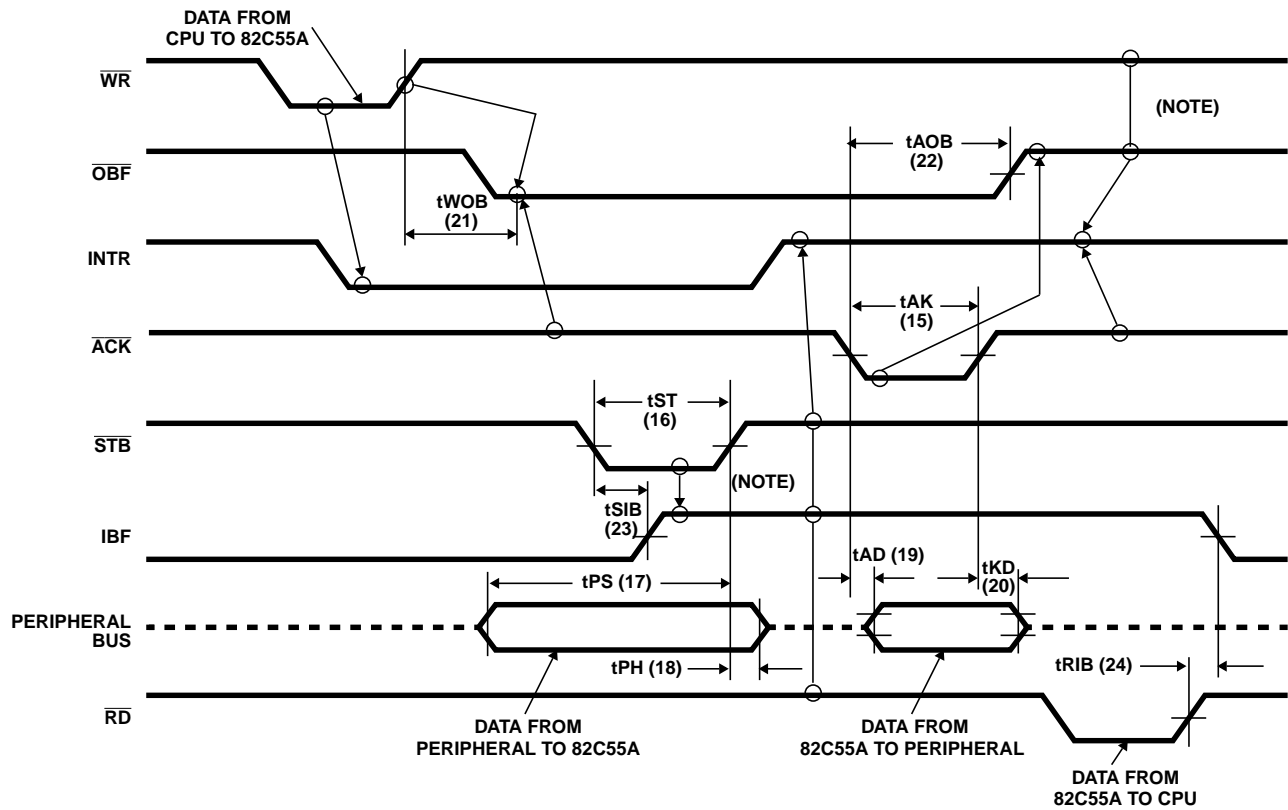## *Timing Waveforms* (Continued)

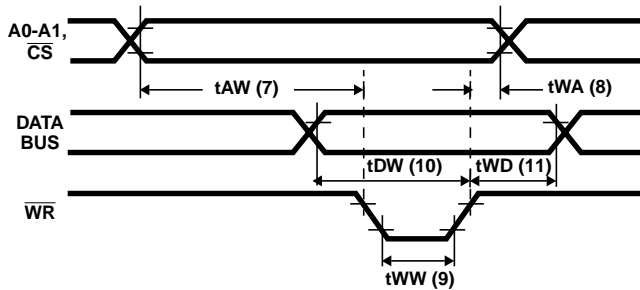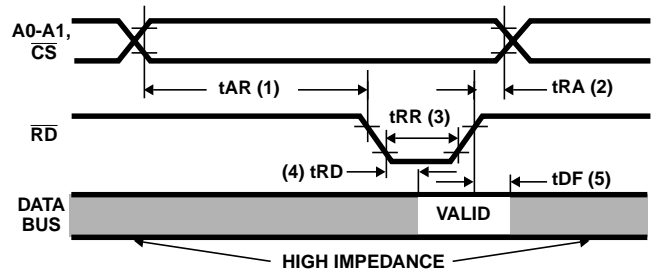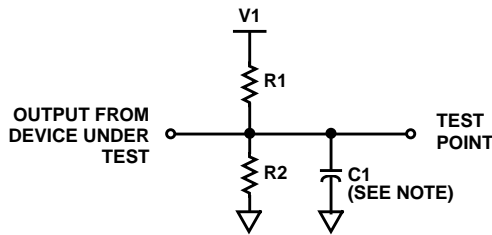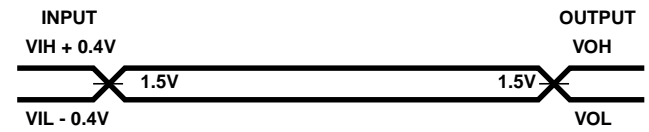**FIGURE 28. MODE 1 (STROBED OUTPUT)**

FIGURE 29. MODE 2 (BI-DIRECTIONAL)

NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible. (INTR = IBF • $\overline{MASK}$ • $\overline{STB}$ • $\overline{RD}$ • $\overline{OBF}$ • $\overline{MASK}$ • $\overline{ACK}$ • $\overline{WR}$)

Timing Waveforms (Continued)

FIGURE 30. WRITE TIMING

FIGURE 31. READ TIMING

AC Test Circuit

NOTE: Includes STRAY and JIG Capacitance
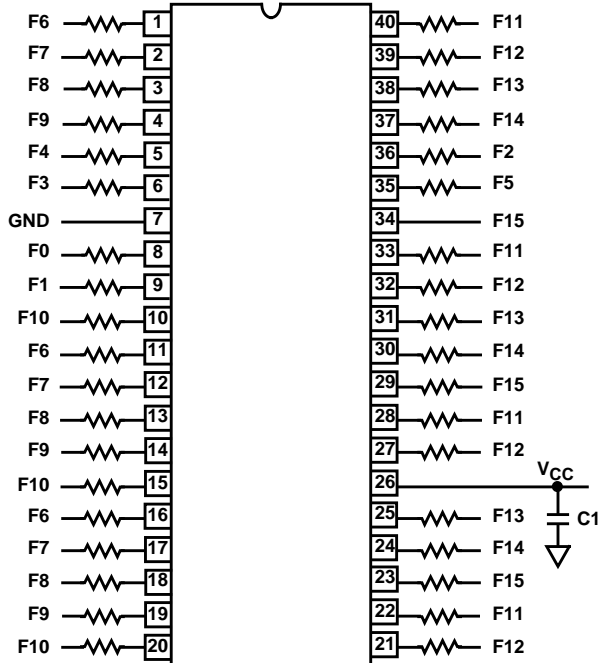
AC Testing Input, Output Waveforms

AC Testing: All AC Parameters tested as per test circuits. Input RISE and FALL times are driven at 1ns/V.

TEST CONDITION DEFINITION TABLE

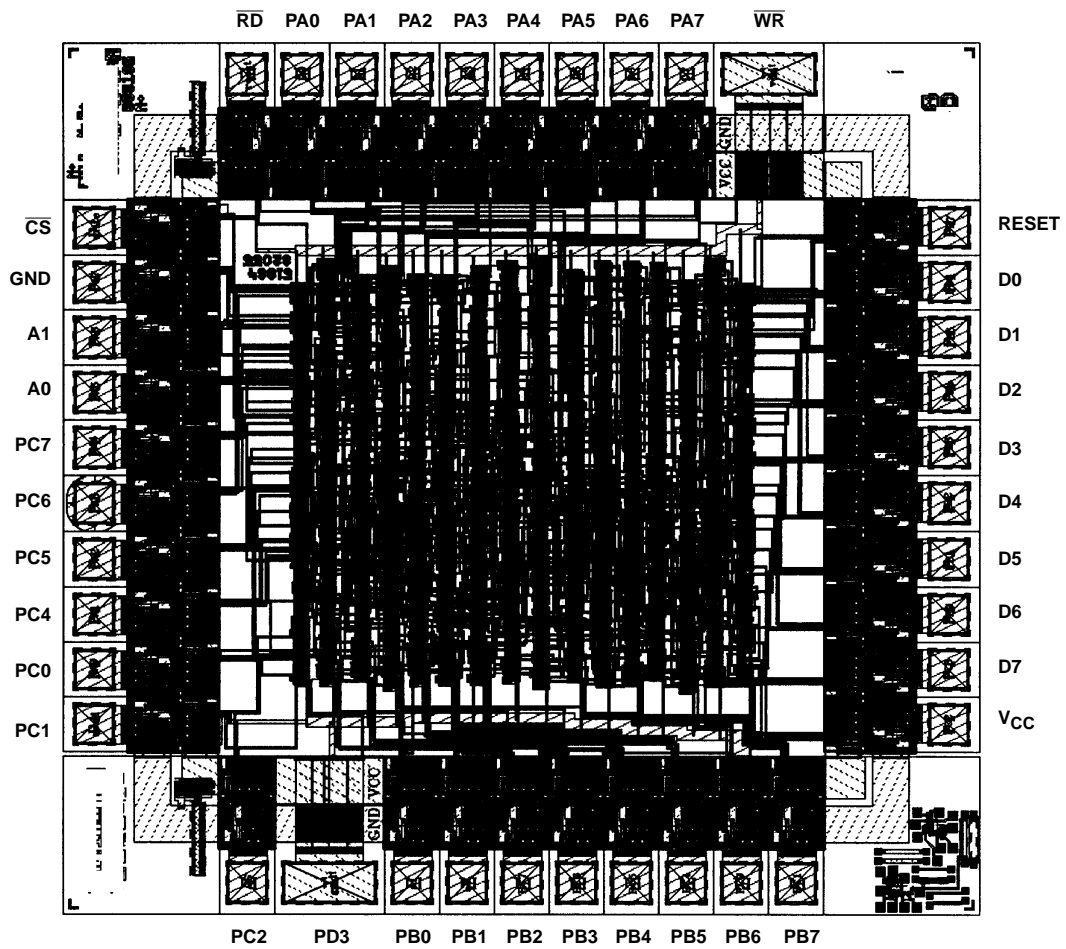| TEST CONDITION	V1	R1	R2	C1
1	1.7V	523Ω	Open	150pF
2	V_{CC}	2kΩ	1.7kΩ	50pF
3	1.5V	750Ω	Open	50pF

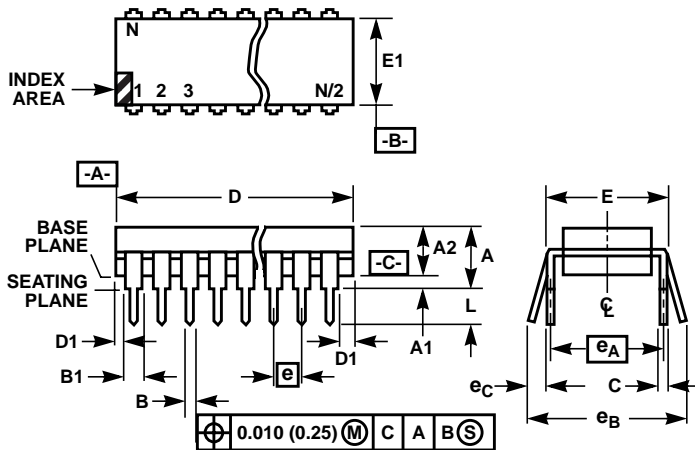## Burn-In Circuits

WS82C55A-5 DIP40L

NOTES:
1. V_{CC} = 5.5V ± 0.5V
2. VIH = 4.5V ± 10%
3. VIL = -0.2V to 0.4V
4. GND = 0V

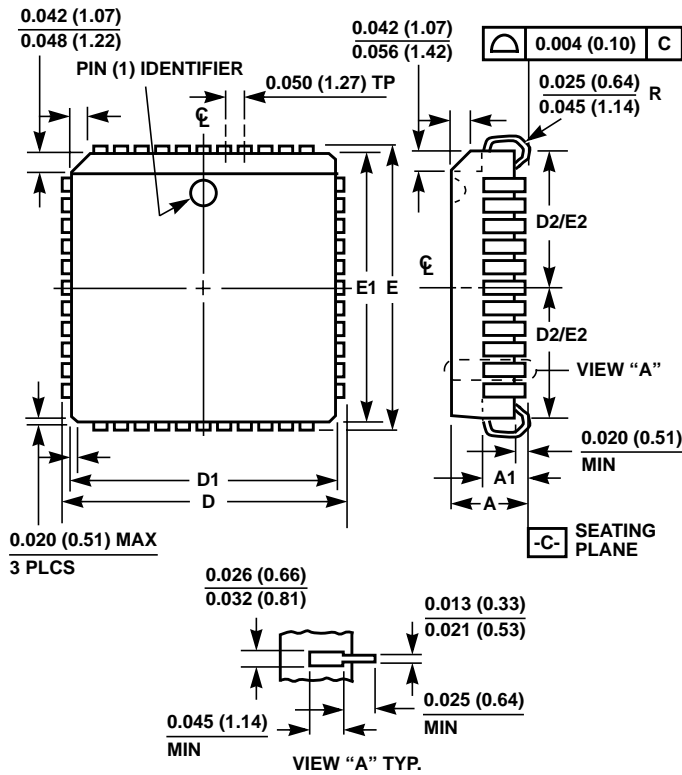## Die Characteristics

DIE SIZE

86x99 mils

Dual-In-Line Plastic Packages (PDIP)

E40.6 (JEDEC MS-011-AC ISSUE B)
40 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	NOTES
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.980	2.095	50.3	53.2	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	40		40		9

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NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.

2. Dimensioning and tolerancing per ANSI Y14.5M-1982.

3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.

4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.

5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).

6. E and e_A are measured with the leads constrained to be perpendicular to datum -C- .

7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.

8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).

9. N is the maximum number of terminal positions.

10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Plastic Leaded Chip Carrier Packages (PLCC)

N44.65 (JEDEC MS-018AC ISSUE A)
44 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

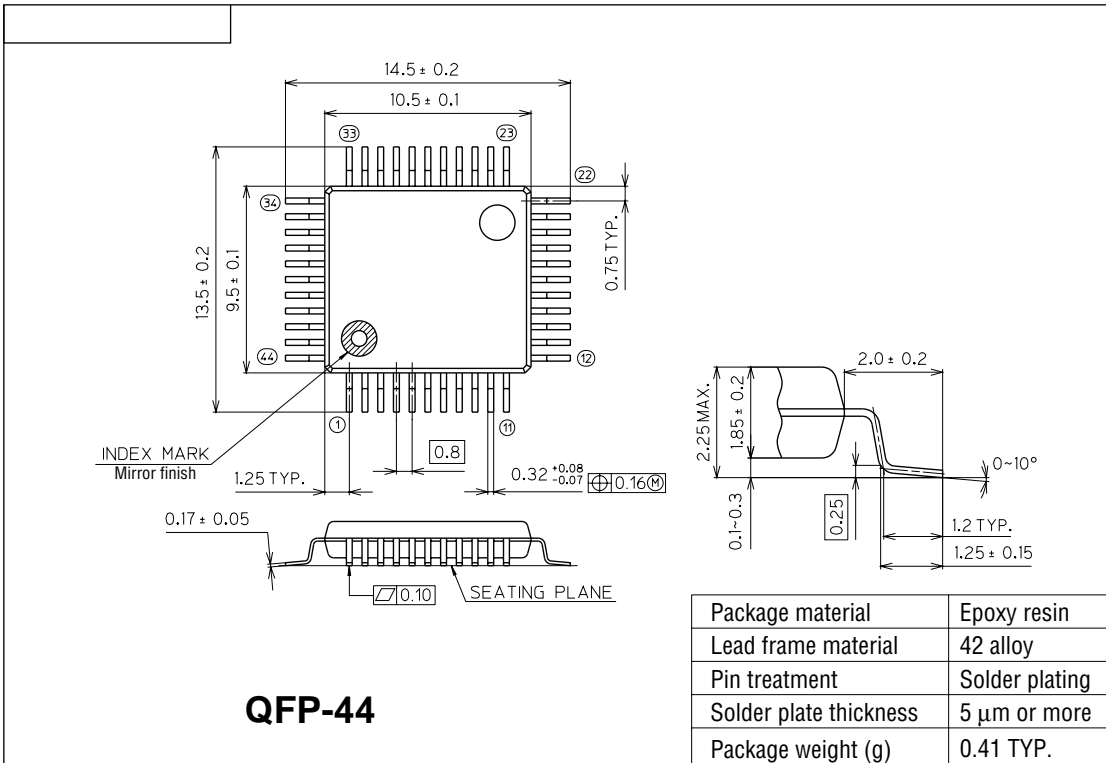| SYM-BOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.685	0.695	17.40	17.65	-
D1	0.650	0.656	16.51	16.66	3
D2	0.291	0.319	7.40	8.10	4, 5
E	0.685	0.695	17.40	17.65	-
E1	0.650	0.656	16.51	16.66	3
E2	0.291	0.319	7.40	8.10	4, 5
N	44		44		6

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NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.

2. Dimensions and tolerancing per ANSI Y14.5M-1982.

3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.

4. To be measured at seating plane -C- contact point.

5. Centerline to be determined where center leads exit plastic body.

6. "N" is the number of terminal positions.

(Unit : mm)

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.41 TYP.

QFP-44

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).