

82S23 82S123 256-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S23 and 82S123 are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S23 and 82S123 devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for memory expansion. They feature either Open collector or Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following pages.

The 82S23 and 82S123 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

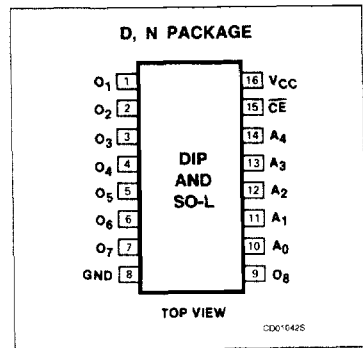
FEATURES

- Address access time: 50ns max
- Power dissipation: 1.3mW/bit typ
- Input loading: $-100\mu\text{A}$ max
- On-chip address decoding
- One chip enable input
- Output options:
 - N82S23: Open collector
 - N82S123: Three-state
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

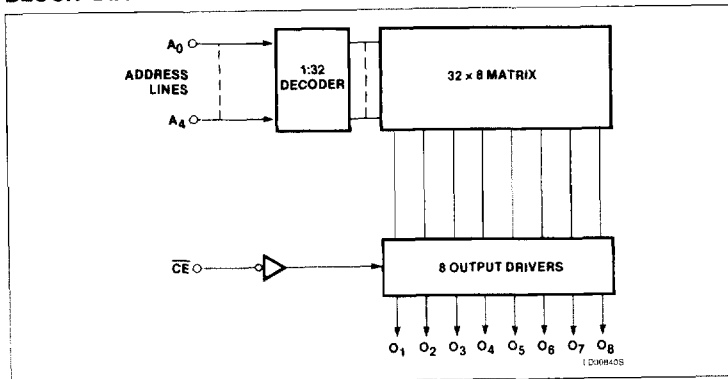
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Format conversion
- Hardwired algorithms
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



256-Bit TTL Bipolar PROM (32 x 8)

82S23, 82S123

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 16-pin	N82S23 N • N82S123 N
Plastic Small Outline 300mil wide 16-pin	N82S23 D • N82S123 D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
V _{OH} Output voltage High (82S23) V _O Off-state (82S123)	+5.5	V _{dc}
T _A Operating T _{STG} Storage	0 to +75 -65 to +150	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage V _{IL} Low V _{IH} High V _{IC} Clamp	V _{CC} = 4.75V V _{CC} = 5.25V I _{IN} = -12mA	2.0		0.8 -1.2	V
Output voltage V _{OL} Low V _{OH} High	\overline{CE} = Low I _{OUT} = 16mA I _{OUT} = -2mA	2.4		0.45	V
Input current I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 50	μA
Output current I _{OLK} Leakage (82S23) I _{OZ} Hi-Z State (82S123) I _{OS} Short circuit (82S123) ³	\overline{CE} = High, V _{OUT} = 5.5V \overline{CE} = High, V _{OUT} = 5.5V \overline{CE} = High, V _{OUT} = 0.5V \overline{CE} = Low, V _{OUT} = 0V, High stored			40 40 -40 -90	μA mA
Supply current I _{CC}	V _{CC} = 5.25V			96	mA
Capacitance C _{IN} Input C _{OUT} Output	\overline{CE} = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

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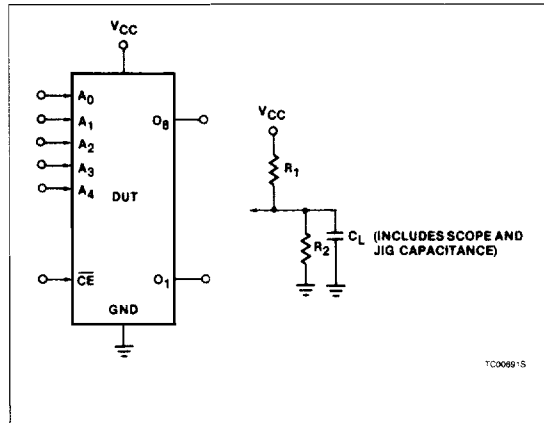
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ⁵	Max	
Access time⁴ T_{AA} T_{CE}	Output Output	Address Chip enable		45	50	ns
					35	
Disable time⁶ T_{CD}	Output	Chip enable			35	ns

NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground terminal.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μ sec.
5. Typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM

