National Semiconductor

PRELIMINARY

NMC9802 2048-Bit Parallel (256 x 8) Electrically Erasable Programmable ROM

General Description

The NMC9802 is a 2048 bit electrically erasable programmable read-only memory (E^2PROM) organized as 256 words by eight bits. Fabricated using National's double poly silicon gate n-channel technology, the device utilizes a novel memory architecture that results in the memory operating as a non-volatile register file. A single bidirectional eight bit data port is used for transmitting the address, data and status information. Both address and input data are latched into onboard registers elminating the need to hold them valid during the long erase/write operation. In addition, all the erase/write control logic is incorporated on chip completely freeing the microprocessor once the erase/write cycle has been initiated. Both a $\overline{BUSY}$ signal and status register are available to facilitate easy interface in a wide variety of microprocessor based systems.

The in-system erase/write capability of the NMC9802 make it suitable for a wide variety of applications requiring a small amount of alterable non-volatile storage. Any byte can be erased and written without affecting the rest of memory. Alternatively, the entire memory can be erased.

The NMC9802 utilizes fully static circuitry and is completely TTL compatible in the read and erase/write modes. The device has an on-chip voltage generator eliminating the need for any high voltage pulses or power supplies. The single +5V power supply is all that is required for any operation. The NMC9802 can be a direct replacement for Synertek's SY2802E.

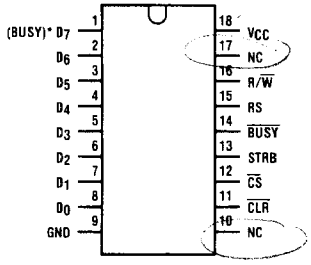
Features

- Reliable E^2 floating gate technology
- Microprocessor compatible architecture
- On-chip address/data latches
- Single cycle byte erase/write capability
- Fully TTL compatible
- Endurance 1 x 10^4 write cycles (Min.)
- Single +5V operation
- Erase/write specifications guaranteed 0–70°C
- On-chip ERASE/WRITE timing and control
- Both $\overline{BUSY}$ signal and status register
- Data retention: 10 years (Min.)

020663

Connection and Block Diagrams

Dual In-Line Package

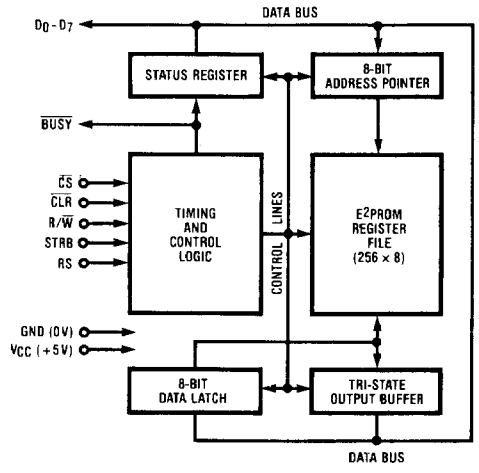


TL/D/8348–1

Top View

*SEE STATUS REGISTER

See Ordering Information



TL/D/8348–2

1-38

Absolute Maximum Ratings

Temperature Under Bias	−10°C to +80°
Storage Temperature	−65°C to 125°
Voltage on Any Pin with Respect to Ground	−0.5V to +7V

Comment

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Characteristics T_A = 0°C to 70°C, V_{CC} = +5V ±10% (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}			10	μA
I_{LO}	Output Leakage Current	V_{IN} = GND to V_{CC}			10	μA
I_{CC}	V_{CC} Current	Outputs Open			80	mA
V_{IL}	Input LOW Voltage		−0.3		0.8	V
V_{IH}	Input HIGH Voltage		2.0		V_{CC} +1	V
V_{OL}	Output LOW Voltage	I_{OL} = 3.2 mA			0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = −1.0 mA	2.4			V

Capacitance T_A = 25°C, f = 1.0 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note: This parameter is periodically sampled and not 100% tested.

AC Electrical Characteristics T_A = 0°C to 70°C, V_{CC} = +5V ±10% (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{CYC}	Cycle Time		350			ns
t_{CS}	Chip Select Access Time				120	ns
t_{SA}	Valid Data from Strobe				450	ns
t_{LZ}	Select to Output LOW Z		10			ns
t_{HZ}	Select to Output HIGH Z	(Note 2)	10		75	ns
t_{AR}	Access Time from RS or R/$\overline{W}$				200	ns
t_{WS}	Write Setup Time		120			ns
t_{WH}	Write Hold Time		0			ns
t_{DS}	Data Setup Time		60			ns
t_{DH}	Data Hold Time		0			ns
t_{SH}	Strobe Pulse Width High		85			ns
t_{SL}	Strobe Pulse Width Low		120			ns
t_{BA}	$\overline{BUSY}$ Active From Strobe		30		300	ns
t_{BLW}	$\overline{BUSY}$ Low Pulse Width (WRITE)				25	ms
t_{SCY}	Busy HIGH to Cycle Start		0			ns
t_{BLC}	$\overline{BUSY}$ Low Pulse Width (CLEAR)				12.5	ms

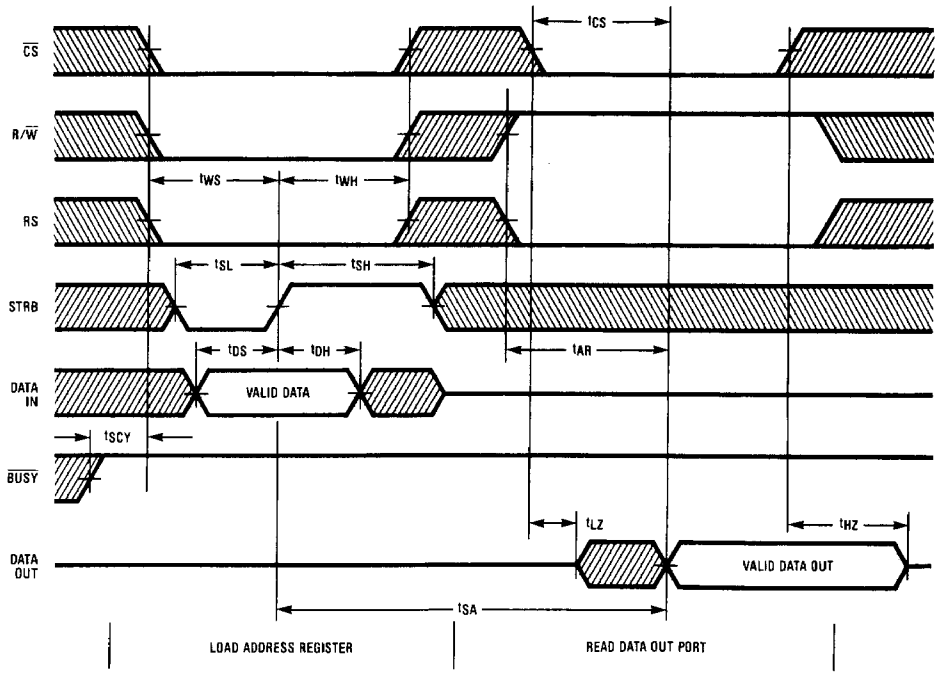
Note 1: A minimum 0.5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

Note 2: Current goes through 50% change from I_{OH} (MAX) or I_{OL} (MAX).

Note 3: Pins 11 and 16 must be held below V_{CC} during power up.

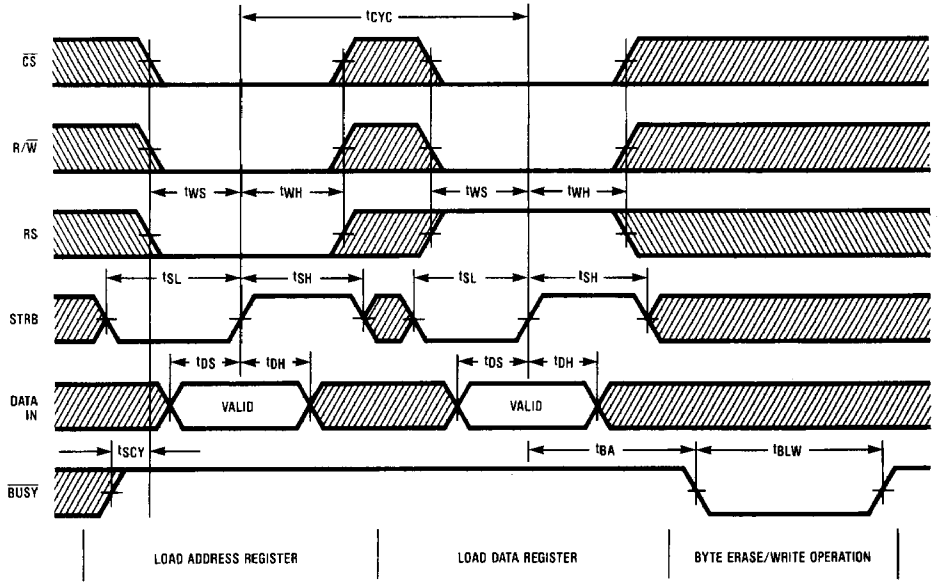
Timing Diagrams

Data Fetch ($\overline{CLR}$ = HIGH, $\overline{BUSY}$ = HIGH) (Note 1)



TL/D/8348–3

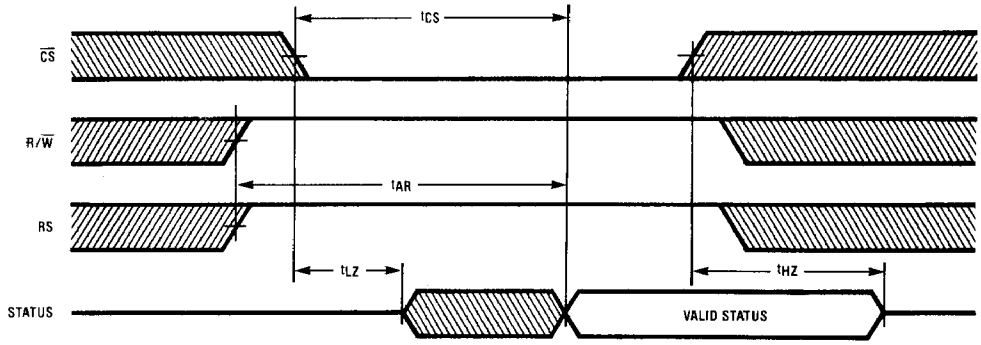
Data Store ($\overline{CLR}$ = HIGH) (Note 1)



TL/D/8348–4

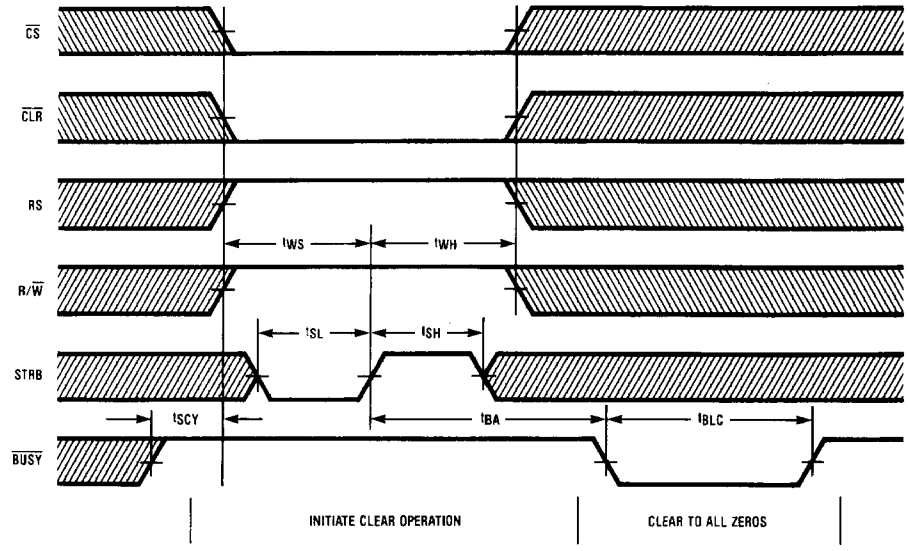
Timing Diagram (Continued)

Read Status Register ($\overline{CLR}$ = HIGH, $\overline{BUSY}$ = Don't Care) (Note 1)



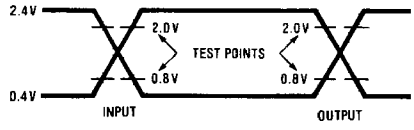
TL/D/8348–5

Clear Cycle (Data = Don't Care) (Note 1)



TL/D/8348–6

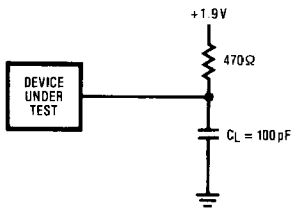
A.C. Testing Input, Output Waveform



AC TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.4V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0". INPUT PULSE RISE AND FALL TIMES ARE 5ns.

TL/D/8348–7

A.C. Testing Load Circuit



C_L INCLUDES SCOPE AND JIG CAPACITANCE

TL/D/8348–8

DEVICE OPERATION

The NMC9802 has seven modes of operation as listed in Table I. All the modes of the NMC9802 involve reading or loading registers. This eliminates any timing problems associated with interfacing to a wide variety of microprocessors and microcomputers.

DATA FETCH

Reading the NMC9802 involves two cycles as shown in the timing diagram. First the address pointer is loaded and then the data from the selected location can be read. Both the address and data are transmitted through the same eight bit port.

DATA STORE

Writing the device requires two cycles as shown in the timing diagram. As with the read operation, first the address pointer must be loaded. Loading the data input register then initiates the byte erase/write operation and the microprocessor is free to do other tasks. The timing interface with the microprocessor is handled with both a $\overline{BUSY}$ signal and a status register. Loading the data in register causes the open-drain $\overline{BUSY}$ signal to be set LOW and bit seven (pin 1) of the status register to be set HIGH for the duration of the byte erase/write operation. Once complete, these two signals are reset to their inactive states. Note that it is not necessary for the microprocessor to erase the location prior to writing new data. This is automatically done by the memory itself.

Once the erase/write operation has been initiated, the NMC9802 doesn't allow access to address pointer, data input register or data output drivers.

READ STATUS REGISTER

To facilitate interfacing the NMC9802 in microprocessor based systems, a status register has been provided that is accessible at all times including during the erase/write operation. This allows a polling routine to be used to determine if the NMC9802 is busy. If bit 7 (pin 1) is a logic "1", the device is in the erase/write operation and if it is a logic "0" it is available for normal operation.

CLEAR CYCLE

The NMC9802 can be block cleared to all zeros as shown in the timing diagram. As with the data store operation, this cycle only needs to be initiated, all the timing is controlled internally. On initiating the clear cycle, $\overline{BUSY}$ and bit 7 (pin 1) are set active and remain so until the operation is complete. During the clear cycle, only the status register is accessible.

ENDURANCE CHARACTERISTIC

A characteristic of E^2PROMs is that the number of erase/write cycles is limited. The NMC9802 has been designed to meet applications where up to 1×10^4 erase/write cycles per word are required. The erase/write cycling is completely word independent. Adjacent words are not affected during the erase/write cycling.

TABLE I. Mode Selection $V_{CC} = +5V$ (Note 1)

Mode	Pin						Data Input/ Outputs (0-7)
	$\overline{CS}$ (12)	R/$\overline{W}$ (16)	RS (15)	STRB (13)	$\overline{BUSY}$ (14)	$\overline{CLR}$ (11)	
Read Register File	0	1	0	X	1	1	Data Out
Read Status Register	0	1	1	X	X	1	Data Out
Write Address Pointer	0	0	0	↗	1	1	Data In
Write Data-In Latch	0	0	1	↗	⊓	1	Data In
Deselected	1	X	X	X	X	X	High Z
Write Inhibited	X	X	0	0	1	X	X
Block Clear	0	1	1	↗	⊓	0	High Z

X = DON'T CARE

↗ = POSITIVE TRANSITION

⊓ = NEGATIVE PULSE

Ordering Information

Order Number	Select Access Time	Cycle Time (Min)	Supply Current (Max)	Package Type
NMC9802J	120 ns	350	70 mA	Cerdip
NMC9802N	120 ns	350	70 mA	Plastic