

---

## *10-Bit Serial Input Latched Source Driver*

---

### **Discontinued Product**

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: November 1, 2010

#### **Recommended Substitutions:**

*For existing customer transition, and for new customers or new applications, contact Allegro Sales.*

---

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

---

*Allegro MicroSystems, Inc. reserves the right to make, from time to time, revisions to the anticipated product life cycle plan for a product to accommodate changes in production capabilities, alternative product availabilities, or market demand. The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringements of patents or other rights of third parties which may result from its use.*

---

## 10-Bit Serial Input Latched Source Driver

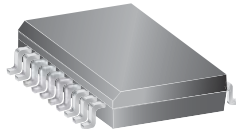
### Features and Benefits

- Controlled output slew rate
- High-speed data storage
- 60 V minimum output breakdown
- High data-input rate
- PNP active pull-downs
- Low output-saturation voltages
- Low-power CMOS logic and latches
- Improved replacements for TL4810x, UCN5810x, and UCQ5810x

### Packages:



18-pin DIP  
(A package)



20-pin SOICW  
(LW package)

Not to scale

### Description

The A6810 combines 10-bit CMOS shift registers, accompanying data latches, and control circuitry with bipolar sourcing outputs and PNP active pull-downs. Designed primarily to drive vacuum-fluorescent (VF) displays, the 60 V and -40 mA output ratings also allow this device to be used in many other peripheral power driver applications. The A6810 features an increased data input rate (compared with the older UCN/UCQ5810-F) and a controlled output slew rate.

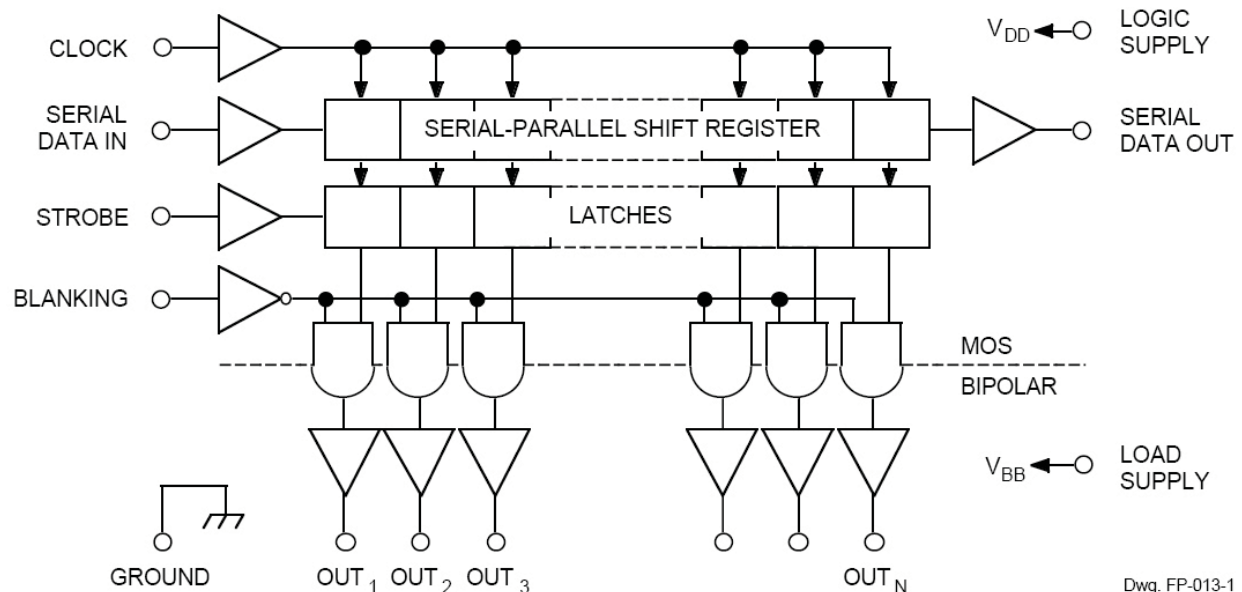
The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. With a 3.3 or 5 V logic supply, serial data-input rates of at least 10 MHz can be attained

A CMOS serial data output permits cascaded connections in applications requiring additional drive lines. Similar devices are available as the A6812 (20-bit) and A6818 (32-bit).

The A6810 output source drivers are NPN Darlingtontons, capable of sourcing up to 40 mA. The controlled output slew rate reduces electromagnetic noise, which is an important consideration in systems that include telecommunications and microprocessors, and to meet government emissions regulations. For inter-digit

Continued on the next page...

### Functional Block Diagram



Dwg. FP-013-1

## Description (continued)

blanking, all output drivers can be disabled and all sink drivers turned on with a BLANKING input high. The PNP active pull-downs can sink at least 2.5 mA.

The A6810 is available in three temperature ranges for optimum performance in commercial (S), industrial (E), and automotive (K) applications. It is provided in two package styles, through-hole

DIP (package A) and surface-mount SOIC (package LW). Copper leadframes, low logic-power dissipation, and low output-saturation voltages allow all devices to source 25 mA from all outputs continuously over the full operating temperature range.

The lead (Pb) free versions have 100% matte tin leadframe plating.

Selection Guide				
Part Number	Pb-free	Packing	Ambient Temperature, T <sub>A</sub> (°C)	Package
A6810EA-T	Yes	21 pieces/tube	-40 to 85	18-pin DIP
A6810SA-T	Yes	21 pieces/tube	-20 to 85	
A6810ELWTR-T	Yes	1000 pieces/13-in. reel	-40 to 85	20-pin SOIC-W
A6810KLWTR-T	Yes	1000 pieces/13-in. reel	-40 to 125	
A6810SLWTR-T	Yes	1000 pieces/13-in. reel	-20 to 85	

\*Variant is in production but has been determined to be LAST TIME BUY. This classification indicates that the variant is obsolete and notice has been given. Sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change May 3, 2010. Deadline for receipt of LAST TIME BUY orders is October 29, 2010.

## Absolute Maximum Ratings\*

Characteristic	Symbol	Notes	Rating	Units
Logic Supply Voltage	V <sub>DD</sub>		7.0	V
Driver Supply Voltage	V <sub>BB</sub>		60	V
Input Voltage Range	V <sub>IN</sub>		-0.3 to V <sub>DD</sub> + 0.3	V
Continuous Output Current Range	I <sub>OUT</sub>		-40 to 15	mA
Operating Ambient Temperature	T <sub>A</sub>	Range E	-40 to 85	°C
		Range K	-40 to 125	°C
		Range S	-20 to 85	°C
Maximum Junction Temperature	T <sub>J(max)</sub>		150	°C
Storage Temperature	T <sub>stg</sub>		-55 to 125	°C

\*Caution: These CMOS devices have input static protection (Class 2) but are still susceptible to damage if exposed to extremely high static electrical charges.



ELECTRICAL CHARACTERISTICS at  $T_A = +25^\circ\text{C}$  (A6810S-) or over operating temperature range (A6810E-),  $V_{BB} = 60\text{ V}$ , logic supply operating voltage  $V_{DD} = 3.0\text{ to }5.5\text{ V}$ ; unless otherwise noted

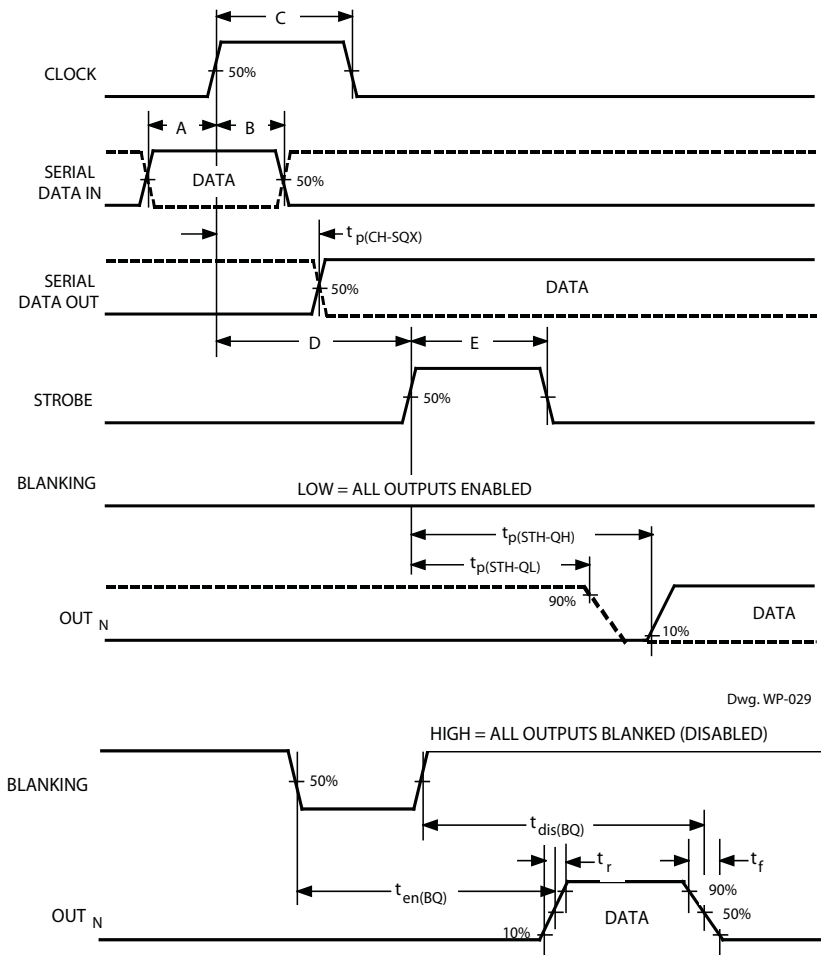
Characteristic	Symbol	Test Conditions	Limits @ $V_{DD} = 3.3\text{ V}$			Limits @ $V_{DD} = 5\text{ V}$			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	$I_{CEX}$	$V_{OUT} = 0\text{ V}$	—	<-0.1	-15	—	<-0.1	-15	$\mu\text{A}$
Output Voltage	$V_{OUT(1)}$	$I_{OUT} = -25\text{ mA}$	57.5	58.3	—	57.5	58.3	—	V
	$V_{OUT(0)}$	$I_{OUT} = 1\text{ mA}$	—	1.0	1.5	—	1.0	1.5	V
Output Pull-Down Current	$I_{OUT(0)}$	$V_{OUT} = 5\text{ V to }V_{BB}$	2.5	5.0	—	2.5	5.0	—	mA
Input Voltage	$V_{IN(1)}$		2.2	—	—	3.3	—	—	V
	$V_{IN(0)}$		—	—	1.1	—	—	1.7	V
Input Current	$I_{IN(1)}$	$V_{IN} = V_{DD}$	—	<0.01	1.0	—	<0.01	1.0	$\mu\text{A}$
	$I_{IN(0)}$	$V_{IN} = 0\text{ V}$	—	<-0.01	-1.0	—	<-0.01	-1.0	$\mu\text{A}$
Input Clamp Voltage	$V_{IK}$	$I_{IN} = -200\text{ }\mu\text{A}$	—	-0.8	-1.5	—	-0.8	-1.5	V
Serial Data Output Voltage	$V_{OUT(1)}$	$I_{OUT} = -200\text{ }\mu\text{A}$	2.8	3.05	—	4.5	4.75	—	V
	$V_{OUT(0)}$	$I_{OUT} = 200\text{ }\mu\text{A}$	—	0.15	0.3	—	0.15	0.3	V
Maximum Clock Frequency	$f_c$		10*	—	—	10*	—	—	MHz
Logic Supply Current	$I_{DD(1)}$	All Outputs High	—	0.25	0.75	—	0.3	1.0	mA
	$I_{DD(0)}$	All Outputs Low	—	0.25	0.75	—	0.3	1.0	mA
Load Supply Current	$I_{BB(1)}$	All Outputs High, No Load	—	1.5	3.0	—	1.5	3.0	mA
	$I_{BB(0)}$	All Outputs Low	—	0.2	20	—	0.2	20	$\mu\text{A}$
Blanking-to-Output Delay	$t_{dis(BQ)}$	$C_L = 30\text{ pF}$ , 50% to 50%	—	0.7	2.0	—	0.7	2.0	$\mu\text{s}$
	$t_{en(BQ)}$	$C_L = 30\text{ pF}$ , 50% to 50%	—	1.8	3.0	—	1.8	3.0	$\mu\text{s}$
Strobe-to-Output Delay	$t_{p(STH-QL)}$	$R_L = 2.3\text{ k}\Omega$ , $C_L \leq 30\text{ pF}$	—	0.7	2.0	—	0.7	2.0	$\mu\text{s}$
	$t_{p(STH-QH)}$	$R_L = 2.3\text{ k}\Omega$ , $C_L \leq 30\text{ pF}$	—	1.8	3.0	—	1.8	3.0	$\mu\text{s}$
Output Fall Time	$t_f$	$R_L = 2.3\text{ k}\Omega$ , $C_L \leq 30\text{ pF}$	2.4	—	12	2.4	—	12	$\mu\text{s}$
Output Rise Time	$t_r$	$R_L = 2.3\text{ k}\Omega$ , $C_L \leq 30\text{ pF}$	2.4	—	12	2.4	—	12	$\mu\text{s}$
Output Slew Rate	dV/dt	$R_L = 2.3\text{ k}\Omega$ , $C_L \leq 30\text{ pF}$	4.0	—	20	4.0	—	20	V/ $\mu\text{s}$
Clock-to-Serial Data Out Delay	$t_{p(CH-SQX)}$	$I_{OUT} = \pm 200\text{ }\mu\text{A}$	—	50	—	—	50	—	ns

Negative current is defined as coming out of (sourcing) the specified device terminal.

Typical data is for design information only and is at  $T_A = +25^\circ\text{C}$ .

\*Operation at a clock frequency greater than the specified minimum value is possible but not warranted.

**TIMING REQUIREMENTS and SPECIFICATIONS**  
(Logic Levels are  $V_{DD}$  and Ground)



Dwg. WP-029

Dwg. WP-030A

- A.** Data Active Time Before Clock Pulse  
(Data Set-Up Time),  $t_{su(D)}$  ..... **25 ns**
- B.** Data Active Time After Clock Pulse  
(Data Hold Time),  $t_{h(D)}$  ..... **25 ns**
- C.** Clock Pulse Width,  $t_{w(CH)}$  ..... **50 ns**
- D.** Time Between Clock Activation and Strobe,  $t_{su(C)}$  ..... **100 ns**
- E.** Strobe Pulse Width,  $t_{w(STH)}$  ..... **50 ns**

NOTE – Timing is representative of a 10 MHz clock. Higher speeds may be attainable; operation at high temperatures will reduce the specified maximum clock frequency.

Serial Data present at the input is transferred to the shift register on the logic “0” to logic “1” transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The

SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

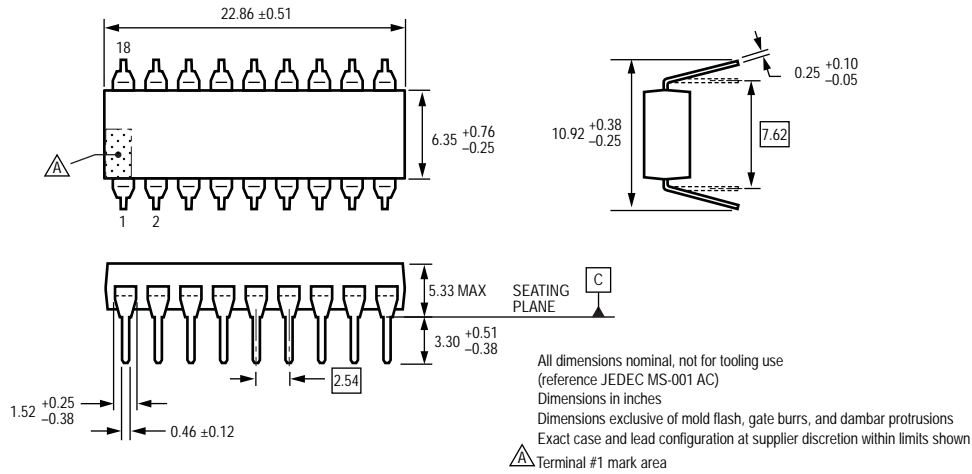
When the BLANKING input is high, the output source drivers are disabled (OFF); the PNP active pull-down sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

**TRUTH TABLE**

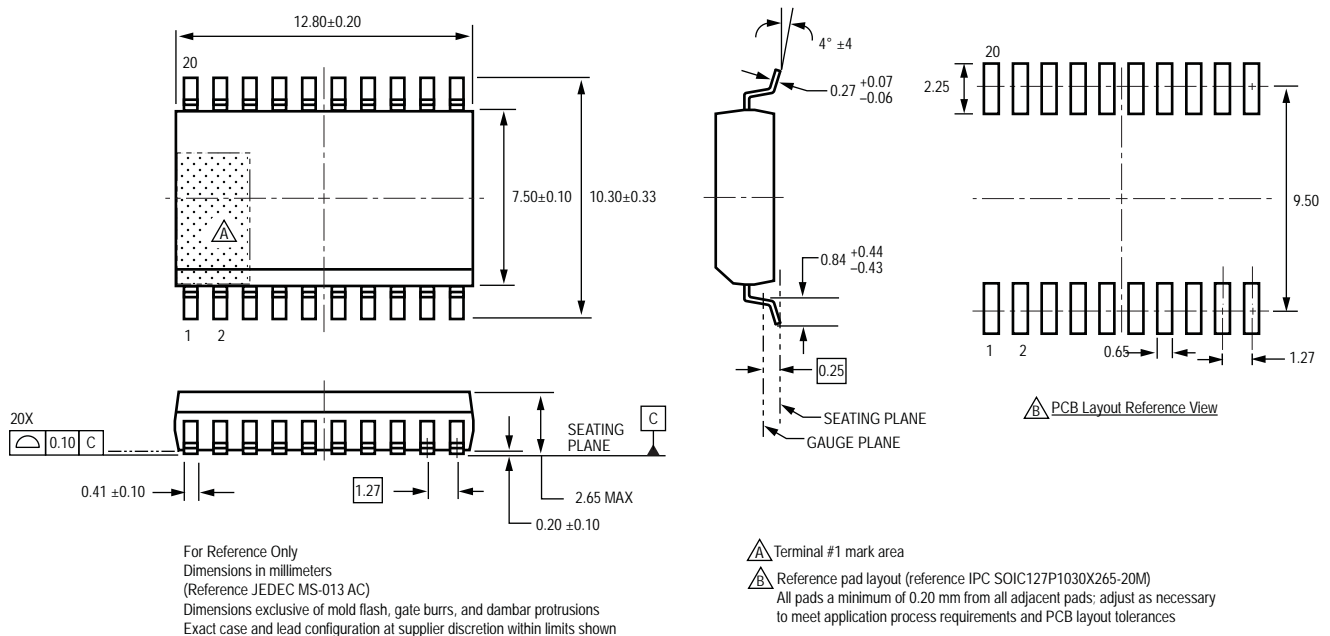
Serial Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe Input	Latch Contents						Output Contents						
		I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	...	I <sub>N-1</sub>	I <sub>N</sub>			I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	...	I <sub>N-1</sub>	I <sub>N</sub>	Blanking	I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	...	I <sub>N-1</sub>	I <sub>N</sub>
H		H	R <sub>1</sub>	R <sub>2</sub>	...	R <sub>N-2</sub>	R <sub>N-1</sub>	R <sub>N-1</sub>														
L		L	R <sub>1</sub>	R <sub>2</sub>	...	R <sub>N-2</sub>	R <sub>N-1</sub>	R <sub>N-1</sub>														
X		R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	...	R <sub>N-1</sub>	R <sub>N</sub>	R <sub>N</sub>														
		X	X	X	...	X	X	X	L	R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	...	R <sub>N-1</sub>	R <sub>N</sub>							
		P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	...	P <sub>N-1</sub>	P <sub>N</sub>	P <sub>N</sub>	H	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	...	P <sub>N-1</sub>	P <sub>N</sub>	L	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	...	P <sub>N-1</sub>	P <sub>N</sub>
										X	X	X	...	X	X	H	L	L	L	...	L	L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

Package A 18-Pin DIP



Package LW 20-Pin SOICW





Copyright ©1998-2010, Allegro MicroSystems, Inc.

The products described here are manufactured under one or more U.S. patents or U.S. patents pending.

Allegro MicroSystems, Inc. reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro's products are not to be used in life support devices or systems, if a failure of an Allegro product can reasonably be expected to cause the failure of that life support device or system, or to affect the safety or effectiveness of that device or system.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

For the latest version of this document, visit our website:

[www.allegromicro.com](http://www.allegromicro.com)

