

**DUAL 2-BIT BINARY TO 4-LINE DECODER/DEMULTIPLEXER
WITH OPEN COLLECTOR OUTPUT****DESCRIPTION**

The M74LS156P is a semiconductor integrated circuit containing two 2-bit binary to 4-line decoders/demultiplexers with open collector outputs.

FEATURES

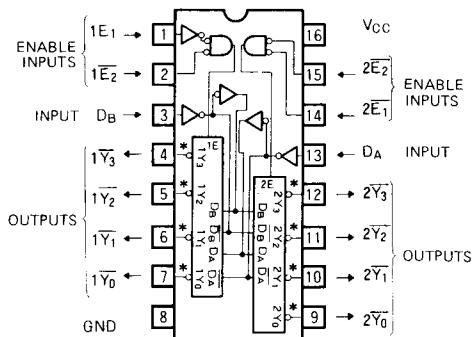
- Usable in AND Tie connection
- Enable inputs provided
- 8-bit output decoder/demultiplexer function is provided without the use of external components
- Wide operating temperature range ($T_a = -20 \sim +75^\circ C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

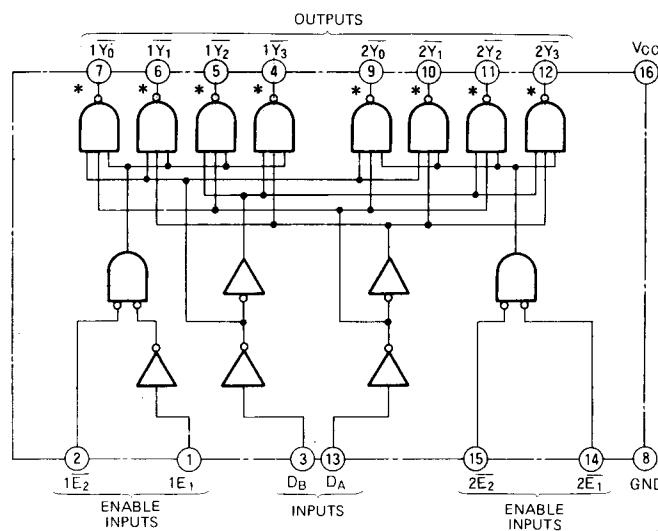
When a 2-bit binary number is decoded as a quaternary number and the 2-bit binary number is applied to inputs D_A and D_B , the corresponding $\bar{Y}_0 \sim \bar{Y}_3$ output is set low and all the other 3 outputs are set high. In this case, enable inputs $1E_1$ and $2E_1$ are kept high and low, respectively, and enable inputs $1E_2$ and $2E_2$ are kept low. When $1E_2$ and $2E_2$ are set high, all the outputs are set high. When decoding a 3-bit binary number in octal numbers, $1E_1$ and $2E_2$ are connected and by applying the third bit binary number to them, the outputs appear in $2\bar{Y}_0 \sim 2\bar{Y}_3$ and $1\bar{Y}_0 \sim 1\bar{Y}_3$, in accordance with the function table.

PIN CONFIGURATION (TOP VIEW)

Outline 16P4

For use as a 1-line to 4-line demultiplexer, the outputs appear in $\bar{Y}_0 \sim \bar{Y}_3$ by making $1E_1$ and $2E_1$ the data inputs and D_A and D_B the selection inputs. For use as a 1-line to 8-line demultiplexer, $1E_1$ and $1E_2$ are connected to be made the third bit selection input and $1E_2$ and $2E_2$ are connected to be made the data inputs so that the outputs appear in $2\bar{Y}_0 \sim 2\bar{Y}_3$ and $1\bar{Y}_0 \sim 1\bar{Y}_3$.

M74LS156P has the same functions and pin connections as M74LS155P but the latter is provided with active pull-up resistor outputs.

BLOCK DIAGRAM

* OPEN COLLECTOR OUTPUT

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FUNCTION TABLE (Note 1)

(2-bit binary to 4-line decoder/1 line
to 4-line demultiplexer)

D _B	D _A	1E ₂	1E ₁	Y ₀	Y ₁	Y ₂	Y ₃
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

D _B	D _A	2E ₂	2E ₁	2Y ₀	2Y ₁	2Y ₂	2Y ₃
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

(3-bit binary to 8-line decoder/1 line
to 8 line demultiplexer)

D _C	D _B	D _A	E	2Y ₀	2Y ₁	2Y ₂	2Y ₃	1Y ₀	1Y ₁	1Y ₂	1Y ₃
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	H	L	L	H	H	H	H	H	L	H	H
H	H	H	L	H	H	H	H	H	H	L	H

Note 1 X : Irrelevant

D_C : Pin connecting 1E₁ and 2E₁

E : Pin connecting 1E₂ and 2E₂

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions			Limits	Unit
		Min	Typ	Max		
V _{CC}	Supply voltage				-0.5 ~ +7	V
V _I	Input voltage				-0.5 ~ +15	V
V _O	Output voltage	High-level state			-0.5 ~ V _{CC}	V
T _{opr}	Operating free-air ambient temperature range				-20 ~ +75	°C
T _{stg}	Storage temperature range				-65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V _{CC}	Supply voltage	4.75	5	5.25	V
I _{OH}	High-level output current	V _O =5.5V	0	100	μA
I _{OL}	Low-level output current	V _{OL} ≤0.4V	0	4	mA
		V _{OL} ≤0.5V	0	8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Unit
		Min	Typ	Max	Min	Typ	Max	
V _{IH}	High-level input voltage				2			V
V _{IL}	Low-level input voltage						0.8	V
V _{IC}	Input clamp voltage	V _{CC} =4.75V, I _{IC} =-18mA					-1.5	V
I _{OH}	High-level output current	V _{CC} =4.75V, V _I =0.8V V _I =2V, V _O =5.5V					100	μA
V _{OL}	Low-level output voltage	V _{CC} =4.75V V _I =0.8V, V _I =2V		I _{OL} =4mA	0.25	0.4	V	
		V _{CC} =4.75V V _I =0.8V, V _I =2V		I _{OL} =8mA	0.35	0.5	V	
I _{IH}	High-level input current	V _{CC} =5.25V, V _I =2.7V					20	μA
I _{IL}	Low-level input current	V _{CC} =5.25V, V _I =10V					0.1	mA
I _{CC}	Supply current	V _{CC} =5.25V (Note 2)					-0.4	mA
		V _{CC} =5.25V (Note 2)			6.1	10		

* : All typical values are at $V_{CC}=5\text{V}$, $T_a=25^\circ\text{C}$.

Note 2: I_{CC} is measured with inputs 1E₂, 2E₁ and 2E₂ at 0V and with D_A, D_B and 1E₁ at 4.5V

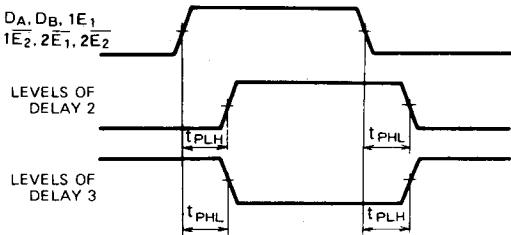
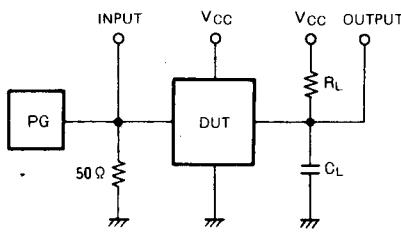
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WITH OPEN COLLECTOR OUTPUT

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_A, D_B to outputs $\bar{Y}_0 \sim \bar{Y}_3$	delay gate stages 2			18	ns
t_{PHL}	delay gate stages 3				18	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $1E_2, 2E_1, 2E_2$ to outputs $\bar{Y}_0 \sim \bar{Y}_3$	$R_L = 2k\Omega$ $C_L = 15pF$ (Note 3)			20	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $1E_1$ to outputs $1\bar{Y}_0 \sim 1\bar{Y}_3$				18	ns
t_{PHL}					16	ns
t_{PLH}					20	ns
t_{PHL}					20	ns
t_{PLH}					25	ns
t_{PHL}					48	ns

Note 3: Measurement circuit

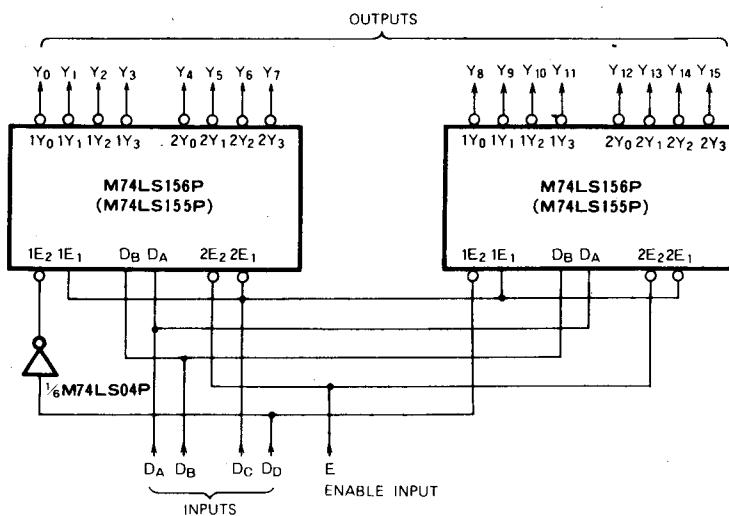
TIMING DIAGRAM (Reference level = 1.3V)



- (1) The pulse generator (PG) has the following characteristics:
 $PRR = 1MHz$, $t_r = 6ns$, $t_f = 6ns$, $t_w = 500ns$, $V_p = 3V_{PP}$, $Z_o = 50\Omega$.
- (2) C_L includes probe and jig capacitance

APPLICATION EXAMPLE

4-bit binary/hexadecimal decoder/demultiplexer



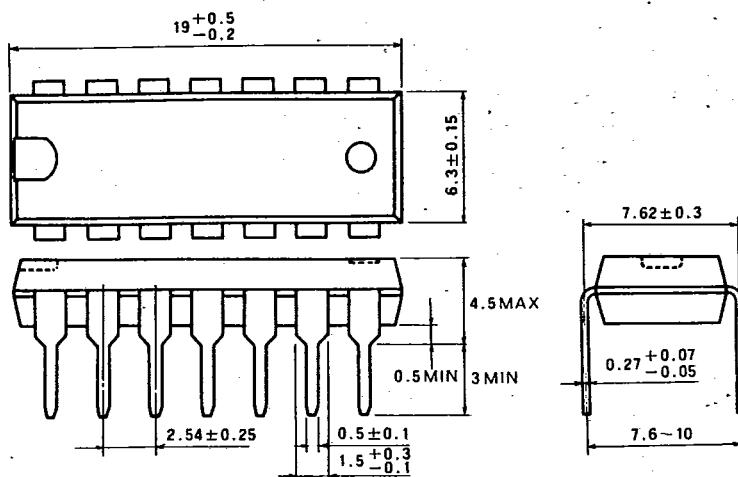
MITSUBISHI LSTTLs
PACKAGE OUTLINES

MITSUBISHI {DGTL LOGIC} 07E D 6249827 0013561 3

T-90-20

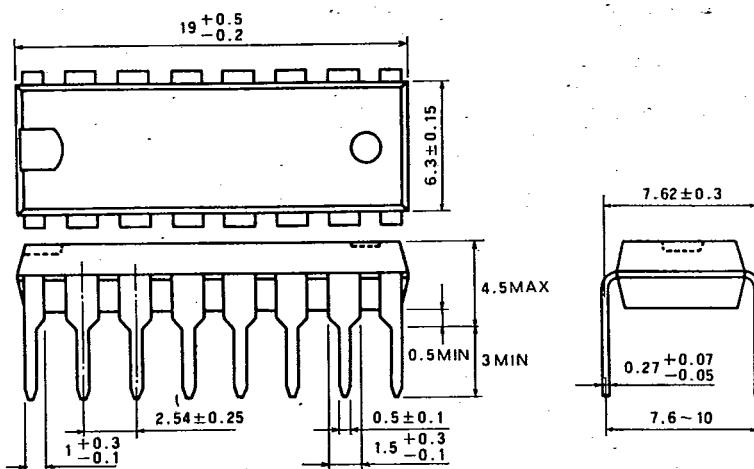
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm

