DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4521B
MSI
24-stage frequency divider and oscillator

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

DESCRIPTION

The HEF4521B consists of a chain of 24 toggle flip-flops with an overriding asynchronous master reset input (MR), and an input circuit that allows three modes of operation. The single inverting stage (I_2/O_2) will function as a crystal oscillator, or in combination with I_1 as an RC oscillator, or as an input buffer for an external oscillator. Low-power operation as a crystal oscillator is enabled by connecting external resistors to pins 3 (V_{SS}') and 5 (V_{DD}').

Each flip-flop divides the frequency of the previous flip-flop by two, consequently the HEF4521B will count up to 2^{24} = 16777216. The counting advances on the HIGH to LOW transition of the clock (I_2). The outputs of the last seven stages are available for additional flexibility.

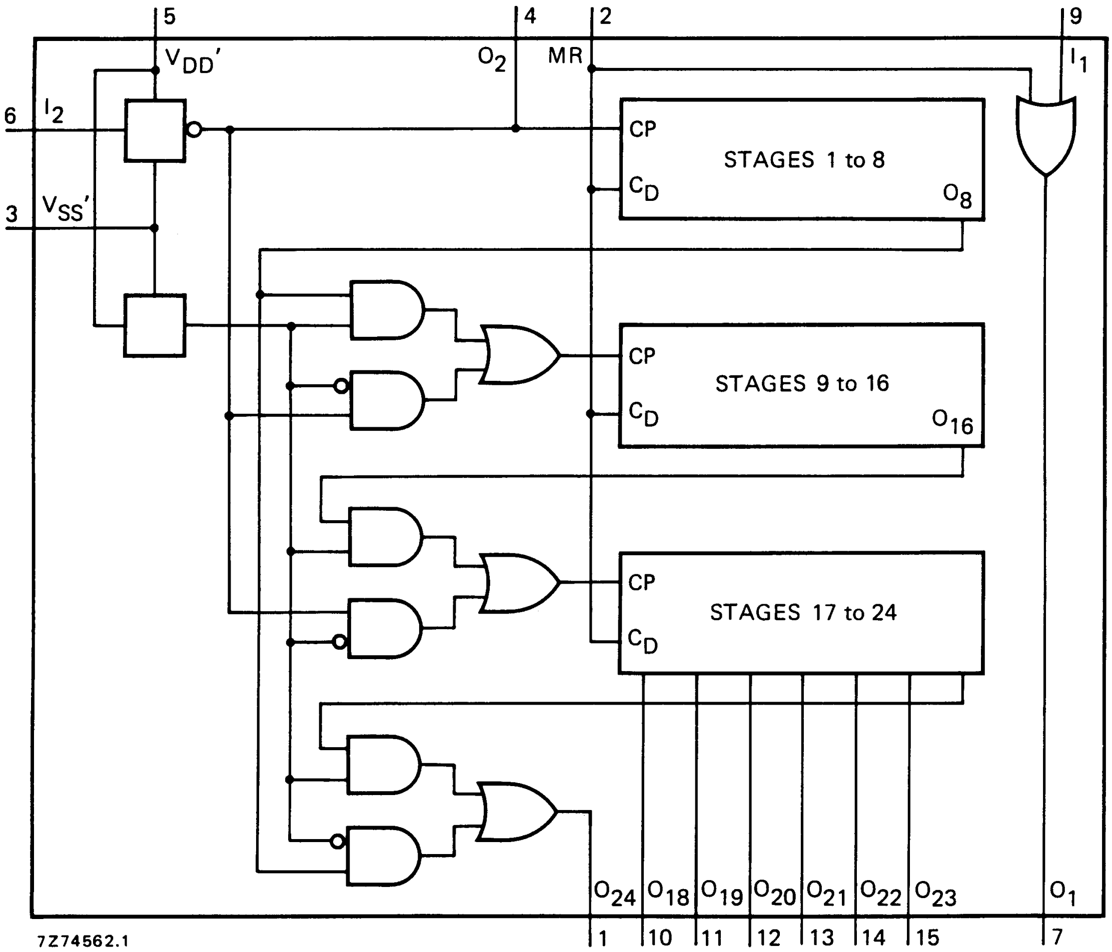


Fig.1 Functional diagram.

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

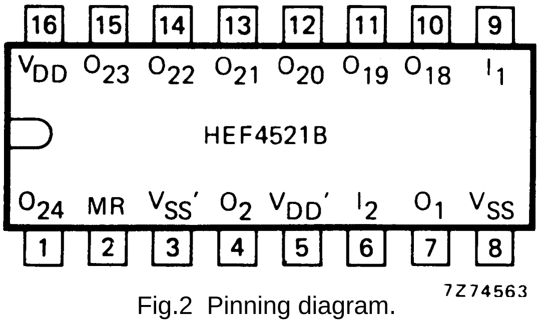


Fig.2 Pinning diagram.

COUNT CAPACITY

OUTPUT	COUNT CAPACITY
O_{18}	2^{18} = 262 144
O_{19}	2^{19} = 524 288
O_{20}	2^{20} = 1 048 576
O_{21}	2^{21} = 2 097 152
O_{22}	2^{22} = 4 194 304
O_{23}	2^{23} = 8 388 608
O_{24}	2^{24} = 16 777 216

HEF4521BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4521BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4521BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

FUNCTIONAL TEST SEQUENCE

INPUTS		CONTROL TERMINALS			OUTPUTS	REMARKS
MR	**I_2**	**O_2**	**V_{SS}'**	**V_{DD}'**	**O_{18} to O_{24}**	
H	L	L	V_{DD}	V_{SS}	L	counter is in three 8-stage sections in parallel mode; I_2 and O_2 are interconnected (O_2 is now input); counter is reset by MR
L	⎍	⎍	V_{DD}	V_{SS}	H	255 pulses are clocked into I_2, O_2 (the counter advances on the LOW to HIGH transition)
L	L	L	V_{SS}	V_{SS}	H	V_{SS}' is connected to V_{SS}
L	H	L	V_{SS}	V_{SS}	H	the input I_2 is made HIGH
L	H	L	V_{SS}	V_{DD}	H	V_{DD}' is connected to V_{DD}; O_2 is now made floating and becomes an output; the device is now in the 2^{24} mode
L	⎺╲⎽		V_{SS}	V_{DD}	L	counter ripples from an all HIGH state to an all LOW state

A test function has been included for the reduction of the test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections by connecting V_{SS}' to V_{DD} and V_{DD}' to V_{SS}. Via I_2 (connected to O_2) 255 counts are loaded into each of the 8-stage sections in parallel. All flip-flops are now at a HIGH state.

The counter is now returned to the normal 24-stage in series configuration by connecting V_{SS}' to V_{SS} and V_{DD}' to V_{DD}. One more pulse is entered into input I_2, which will cause the counter to ripple from an all HIGH state to an all LOW state.

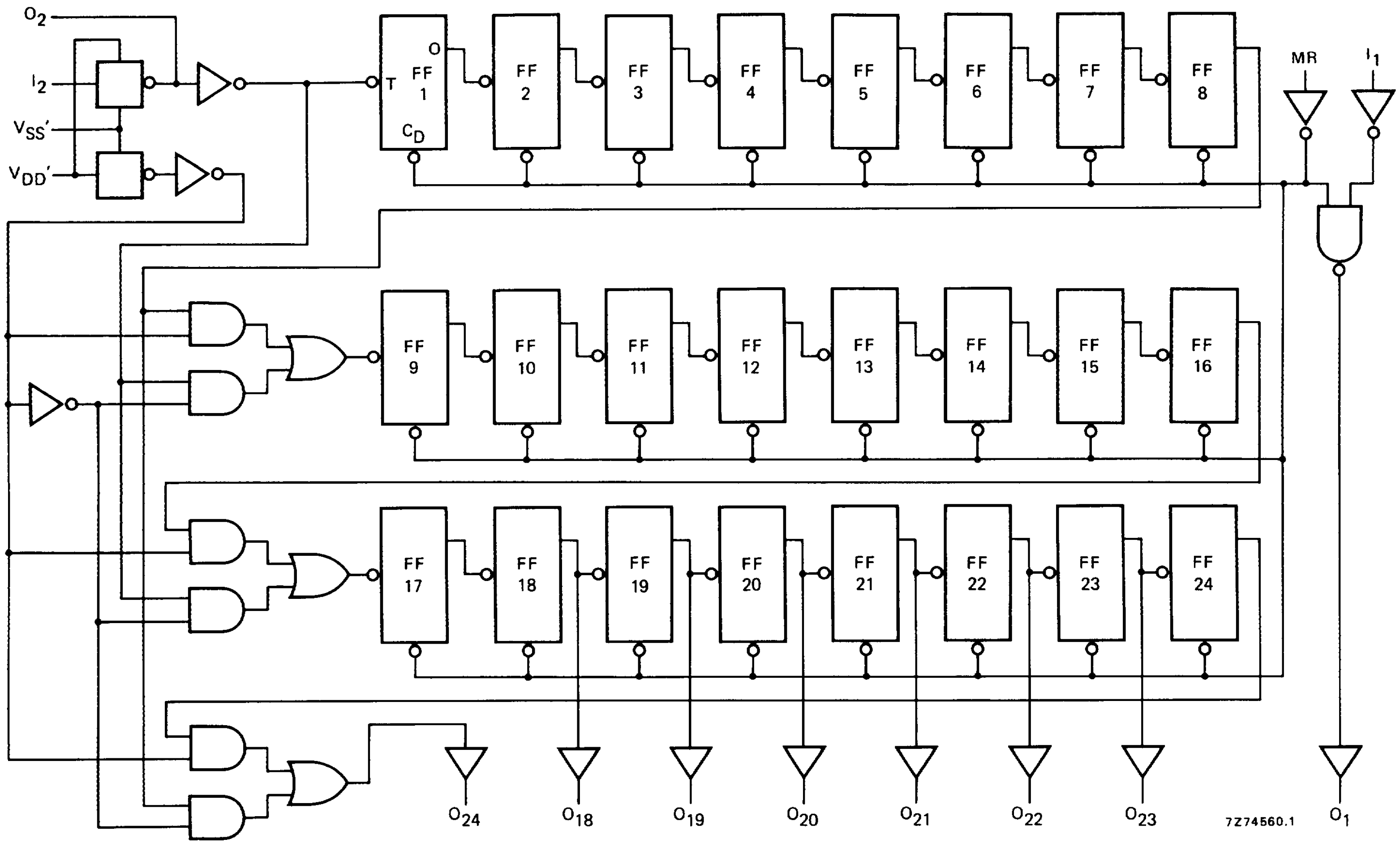


Fig.3 Logic diagram; for schematic diagram of clock circuit see Fig.4.

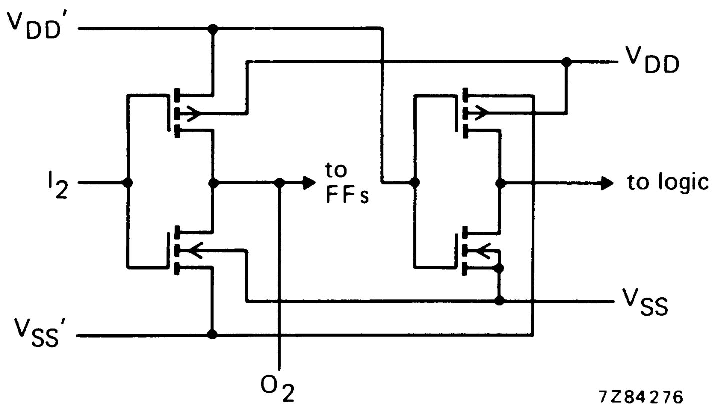


Fig.4 Schematic diagram of clock input circuitry.

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays							
$I_2 \rightarrow O_{18}$	5			950	1900	ns	923 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		350	700	ns	339 ns + (0,23 ns/pF) C_L
	15			220	440	ns	212 ns + (0,16 ns/pF) C_L
	5			950	1900	ns	923 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		350	700	ns	339 ns + (0,23 ns/pF) C_L
	15			220	440	ns	212 ns + (0,16 ns/pF) C_L
$O_n \rightarrow O_n + 1$	5			40	80	ns	13 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		15	30	ns	4 ns + (0,23 ns/pF) C_L
	15			10	20	ns	2 ns + (0,16 ns/pF) C_L
	5			40	80	ns	13 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		15	30	ns	4 ns + (0,23 ns/pF) C_L
	15			10	20	ns	2 ns + (0,16 ns/pF) C_L
$MR \rightarrow O_n$	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
$I_1 \rightarrow O_1$	5			90	180	ns	63 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
	5			60	120	ns	33 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		30	60	ns	19 ns + (0,23 ns/pF) C_L
	15			20	40	ns	12 ns + (0,16 ns/pF) C_L

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Output transition times							
HIGH to LOW	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
LOW to HIGH	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		
Minimum I_2 pulse width; HIGH	5		80	40		ns	see also waveforms Fig.5
	10	t_{WI2H}	40	20		ns	
	15		30	15		ns	
Minimum MR pulse width; HIGH	5		70	35		ns	
	10	t_{WMRH}	40	20		ns	
	15		30	15		ns	
Recovery time for MR	5		20	–10		ns	
	10	t_{RMR}	15	–5		ns	
	15		15	0		ns	
Maximum clock pulse frequency	5		6	12		MHz	
	10	f_{max}	12	25		MHz	
	15		17	35		MHz	

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$1\,200\ f_i + \sum (f_oC_L) \times V_{DD}^2$	where
	10	$5\,100\ f_i + \sum (f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	15	$13\,050\ f_i + \sum (f_oC_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = load capacitance (pF)
			$\sum (f_oC_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

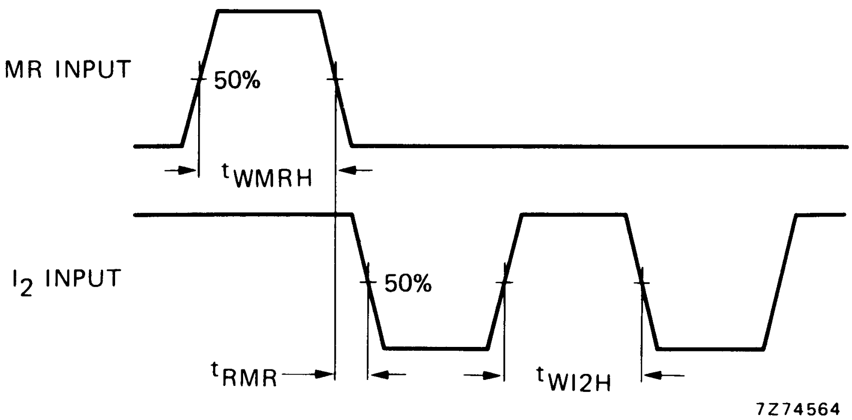
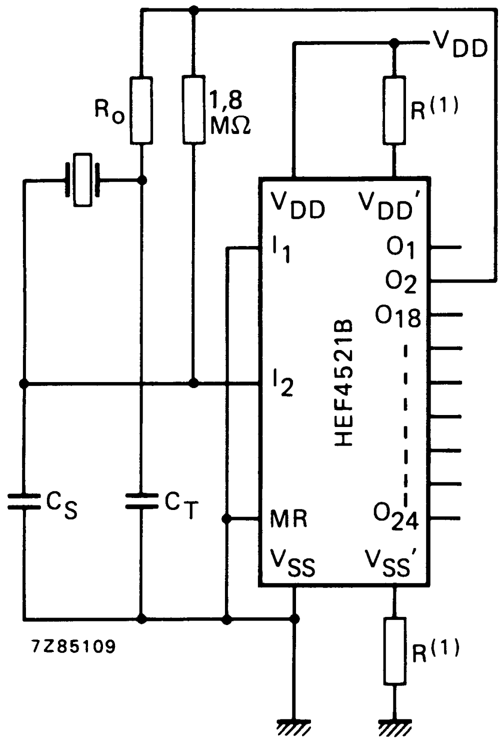


Fig.5 Waveforms showing minimum pulse widths for MR and I_2, recovery time for MR.

APPLICATION INFORMATION



(1) Optional for low power operation.

Fig.6 Crystal oscillator circuit.

Typical characteristics for crystal oscillator circuit (Fig.6):

	500 kHz CIRCUIT	**50 kHz CIRCUIT**	**UNIT**
Crystal characteristics			
resonance frequency	500	50	kHz
crystal cut	S	N	–
equivalent resistance; R_S	1	6,2	kΩ
External resistor/capacitor values			
R_o	47	750	kΩ
C_T	82	82	pF
C_S	20	20	pF

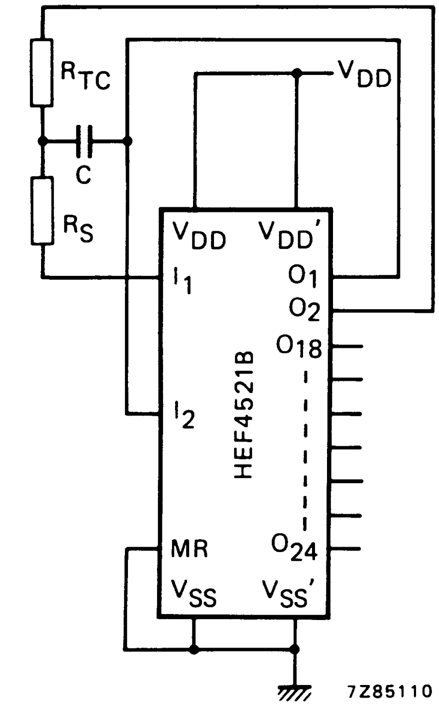
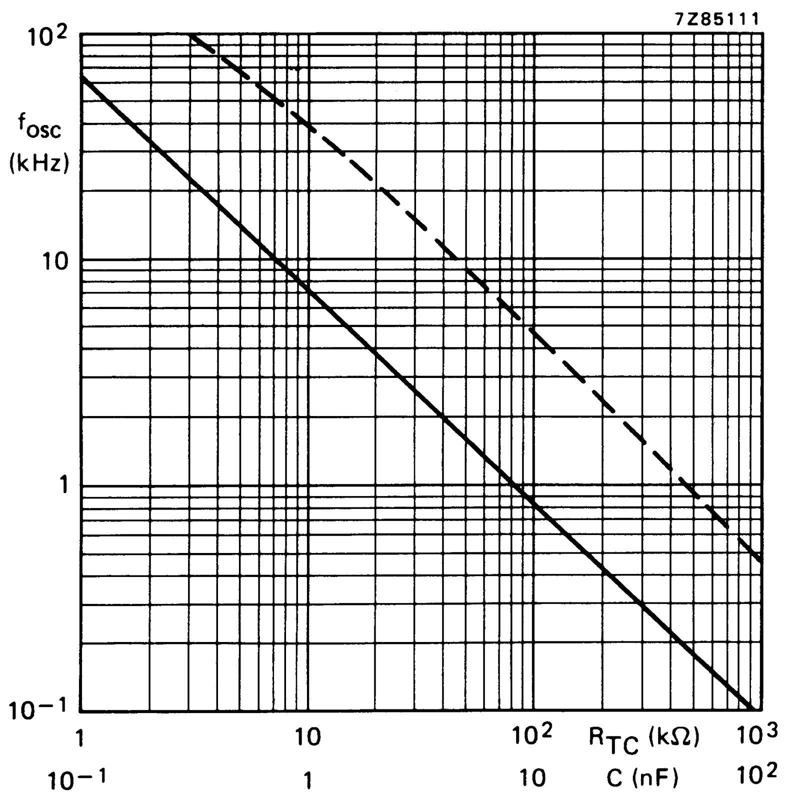


Fig.7 RC oscillator circuit;

$$f \approx \frac{1}{2{,}3 \times R_{TC} \times C};\ R_S \geq 2\ R_{TC}, \text{ in which:}$$

f in Hz, R in Ω, C in F.

$$R_S + R_{TC} < \frac{V_{IL\ max}}{I_{LI}}$$ (maximum input voltage LOW) (input leakage current)



— — — R_{TC}; C = 1 nF; $R_S \approx 2\ R_{TC}$
——— C; R_{TC} = 56 kΩ; R_S = 120 kΩ

Fig.8 Oscillator frequency as a function of R_{TC} and C; V_{DD} = 10 V; test circuit is Fig.7.

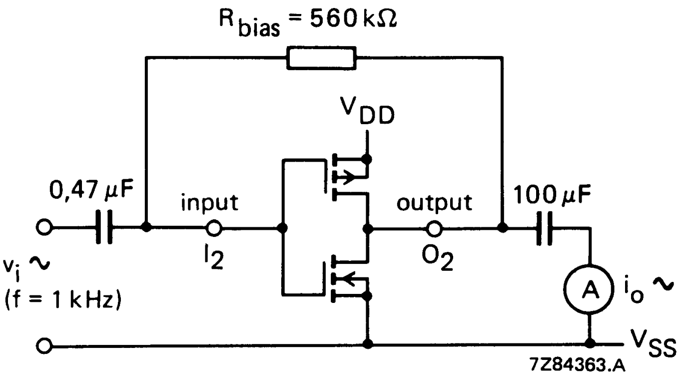
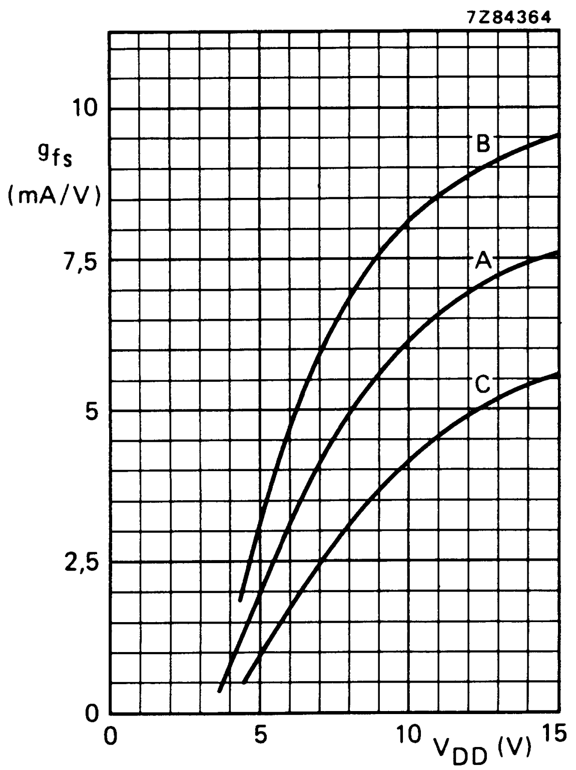


Fig.9 Test set-up for measuring forward transconductance $g_{fs} = di_o/d_{vi}$ at v_o is constant (see also graph Fig.10).



A: average,

B: average + 2 s,

C: average – 2 s, in which: ‘s’ is the observed standard deviation.

Fig.10 Typical forward transconductance g_{fs} as a function of the supply voltage at T_{amb} = 25 °C.

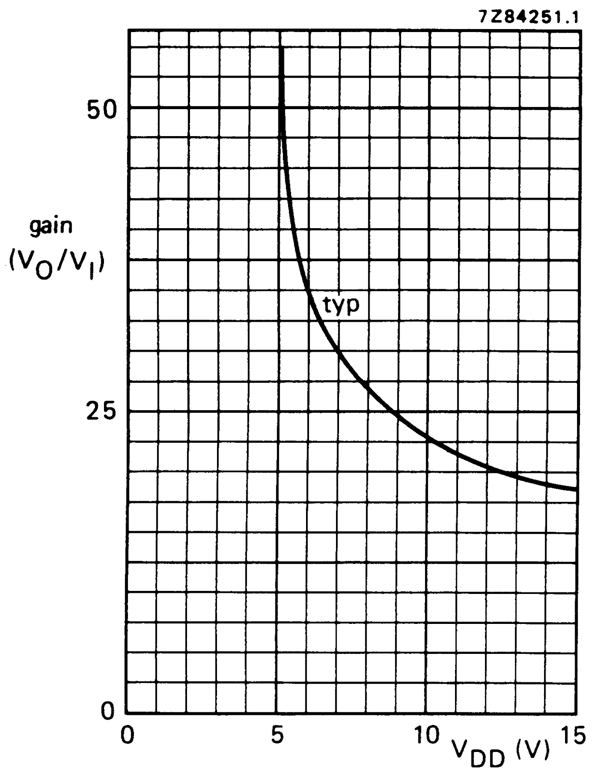


Fig.11 Voltage gain V_O/V_I as a function of supply voltage.

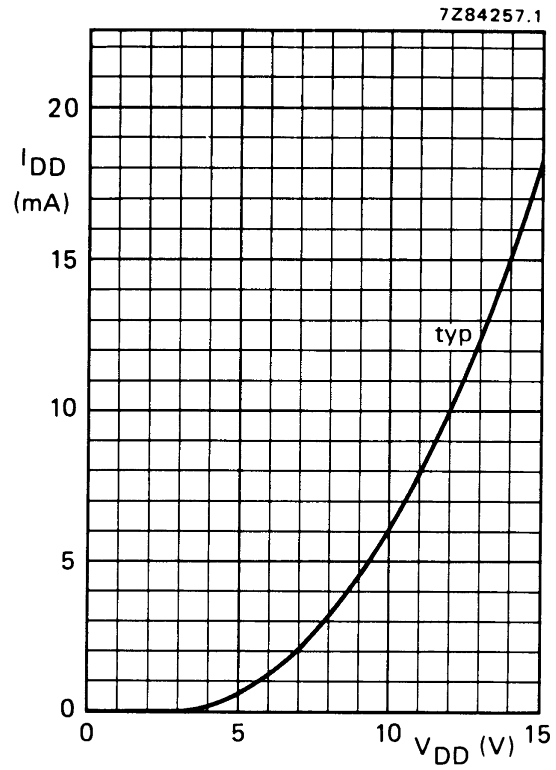


Fig.12 Supply current as a function of supply voltage.

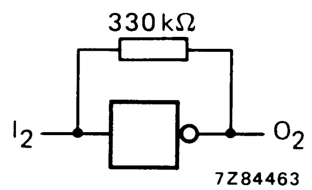


Fig.13 Test set-up for measuring graphs of Figs 11 and 12.