MT6223 GSM/GPRS Baseband Processor Data Sheet

Revision 2.10

Jan 29, 2008

Revision History

Revision	Date	Comments
1.00	Oct 26, 2006	First Release
1.01	Nov 6, 2006	Modify Pin-out, LCD interface, GPIO and analog control
1.02	Nov 17, 2006	1. Modify LCD interface 2. Modify EMI descriptions 3. Modify GPIO 4. Modify Analog front end and audio front end
1.03	Dec 1, 2006	1. Modify micro-controller subsystem descriptions. 2. Add PMU descriptions into analog front end part.
1.06	Mar 19, 2007	1. Update Baseband Front End descriptions 2. Update General Purpose IO descriptions 3. Add Efuse Controller segment 4. Update analog front end and PMU part descriptions 5. Update Auxiliary ADC segment 6. Update Automatic Frequency Control segment 7. Update Timing Generator descriptions 8. Update Software power down control
1.07	Apr 3, 2007	1. Remove NAND and memory card interface descriptions 2. Remove NiMH battry charger support in product summary section
1.08	Apr 13, 2007	1. Modify naming of external memory interface pin out
1.09	May 29,2007	1. Modify system overview descriptions
1.10	Jun 6th, 2007	1. Update information for MT6223P, including feature and part number 2. Hardware change for MT6223P's new feature, including LCD interface change and GPIO setting
1.11	Jun 13th, 2007	1. Correct the typo in row number of TFBGA dimension 2. BPI_BUS2 should be placed in ball number R3, and number U2 have no ball out
1.12	Jun 14th, 2007	1. Modified TFBGA diagram figure
1.13	Jun 21th, 2007	Limit the card type
1.14	Jun 26th, 2007	Reverse Aux Func. 0 and Aux Func. 1
1.15	Jun 27th, 2007	Remove serial LCD interface and EINT7 in 2.3 Pin description, MFIQ should reside at GPIO

		mode 1 of GPIO52
1.16	Jul 5th, 2007	Add driving strength to BPI_BUS3 and slow-down control for wavetable, corresponding to E5
1.17	Jul 21th, 2007	Modify the BGA diagram
1.18	Aug 02th, 2007	Remove incorrect description about USB and other project name. Change the VRTC LDO spec.
1.19	Aug 22th, 2007	Remove GPIO52 mode 0 from ECS3_B. Add digital pin electrical characteristics section
1.20	Aug 24th, 2007	Replace MIRQ at EINT2 (GPIO42)
2.00	Aug 30th, 2007	Revised CC mode spec.
2.01	Oct 4th, 2007	Correct GPIO50 definition and new electrical characteristics
2.02	Oct 9th, 2007	Revised LCD datasheet
2.03	Oct 11th, 2007	Add RGU, Clock chapters
2.04	Oct 19th, 2007	Resume GPI52: GPIO52 allows input mode only
2.05	Oct 31th, 2007	Remove serial LCD in GPIO chapter
2.06	Nov 20th, 2007	EMI_ADMUX defined at GPIO20, rather than GPIO4
2.07	Nov 30th, 2007	Remove EINT7 from GPIO list of LCD_CS1_B. Remove EINT7 source description from CIRQ
2.08	Dec 17th, 2007	Add manual for CIF. Remove MT6227 description in EMI chapter
2.09	Jan 18th, 2008	Description of PMIC_CON1
2.10	Jan 29th, 2008	Application notes for camera back-end

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1. System Overview

MT6223 is an entry level chipset solution with class 12 GPRS/GSM modem. It integrates only only analog baseband but also power management blocks into one chip and can greatly reduce the component count and make smaller PCB size. Besides, MT6223 is capable of SAIC (Single Antenna Interference Cancellation) and AMR speech. Based on 32 bit ARM7EJ-S™ RISC processor, MT6223 provides an unprecedented platform for high quality modem performance.

Typical application diagram is shown in **Figure** 1.

Platform

MT6223 runs the ARM7EJ-S™ RISC processor at up to 52Mhz, thus providing best trade-off between system performance and power consumption.

For large amount of data transfer, high performance DMA (Direct Memory Access) with hardware flow control is implemented, which greatly enhances the data movement speed while reducing MCU processing load.

Targeted as a modem-centric platform for mobile applications, MT6223 also provides hardware security digital rights management for copyright protection. For further safeguarding, and to protect manufacturer's development investment, hardware flash content protection is also provided to prevent unauthorized porting of software load.

Memory

MT6223 supports up to 4 external state-of-the-art devices through its 8/16-bit host interface. Devices such as burst/page mode Flash, page mode SRAM, and Pseudo SRAM are supported including ADMUX type devices. For greatest compatibility, the memory interface can also be used to connect to legacy devices such as Color/Parallel LCD, and multi-media companion chip are all supported through this interface. To minimize power consumption and ensure low noise, this interface is designed for flexible I/O voltage and allows lowering of supply voltage down to 1.8V. The driving strength is configurable for signal integrity adjustment. The data bus also employs retention technology to prevent the bus from floating during turn over.

Multi-media

MT6223 utilize high resolution audio DAC, digital audio, and audio synthesis technology to provide superior audio features., e.g. MP3 ring tone. For MT6223C, MP3 player is also supported.

Connectivity, and Storage

MT6223 supports UART as well as Bluetooth interface. Also, necessary peripheral blocks are embedded for a voice centric phone: Keypad Scanner with the capability to detect multiple key presses, SIM Controller, Alerter, Real Time Clock, PWM, Serial LCD Controller, and General Purpose Programmable I/Os.

Furthermore, to provide more configuration and bandwidth for display, an additional 9-bit parallel interface is incorporated.

For MT6223C, memory card control is provided through LCD interface, including SD and mini SD, etc. Therefore high quality MP3 playback of 48kHz sampling with 320kbps format can be supported

Audio

Using a highly integrated mixed-signal Audio Front-End, architecture of MT6223 allows for easy audio interfacing with direct connection to the audio transducers. The audio interface integrates D/A and A/D Converters for Voice band, as well as high resolution Stereo D/A Converters for Audio band. In addition, MT6223 also provides Stereo Input and Analog Mux. MT6223 also supports AMR codec to adaptively optimize speech and audio quality.

Radio

MT6223 integrates a mixed-signal Baseband front-end in order to provide a well-organized radio interface with flexibility for efficient customization. It contains gain and offset calibration mechanisms, and filters with programmable coefficients for comprehensive compatibility control on RF modules. This approach also allows the usage of a high resolution D/A Converter for controlling VCXO or crystal, thus reducing the need for expensive TCVCXO. MT6223 achieve great MODEM performance by utilizing 14-bit high resolution A/D Converter in the RF downlink path. Furthermore, to reduce the need for extra external current-driving component, the driving strength of some BPI outputs is designed to be configurable.

Debug Function

The JTAG interface enables in-circuit debugging of software program with the ARM7EJ-S core. With this

standardized debugging interface, MT6223 provides developers with a wide set of options in choosing ARM development kits from different third party vendors.

Low Power Features

MT6223 offers various low-power features to help reduce system power consumption. These features include Pause Mode of 32KHz clocking at Standby State, Power Down Mode for individual peripherals, and Processor Sleep Mode. In addition, MT6223 are also fabricated in advanced low leakage CMOS process, hence providing an overall ultra low leakage solution.

Power Management

MT6223 integrates all regulators that a voice-centric phone needs. Seven LDOs optimized for Specific GSM/GPRS baseband sub-systems are included, and a RF transceiver needed LDO is also built-in. Besides Li-Ion battery charge function, SIM card level shifter interface, two open-drain output switches to control the LED and vibrator are equipped. Other power management schemes such as thermal overload protection, Under Voltage Lock-out Protection (UVLO), over voltage protection and oower-on reset and start-up timer are also MT6223 features. Besides, 3 NMOS switches controlling the RGB LEDs are also embedded to reduce BOM coount.

Package

The MT6223 device is offered in 9mm×9mm, 224-ball, 0.5 mm pitch, TFBGA package.

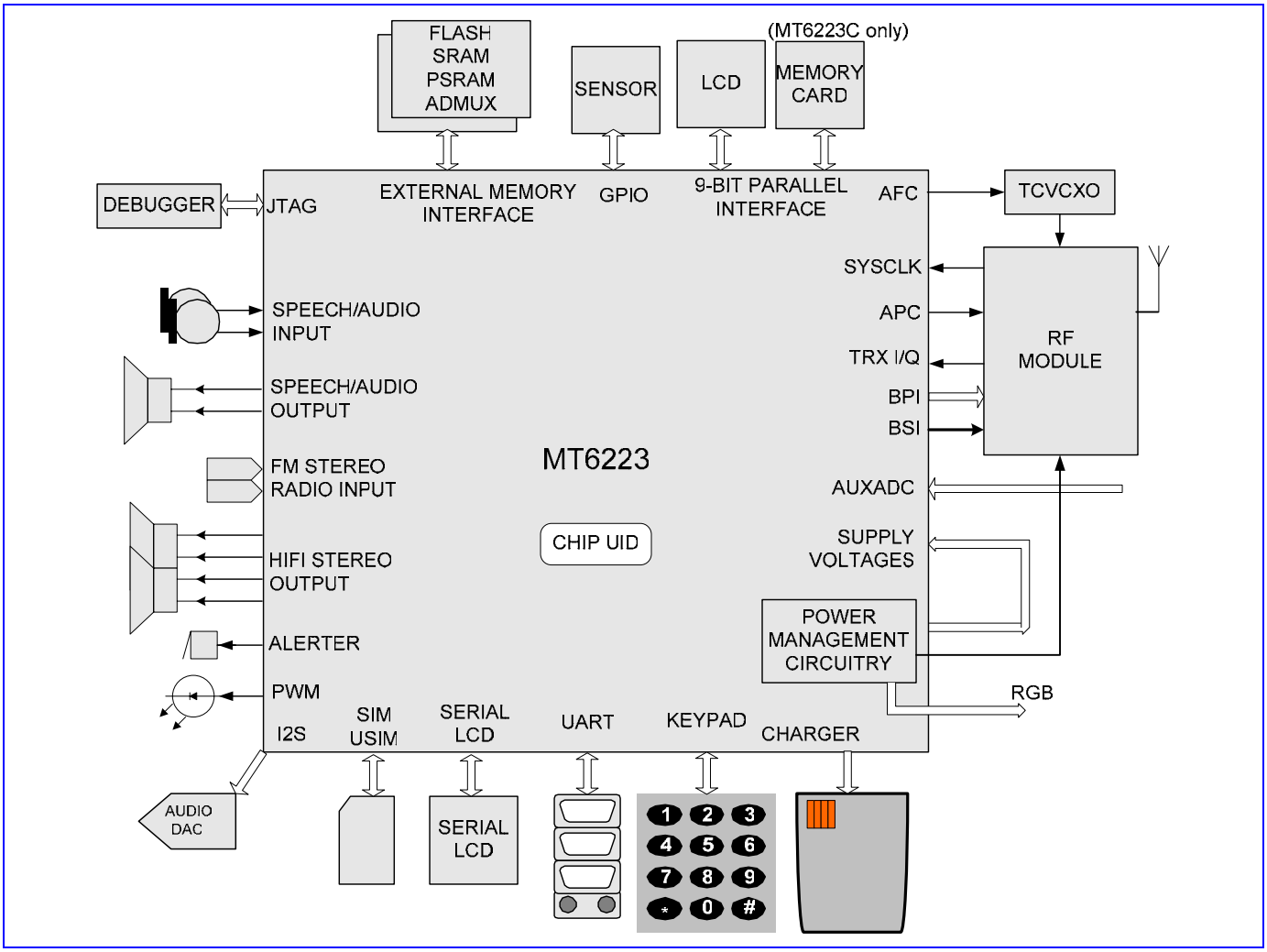


Figure 1 Typical application of MT6223.

1.1 Platform Features

- **General**
  - Integrated voice-band, audio-band and base-band analog front ends
  - TFBGA 9mm×9mm, 224-ball, 0.5 mm pitch package
- **MCU Subsystem**
  - ARM7EJ-S 32-bit RISC processor
  - High performance multi-layer AMBA bus
  - Java hardware acceleration for fast Java-based games and applets
  - Operating frequency: 26/52 MHz
  - Dedicated DMA bus
  - 7 DMA channels
  - 320K bits on-chip SRAM
  - On-chip boot ROM for Factory Flash Programming
  - Watchdog timer for system crash recovery
  - 3 sets of General Purpose Timer
  - Circuit Switch Data coprocessor
  - Division coprocessor
- **External Memory Interface**
  - Supports up to 4 external devices
  - Supports 8-bit or 16-bit memory components with maximum size of up to 32M Bytes each
  - Supports Flash and SRAM/PSRAM with Page Mode or Burst Mode
  - Supports ADMUX
  - Industry standard 9-bit Parallel LCD Interface
  - Supports multi-media companion chips with 8/16 bits data width
  - Flexible I/O voltage of 1.8V ~ 2.8V for memory interface
  - Configurable driving strength for memory interface
- **User Interfaces**
  - 5-row × 7-column keypad controller with hardware scanner
  - Supports multiple key presses for gaming
  - SIM/USIM Controller with hardware T=0/T=1 protocol control
  - Real Time Clock (RTC) operating with a separate power supply
  - General Purpose I/Os (GPIOs)
  - 2 Sets of Pulse Width Modulation (PWM) Output
  - Alerter Output with Enhanced PWM or PDM
  - 6 external interrupt lines
- **Security**
  - Supports security key and 59 bit chip unique ID
- **Connectivity**
  - 3 UARTs with hardware flow control and speed up to 921600 bps
  - DAI/PCM and I2S interface for Audio application
  - Memory card interface is provided for MT6223C. SD and MMC cards are supported
- **Low Power Schemes**
  - Power Down Mode for analog and digital circuits
  - Processor Sleep Mode
  - Pause Mode of 32KHz clocking at Standby State
  - 3-channel Auxiliary 10-bit A/D Converter for application usage other than battery monitoring
- **Power and Supply Management**
  - 2.8V to 5.5V Input Range
  - Charger Input up to 8V
  - Seven LDOs Optimized for Specific GSM Sub-systems
  - One LDO for RF transceiver
  - High Operation Efficiency and Low Stand-by Current
  - Li-Ion Battery Charge function
  - SIM Card Interface
  - Two Open-Drain Output Switches to Control the LED and Vibrator
  - Three NMOS switches to control RGB LEDs

- Thermal Overload Protection
- Under Voltage Lock-out Protection
- Over Voltage Protection
- Power-on Reset and Start-up Timer

- **Test and Debug**
  - Built-in digital and analog loop back modes for both Audio and Baseband Front-End
  - DAI port complying with GSM Rec.11.10
  - JTAG port for debugging embedded MCU

1.2 MODEM Features

- **Radio Interface and Baseband Front End**
  - GMSK modulator with analog I and Q channel outputs
  - 10-bit D/A Converter for uplink baseband I and Q signals
  - 14-bit high resolution A/D Converter for downlink baseband I and Q signals
  - Calibration mechanism of offset and gain mismatch for baseband A/D Converter and D/A Converter
  - 10-bit D/A Converter for Automatic Power Control
  - 13-bit high resolution D/A Converter for Automatic Frequency Control
  - Programmable Radio RX filter with adaptive bandwidth control
  - Dedicated Rx filter for FB acquisition
  - 2 Channels Baseband Serial Interface (BSI) with 3-wire control
  - Bi-directional BSI interface. RF chip register read access with 3-wire or 4-wire interface.
  - 10-Pin Baseband Parallel Interface (BPI) with programmable driving strength
  - Multi-band support
- **Voice and Modem CODEC**
  - Dial tone generation
  - Voice Memo
  - Noise Reduction
  - Echo Suppression
  - Advanced Sidetone Oscillation Reduction
  - Digital sidetone generator with programmable gain
  - Two programmable acoustic compensation filters
  - GSM/GPRS quad vocoders for adaptive multirate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
  - GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
  - GPRS GEA1, GEA2 and GEA3 ciphering

- Programmable GSM/GPRS Modem
- GSM Circuit Switch Data
- GPRS Class 12

- **Voice Interface and Voice Front End**
  - Two microphone inputs sharing one low noise amplifier with programmable gain and automatic gain control (AGC) mechanism
  - Voice power amplifier with programmable gain
  - 2nd order Sigma-Delta A/D Converter for voice uplink path
  - D/A Converter for voice downlink path
  - Supports half-duplex hands-free operation
  - Compliant with GSM 03.50

1.3 Multi-Media Features

- **LCD Interface**
  - Dedicated Parallel Interface supports 2 external 8/9 bit Parallel Interface, and Serial interface for LCM
  - For MT6223C, memory card interface is shared with LCD interface. And the memory card control is available for MP3 playback
- **LCD Controller**
  - Supports simultaneous connection to up to 3 parallel LCD or 2 serial LCD modules
  - Supports LCM format: RGB332, RGB444, RGB565, RGB666, RGB888
  - Supports LCD module with maximum resolution up to 176x220 at 24bpp
  - 2 layer blending
  - Supports hardware display rotation for each layer
- **Audio CODEC**
  - Wavetable synthesis with up to 64 tones
  - Advanced wavetable synthesizer capable of generating simulated stereo
  - Wavetable including GM full set of 128 instruments and 47 sets of percussions
  - PCM Playback and Record
  - Digital Audio Playback
- **Audio Interface and Audio Front End**
  - Supports I2S interface
  - High resolution D/A Converters for Stereo Audio playback
  - Stereo analog input for stereo audio source
  - Analog multiplexer for Stereo Audio
  - FM Radio Recording
  - Stereo to Mono Conversion

1.4 General Description

Figure 2 details the block diagram of MT6223. Based on a dual-processor architecture, MT6223 integrate both an ARM7EJ-S core and 2 digital signal processor cores. ARM7EJ-S is the main processor that is responsible for running 2G and 2.5G protocol software. Digital signal processors handle the MODEM algorithms as well as advanced audio functions. Except for some mixed-signal circuitries, the other building blocks in MT6223 are connected to either the microcontroller or one of the digital signal processor.

Specifically, both MT6223 consist of the following subsystems:

- Microcontroller Unit (MCU) Subsystem - includes an ARM7EJ-S RISC processor and its accompanying memory management and interrupt handling logics.
- Digital Signal Processor (DSP) Subsystem - includes 2 DSP cores and their accompanying memory, memory controller, and interrupt controller.
- MCU/DSP Interface - where the MCU and the DSPs exchange hardware and software information.
- Microcontroller Peripherals - includes all user interface modules and RF control interface modules.
- Microcontroller Coprocessors - runs computing-intensive processes in place of Microcontroller.
- DSP Peripherals - hardware accelerators for GSM/GPRS/EGDE channel codec.
- Voice Front End - the data path for converting analog speech from and to digital speech.
- Audio Front End - the data path for converting stereo audio from stereo audio source
- Baseband Front End - the data path for converting digital signal from and to analog signal of RF modules.
- Timing Generator - generates the control signals related to the TDMA frame timing.
- Power, Reset and Clock subsystem - manages the power, reset, and clock distribution inside MT6223
- LDOs, Power-on sequences, swicthes and SIM level shifters.

Details of the individual subsystems and blocks are described in following Chapters.

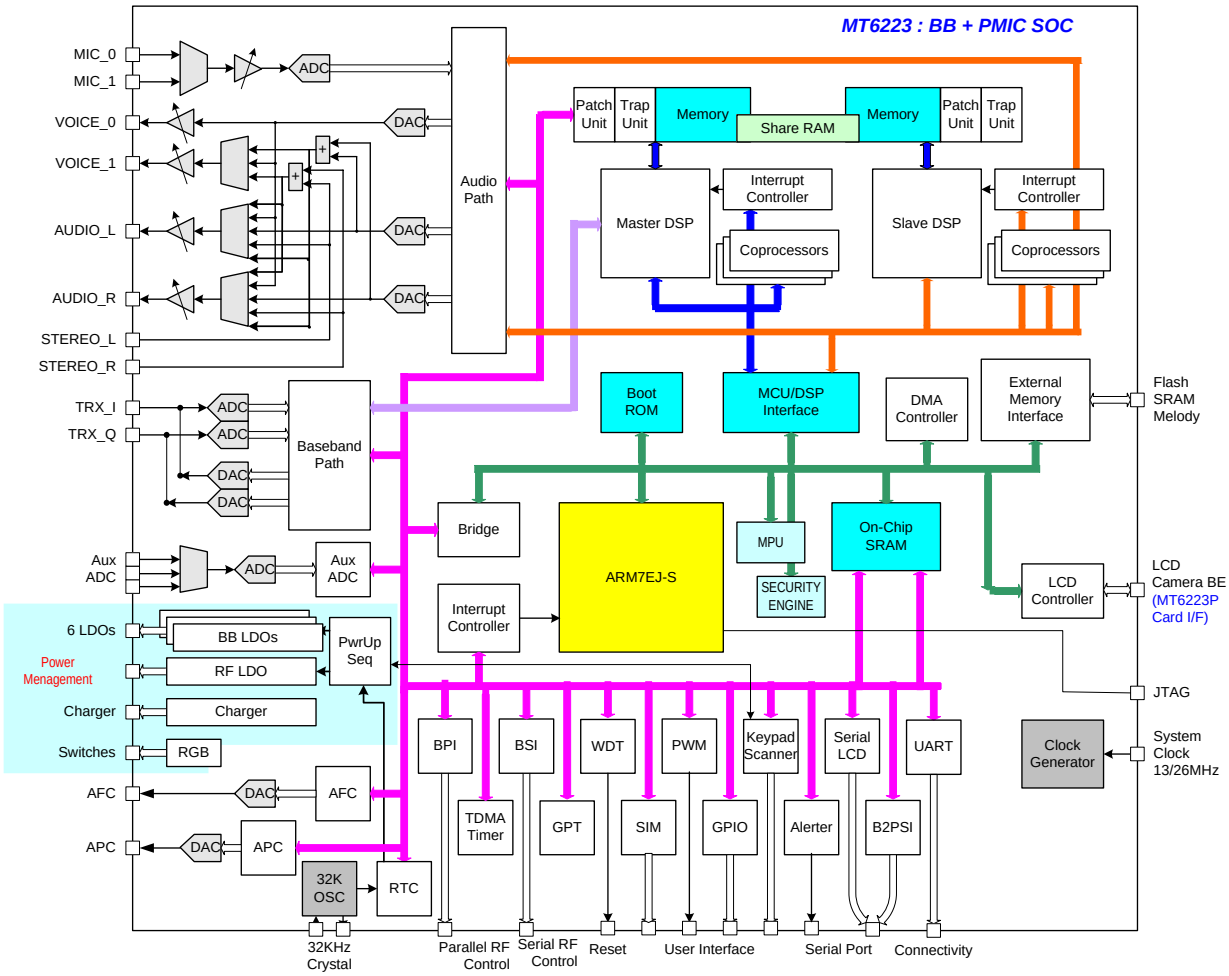


Figure 2 MT6223 block diagram.

2 Product Descriptions

2.1 Pin Outs

One type of package for this product, TFBGA 9mm * 9mm, 224-ball, 0.5mm pitch Package is offered.

Pin-outs and the top view are illustrated in **Figure 3** for this package. Outline and dimension of package is illustrated in **Figure 4**, while the definition of package is shown in **Table 1**.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	VBAT	AVBAT	VBAT_RF	BATSENSE	VSIM	AGND_RF	VCORE	VRF	UTXD3	XOUT	XIN	KROW2	KCOL0	KCOL2	KCOL4	SRCLKENA	SRCLKENAI	A
B	VREF	VBAT	VBAT	ISENSE	SIMIO	VM	VIO	VRF_SENSE	URXD3	AVDD_RTC	EINT1	KROW1	KROW4	KCOL1	KCOL3	EA24	EA23	B
C	VA	RESET		GATEDRV	BATDET	SIMRST	URXD1	URXD2	URTS1_B	UTXD1	EINT2	KROW0	KROW3	EA22		EA21	EA20	C
D	AGND	RSTCAP	PWRKEY	LED	CHRIN	SIMCLK	BAT_BACKUP	UTXD2	VDDK	UCTS1_B	EINT3	EINT0	VDD33	EA19	EA18	EA17	EA16	D
E	AVDD_AFE	VCTXO	AU_FMINR	VMSEL										EA15	EA14	EA13	EA12	E
F	AU_MOUTR	AU_MOUTL	AU_FMINL	AVDD_MBUFL										VDD33_EMI	EA11	EA10	EA9	F
G	AU_OUT0_N	AU_OUT0_P	AU_MICBIAS_P	AVSS_MBUFL				VIBRATOR	LED_G	LED_B				VDD33_EMI	EA8	EA7	EA6	G
H	AGND_AFE	AU_MICBIAS_N	AU_VREF_NI	AU_VREF_PO			DGND	LED_R	DGND	DGND	DGND			VDDK	EA5	EA4	EA3	H
J	AU_VIN0_P	AU_VIN0_N	AVSS_AFE	AVDD_GSMRFRX			VSS33	PGND		TESTMODE	VSS33			EA2	EA1	EA0	EUB_B	J
K	AU_VIN1_N	AU_VIN1_P	AGND_RFE	AVDD_RFE			VSS33	VSS33	VSS33_EMI	VSS33_EMI	VSS33_EMI			ELB_B	ECS3_B	ECS2_B	ECS1_B	K
L	BDLAQP	BDLAQN	BDLAIN	BDLAIP				VSS33_LOD	VSS33_EMI	VSS33_EMI				ECS0_B	EWR_B	ERD_B	ED15	L
M	AVSS_GSMRFRX	AUXADIN0	AUXADIN1	AVDD_PLL										VDD33_EMI	ED14	ED13	ED12	M
N	APC	AUXADIN2	AUX_REF	VDDK										VDD33_EMI	ED11	ED10	ED9	N
P	AVSS_RFE	AFC_BYP	BPI_BUS5	VDD33	VDD33	DAISYNC	PWM	JTDI	VDDK	LCD_D6	VDD33_LCD	VDD33_EMI	EA25	ED3	ED8	ED7	ED6	P
R	AFC	BPI_BUS0	BPI_BUS2	BPI_BUS6	BSI_DATA	DAIRST	ALERTER	JTRST_B	JTDO	LCD_D7	LCD_D2	LCD_WR_B	LCD_A0	LCD_CS0_B		ED4	ED5	R
T	AVSS_PLL	BPI_BUS1	BPI_BUS4	BPI_BUS7	BSI_CS0	DAICLK	DAIPCMIN	SYSRST_B	JTMS	LCD_D8	LCD_D3	LCD_RSTB	LCD_D0	WATCHDOG	EWAIT	ED0	ED2	T
U	SYSCLK		BPI_BUS3	BPI_BUS8	BPI_BUS9	BSI_CLK	DAIPCMOUT	JRTCK	JTCK	LCD_D5	LCD_D4	LCD_D1	LCD_RD_B	LCD_CS1_B	EADV_B	ECLK	ED1	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 3 Top View of MT6223 TFBGA 9mm*9mm 0.5mm pitch package

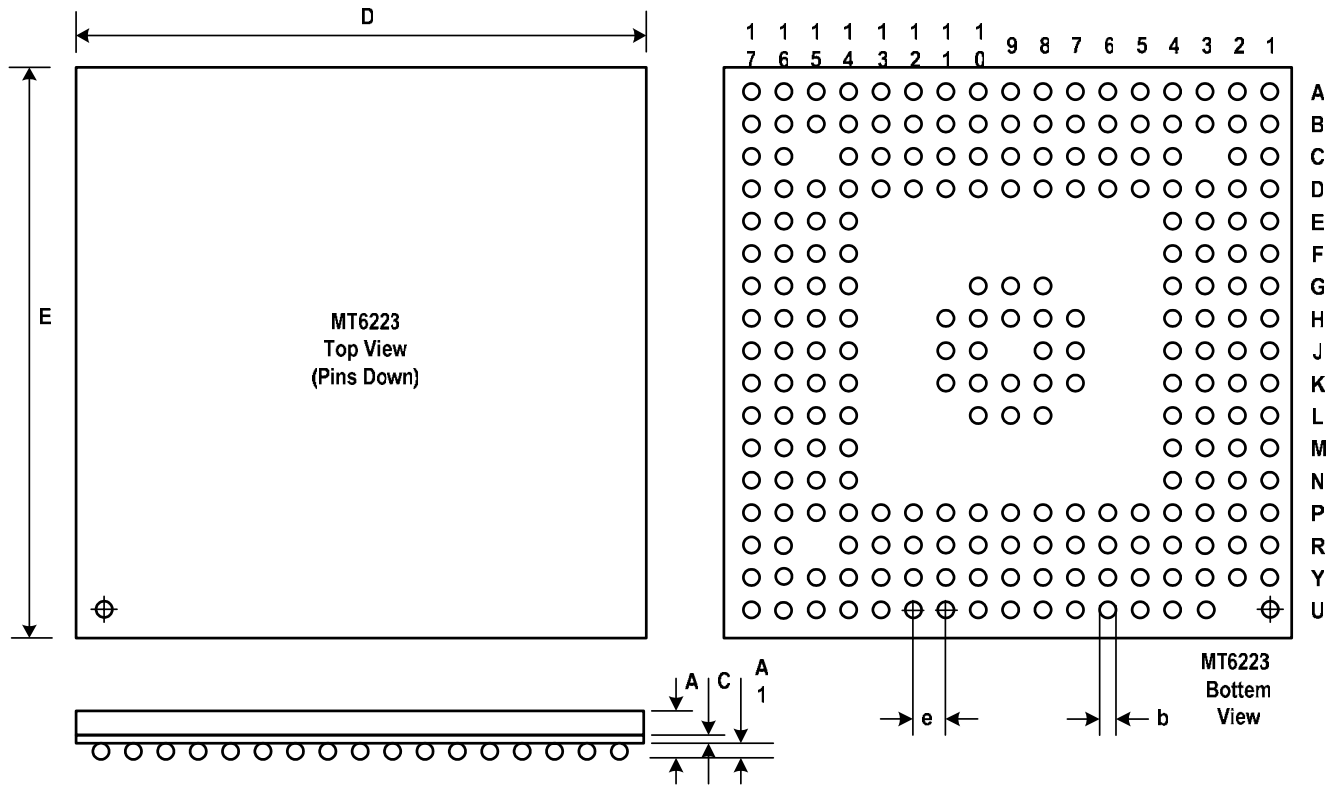


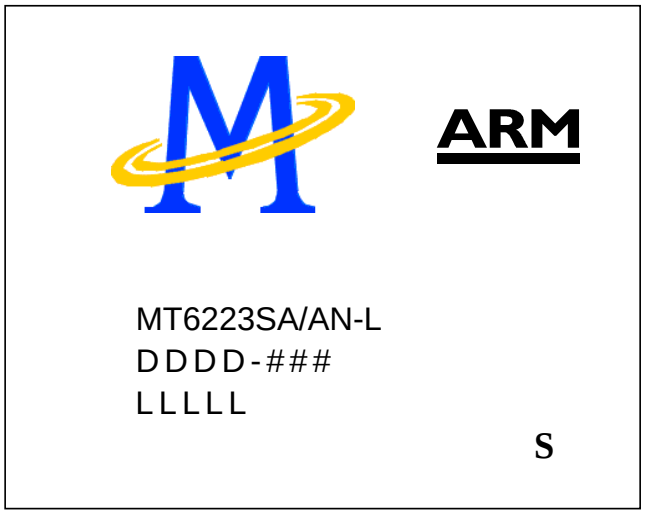
Figure 4 Outlines and Dimension of TFBGA 9mm*9mm, 224-ball, 0. 5 mm pitch Package

Body Size		Ball Count	Ball Pitch	Ball Dia.	Package Thk.	Stand Off	Substrate Thk.
D	E	N	e	b	A (Max.)	A1	C
9.0	9.0	224	0.5	0.275	1.2	0.21	0.36

Table 1 Definition of TFBGA 9mm*9mm, 224-ball, 0.5 mm pitch Package (Unit: mm)

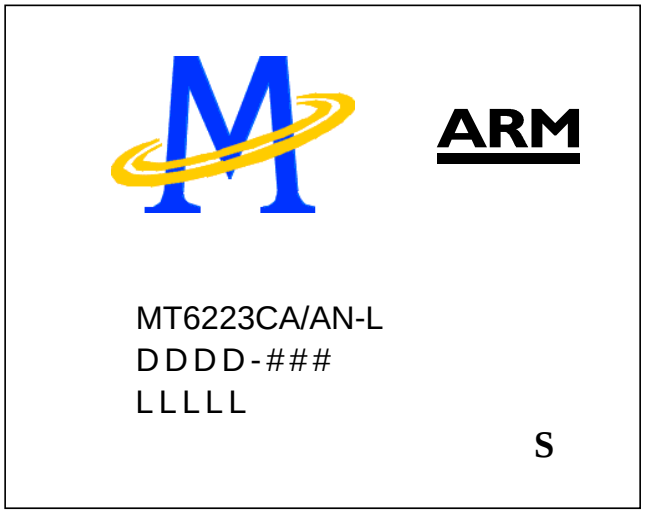
2.2 Top Marking Definition

Security version (MT6223S)



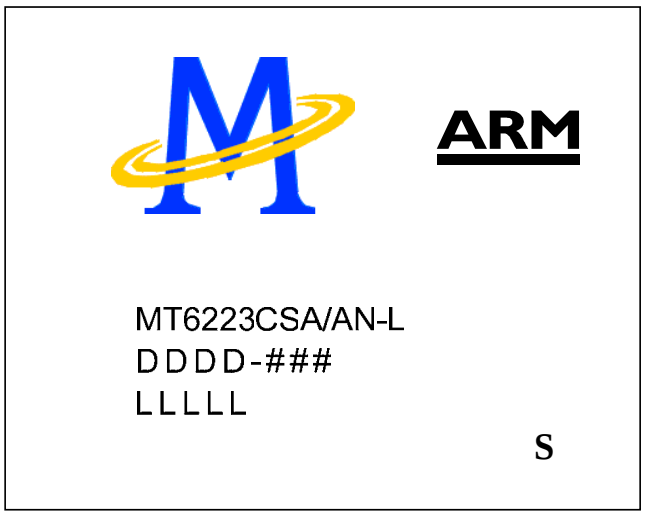
MT6223SA/AN-L: Part No.
DDDD: Date Code
###: Subcontractor Code
LLLLL: Die Lot No.
S: Special Code

Memory card MP3 version (MT6223C)



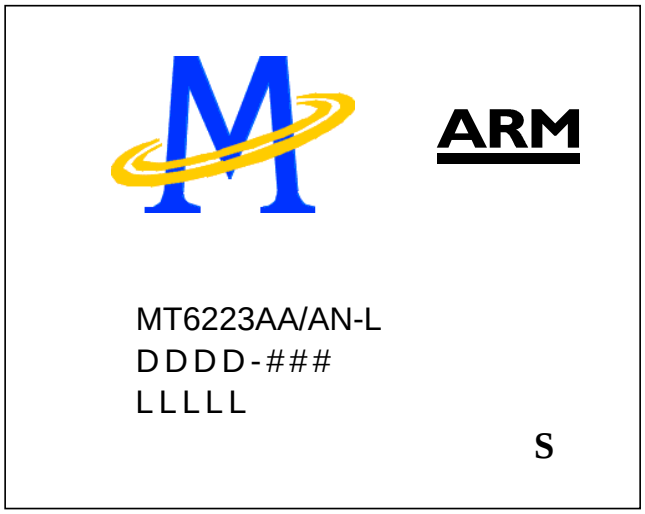
MT6223CA/AN-L: Part No.
DDDD: Date Code
###: Subcontractor Code
LLLLL: Die Lot No.
S: Special Code

Security, Memory card MP3 version (MT6223CS)



MT6223CSA/AN-L:Part No.
DDDD: Date Code
###: Subcontractor Code
LLLLL: Die Lot No.
S: Special Code

Non-security version (MT6223)



MT6223AA/AN-L: Part No.
DDDD: Date Code
###: Subcontractor Code
LLLLL: Die Lot No.
S: Special Code

#

DC Characteristics

2.2.1 Absolute Maximum Ratings

Prolonged exposure to absolute maximum ratings may reduce device reliability. Functional operation at these maximum ratings is not implied.

Item	Symbol	Min	Max	Unit
IO power supply	VDD33	-0.3	VDD33+0.3	V
I/O input voltage	VDD33I	-0.3	VDD33+0.3	V
Operating temperature	Topr	-20	80	Celsius
Storage temperature	Tstg	-55	125	Celsius

2.3 Pin Description

Below pin description is identical for both MT6223.

BGA	NAME	Dir	PIN DESCRIPTION	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	PU/PD	Reset
			Analog Baseband Interface						
F2	AU_MOUTL		Audio analog output left channel						
F1	AU_MOUTR		Audio analog output right channel						
E3	AU_FMINR		FM radio analog input right channel						
F3	AU_FMINL		FM radio analog input left channel						
G1	AU_OUT0_N		Earphone 0 amplifier output (-)						
G2	AU_OUT0_P		Earphone 0 amplifier output (+)						
G3	AU_MICBIAS_P		Microphone bias supply (+)						
H2	AU_MICBIAS_N		Microphone bias supply (-)						
H4	AU_VREF_PO		Audio reference voltage (+)						
H3	AU_VREF_NI		Audio reference voltage (-)						
J1	AU_VIN0_P		Microphone 0 amplifier input (+)						
J2	AU_VIN0_N		Microphone 0 amplifier input (-)						
K1	AU_VIN1_N		Microphone 1 amplifier input (-)						
K2	AU_VIN1_P		Microphone 1 amplifier input (+)						
L1	BDLAQP		Quadrature (Q+) baseband codec						
L2	BDLAQN		Quadrature (Q-) baseband codec						
L3	BDLAIN		Quadrature (I-) baseband codec						
L4	BDLAIP		Quadrature (I+) baseband codec						
N1	APC		Automatic power control DAC output						
M2	AUXADIN0		Auxiliary ADC input 0						
M3	AUXADIN1		Auxiliary ADC input 1						
N2	AUXADIN2		Auxiliary ADC input 2						
N3	AUX_REF		Reference voltage of Auxiliary ADC						
R1	AFC		Automatic frequency control DAC output						
P2	AFC_BYP		Automatic frequency control DAC bypass capacitance						
			RF control circuitry						
R2	BPI_BUS0	O	RF hard-wire control bus bit 0						
T2	BPI_BUS1	O	RF hard-wire control bus bit 1						
R3	BPI_BUS2	O	RF hard-wire control bus bit 2						
U3	BPI_BUS3	O	RF hard-wire control bus bit 3						
T3	BPI_BUS4	O	RF hard-wire control bus bit 4						
P3	BPI_BUS5	O	RF hard-wire control bus bit 5						
R4	BPI_BUS6	IO	RF hard-wire control bus bit 6	GPIO20	BPI_BUS6	XADMUX		PD	
T4	BPI_BUS7	IO	RF hard-wire control bus bit 7	GPIO21	BPI_BUS7	BSI_RFIN	clk_out0	PD	
U4	BPI_BUS8	IO	RF hard-wire control bus bit 8	GPIO22	BPI_BUS8	KCOL5	clk_out1	PU	
U5	BPI_BUS9	IO	RF hard-wire control bus bit 9	GPIO23	BPI_BUS9	BSI_CS1	clk_out2	PD	
T5	BSI_CS0	O	RF 3-wire control interface chip select 0						
R5	BSI_DATA	IO	RF 3-wire control interface data output						
U6	BSI_CLK	O	RF 3-wire control interface clock output						
			Digital Audio Interface (DAI)						
T6	DAICLK	IO	DAI interface clock output	GPIO15	DAICLK	EDICK		PU	
U7	DAIPCMOUT	IO	DAI PCM data output	GPIO16	DAIPCMOUT	EDIDAT		PD	
T7	DAIPCMIN	IO	DAI PCM data input	GPIO17	DAIPCMIN			PU	

R6	DAIRST	IO	DAI reset signal input	GPIO18	DAIRST			PU	
P6	DAISYNC	IO	DAI frame synchronization input	GPIO19	DAISYNC	EDIWS		PU	
			PWM Interface						
R7	ALERTER	IO	Pulse-width modulated signal for buzzer	GPIO24	ALERTER			PD	
P7	PWM	IO	Pulse-width modulated signal	GPIO25	PWM			PD	
			JTAG Interface						
U8	JRTCK	O	JTAG test port returned clock output					PU	
R8	JTRST_B	I	JTAG test port reset input	GPIO26	JTRST_B	EINT4		PD	
U9	JTCK	I	JTAG test port clock input					PU	
P8	JTDI	I	JTAG test port data input	GPIO27	JTDI	EINT5		PU	
T9	JTMS	I	JTAG test port mode switch	GPIO28	JTMS	EINT6		PU	
R9	JTDO	O	JTAG test port data output						
			Parallel LCD Interface						
T10	LCD_D8	IO	Parallel display interface Data 8	GPIO0	LCD_D8			PD	
R10	LCD_D7	IO	Parallel display interface Data 7	GPIO1	LCD_D7			PD	
P10	LCD_D6	IO	Parallel display interface Data 6	GPIO2	LCD_D6			PD	
U10	LCD_D5	IO	Parallel display interface Data 5	GPIO3	LCD_D5			PD	
U11	LCD_D4	IO	Parallel display interface Data 4	GPIO4	LCD_D4			PD	
T11	LCD_D3	IO	Parallel display interface Data 3	GPIO5	LCD_D3			PD	
R11	LCD_D2	IO	Parallel display interface Data 2	GPIO6	LCD_D2			PD	
U12	LCD_D1	IO	Parallel display interface Data 1	GPIO7	LCD_D1			PD	
T12	LCD_RSTB	O	Parallel display interface Reset Signal	GPIO8	LCD_RSTB			PU	
R12	LCD_WR_B	O	Parallel display interface Write Strobe	GPIO9	LCD_WR_B			PU	
U13	LCD_RD_B	O	Parallel display interface Read Strobe	GPIO10	LCD_RD_B			PU	
T13	LCD_D0	IO	Parallel display interface Data 0	GPIO11	LCD_D0			PD	
R13	LCD_A0	O	Parallel display interface address output	GPIO12	LCD_A0			PU	
R14	LCD_CS0_B	O	Parallel display interface chip select 0 output	GPIO13	LCD_CS0_B			PU	
U14	LCD_CS1_B	O	Parallel display interface chip select 1 output	GPIO14	LCD_CS1_B			PU	
			External Memory Interface						
U15	EADV_B	O	Flash, PSRAM and CellularRAM address valid, active low						
T15	EWAIT	O	Flash, PSRAM and CellularRAM data ready					PU	
U16	ECLK	O	Flash, PSRAM and CellularRAM clock						
P13	EA25	IO	External memory CRE pin						
T16	ED0	IO	External memory data bus 0						
U17	ED1	IO	External memory data bus 1						
T17	ED2	IO	External memory data bus 2						
P14	ED3	IO	External memory data bus 3						
R16	ED4	IO	External memory data bus 4						
R17	ED5	IO	External memory data bus 5						
P17	ED6	IO	External memory data bus 6						
P16	ED7	IO	External memory data bus 7						
P15	ED8	IO	External memory data bus 8						
N17	ED9	IO	External memory data bus 9						
N16	ED10	IO	External memory data bus 10						
N15	ED11	IO	External memory data bus 11						
M17	ED12	IO	External memory data bus 12						
M16	ED13	IO	External memory data bus 13						
M15	ED14	IO	External memory data bus 14						

L17	ED15	IO	External memory data bus 15						
L16	ERD_B	O	External memory read strobe, active low						
L15	EWR_B	O	External memory write strobe, active low						
L14	ECS0_B	O	External memory chip select 0						
K17	ECS1_B	O	External memory chip select 1						
K16	ECS2_B	O	External memory chip select 2					—	
K15	ECS3_B	O	External memory chip select 3	GPI52	MFIQ	ECS3		PU	
K14	ELB_B	O	External memory lower byte strobe						
J17	EUB_B	O	External memory upper byte strobe						
J16	EA0	O	External memory address bus 0	GPIO30	EA0	EA25		PD	
J15	EA1	O	External memory address bus 1						
J14	EA2	O	External memory address bus 2						
H17	EA3	O	External memory address bus 3						
H16	EA4	O	External memory address bus 4						
H15	EA5	O	External memory address bus 5						
G17	EA6	O	External memory address bus 6						
G16	EA7	O	External memory address bus 7						
G15	EA8	O	External memory address bus 8						
F17	EA9	O	External memory address bus 9						
F16	EA10	O	External memory address bus 10						
F15	EA11	O	External memory address bus 11						
E17	EA12	O	External memory address bus 12						
E16	EA13	O	External memory address bus 13						
E15	EA14	O	External memory address bus 14						
E14	EA15	O	External memory address bus 15						
D17	EA16	O	External memory address bus 16						
D16	EA17	O	External memory address bus 17						
D15	EA18	O	External memory address bus 18						
D14	EA19	O	External memory address bus 19						
C17	EA20	O	External memory address bus 20						
C16	EA21	O	External memory address bus 21						
C14	EA22	O	External memory address bus 22						
B17	EA23	O	External memory address bus 23						
B16	EA24	O	External memory address bus 24						
			System Miscellaneous						
J10	TESTMODE	I	Factory test mode enable input					PD	
T8	SYSRST_B	I	System reset input active low					PU	
T14	WATCHDOG	O	Watchdog reset output, active low	~~GPIO29~~	WATCHDOG				
A17	SRCLKENAI	I	External VCTCXO enable input	GPIO31	SRCLKENAI			PD	
A16	SRCLKENA	O	External VCTCXO enable output active high						
			Keypad Interface						
A15	KCOL4	I	Keypad column 4	GPIO32	KCOL4			PU	
B15	KCOL3	I	Keypad column 3	GPIO33	KCOL3			PU	
A14	KCOL2	I	Keypad column 2	GPIO34	KCOL2			PU	
B14	KCOL1	I	Keypad column 1	GPIO35	KCOL1			PU	
A13	KCOL0	I	Keypad column 0	GPIO36	KCOL0			PU	
B13	KROW4	O	Keypad row 4	GPIO37	KROW4				
C13	KROW3	O	Keypad row 3	GPIO38	KROW3				

A12	KROW2	O	Keypad row 2	GPIO39	KROW2				
B12	KROW1	O	Keypad row 1	GPIO40	KROW1				
C12	KROW0	O	Keypad row 0	GPIO41	KROW0				
			External Interrupt Inputs						
D12	EINT0	I	External interrupt 0		EINT0			PU	
B11	EINT1	I	External interrupt 1		EINT1			PU	
C11	EINT2	I	External interrupt 2	GPIO42	EINT2	MIRQ	BT	PU	
D11	EINT3	I	External interrupt 3	GPIO43	EINT3		BE	PU	
			UART						
C10	UTXD1	O	UART 1 transmit data	GPIO44	UTXD1			PU	
D10	UCTS1_B	I	UART 1 clear to send, active low	GPIO45	UCTS1_B		SCL	PU	
C9	URTS1_B	O	UART 1 request to send, active low	GPIO46	URTS1_B		SDA	PU	
A9	UTXD3	IO	UART 3 transmit data	GPIO47	UTXD3	UCTS2_B	clk_out3	PU	
B9	URXD3	IO	UART 3 receive data	GPIO48	URXD3	URTS2_B	clk_out4	PU	
C8	URXD2	IO	UART2 receive data	GPIO49	URXD2	clk_out5		PU	
C7	URXD1	I	UART 1 receive data	GPIO50	URXD1			PU	
D8	UTXD2	IO	UART2 transmit data	GPIO51	UTXD2			PU	
			Crystal and Clock Inputs						
U1	SYSCLK		13MHz or 26MHz system clock input						
A11	XIN		32.768 KHz crystal input						
A10	XOUT		32.768 KHz crystal output						
			SIM Card Interface						
B5	SIMIO	IO	SIM Data Input / Outputs						
C6	SIMRST		SIM card reset output						
D6	SIMCLK		SIM card clock output						
			Charger and LED Driving Interface						
D5	CHRIN		Charger input						
C4	GATEDRV								
G10	LED_B								
G9	LED_G								
H8	LED_R								
D4	LED								
G8	VIBRATOR		Vibrator driving output						
			LDO Outputs						
A5	VSIM		LDO output to SIM card						
A8	VRF		RF LDO output						
B8	VRF_SENSE		RF LDO output sensing input						
A7	VCORE		Digital core voltage LDO output						
B7	VIO		Digital I/O voltage LDO output						
B6	VM		External memory LDO output						
C1	VA		Analog LDO output						
E2	VCTXO		Crystal or VCTCXO LDO output						
			PMIC Miscellaneous						
A3	VBAT_RF		RF used battery voltage input						
B3	VBAT		Battery voltage input						
B2	VBAT		Battery voltage input						
A1	VBAT		Battery voltage input						
A2	AVBAT		Battery voltage input						

D7	BAT_BACKUP								
C5	BATDET		Battery detection input						
A4	BATSENSE		Battery sense input						
B4	ISENSE		Current sense input						
C2	RESET		Powr on reset						
D2	RSTCAP		Reset capacitor connection point						
B1	VREF		Reference voltage for PMIC						
E4	VMSEL		Memory supply voltage level select input						
D3	PWRKEY		Power key press input						
			Digital Power and Grounds						
J8	PGND		PMIC ground						
H7	DGND		PMIC ground						
H11	DGND		PMIC ground						
H10	DGND		PMIC ground						
H9	DGND		PMIC ground						
K7	VSS33		Groud of chip digital part I/O circuitry						
L8	VSS33		Groud of chip digital part I/O circuitry						
K8	VSS33		Groud of chip digital part I/O circuitry						
J11	VSS33		Groud of chip digital part I/O circuitry						
J7	VSS33		Groud of chip digital part I/O circuitry						
L9	VSS33_EMI		Groud of external memory interface						
K9	VSS33_EMI		Groud of external memory interface						
L10	VSS33_EMI		Groud of external memory interface						
K10	VSS33_EMI		Groud of external memory interface						
K11	VSS33_EMI		Groud of external memory interface						
N4	VDDK		Supply voltage of digital core circuitry						
P9	VDDK		Supply voltage of digital core circuitry						
D9	VDDK		Supply voltage of digital core circuitry						
H14	VDDK		Supply voltage of digital core circuitry						
D13	VDD33		Supply voltage of digital part I/O circuitry						
P4	VDD33		Supply voltage of digital part I/O circuitry						
P5	VDD33		Supply voltage of digital part I/O circuitry						
P11	VDD33_LCD		Supply voltage of display interface I/O circuitry						
P12	VDD33_EMI		Supply voltage of external memory interface						
N14	VDD33_EMI		Supply voltage of external memory interface						
M14	VDD33_EMI		Supply voltage of external memory interface						
G14	VDD33_EMI		Supply voltage of external memory interface						
F14	VDD33_EMI		Supply voltage of external memory interface						
			Analog Power and Grounds						
K4	AVDD_RFE								
F4	AVDD_MBUFL								
J4	AVDD_GSMRFRX								
M4	AVDD_PLL								
E1	AVDD_AFE								
G4	AVSS_MBUFL								
T1	AVSS_PLL								
M1	AVSS_GSMRFRX								
P1	AVSS_RFE								

J3	**AVSS_AFE**								
D1	**AGND**								
A6	**AGND_RF**								
H1	**AGND_AFE**								
K3	**AGND_RFE**								
B10	**AVDD_RTC**		**Supply voltage of real time clock circuitry**						

Table 2 Pin Descriptions (**Bolded** types are functions at reset)

Power Description

NAME	IO Supply	IO GND	Core Supply	Core GND	Remark
AU_MOUTL					
AU_MOUTR					
AU_FMINR					
AU_FMINL					
AU_OUT0_N					
AU_OUT0_P					
AU_MICBIAS_P					
AU_MICBIAS_N					
AU_VREF_PO					
AU_VREF_NI					
AU_VIN0_P					
AU_VIN0_N					
AU_VIN1_N					
AU_VIN1_P					
BDLAQP					
BDLAQN					
BDLAIN					
BDLAIP					
APC					
AUXADIN0					
AUXADIN1					
AUXADIN2					
AUX_REF					
AFC					
AFC_BYP					
BPI_BUS0	VDD33	VSS33	VDDK	VSSK	
BPI_BUS1	VDD33	VSS33	VDDK	VSSK	
BPI_BUS2	VDD33	VSS33	VDDK	VSSK	
BPI_BUS3	VDD33	VSS33	VDDK	VSSK	
BPI_BUS4	VDD33	VSS33	VDDK	VSSK	
BPI_BUS5	VDD33	VSS33	VDDK	VSSK	
BPI_BUS6	VDD33	VSS33	VDDK	VSSK	
BPI_BUS7	VDD33	VSS33	VDDK	VSSK	
BPI_BUS8	VDD33	VSS33	VDDK	VSSK	
BPI_BUS9	VDD33	VSS33	VDDK	VSSK	
BSI_CS0	VDD33	VSS33	VDDK	VSSK	
BSI_DATA	VDD33	VSS33	VDDK	VSSK	
BSI_CLK	VDD33	VSS33	VDDK	VSSK	
DAICLK	VDD33	VSS33	VDDK	VSSK	
DAIPCMOUT	VDD33	VSS33	VDDK	VSSK	
DAIPCMIN	VDD33	VSS33	VDDK	VSSK	
DAIRST	VDD33	VSS33	VDDK	VSSK	
DAISYNC	VDD33	VSS33	VDDK	VSSK	

ALERTER	VDD33	VSS33	VDDK	VSSK	
PWM	VDD33	VSS33	VDDK	VSSK	
JRTCK	VDD33	VSS33	VDDK	VSSK	
JTRST_B	VDD33	VSS33	VDDK	VSSK	
JTCK	VDD33	VSS33	VDDK	VSSK	
JTDI	VDD33	VSS33	VDDK	VSSK	
JTMS	VDD33	VSS33	VDDK	VSSK	
JTDO	VDD33	VSS33	VDDK	VSSK	
LCD_D8	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_D7	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_D6	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_D5	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_D4	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_D3	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_D2	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_D1	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_RSTB	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_WR_B	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_RD_B	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_D0	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_A0	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_CS0_B	VDD33_LCD	VSS33	VDDK	VSSK	
LCD_CS1_B	VDD33_LCD	VSS33	VDDK	VSSK	
EADV_B	VDD33_EMI	VSS33	VDDK	VSSK	
EWAIT	VDD33_EMI	VSS33	VDDK	VSSK	
ECLK	VDD33_EMI	VSS33	VDDK	VSSK	
EA25	VDD33_EMI	VSS33	VDDK	VSSK	
ED0	VDD33_EMI	VSS33	VDDK	VSSK	
ED1	VDD33_EMI	VSS33	VDDK	VSSK	
ED2	VDD33_EMI	VSS33	VDDK	VSSK	
ED3	VDD33_EMI	VSS33	VDDK	VSSK	
ED4	VDD33_EMI	VSS33	VDDK	VSSK	
ED5	VDD33_EMI	VSS33	VDDK	VSSK	
ED6	VDD33_EMI	VSS33	VDDK	VSSK	
ED7	VDD33_EMI	VSS33	VDDK	VSSK	
ED8	VDD33_EMI	VSS33	VDDK	VSSK	
ED9	VDD33_EMI	VSS33	VDDK	VSSK	
ED10	VDD33_EMI	VSS33	VDDK	VSSK	
ED11	VDD33_EMI	VSS33	VDDK	VSSK	
ED12	VDD33_EMI	VSS33	VDDK	VSSK	
ED13	VDD33_EMI	VSS33	VDDK	VSSK	
ED14	VDD33_EMI	VSS33	VDDK	VSSK	
ED15	VDD33_EMI	VSS33	VDDK	VSSK	
ERD_B	VDD33_EMI	VSS33	VDDK	VSSK	

EWR_B	VDD33_EMI	VSS33	VDDK	VSSK	
ECS0_B	VDD33_EMI	VSS33	VDDK	VSSK	
ECS1_B	VDD33_EMI	VSS33	VDDK	VSSK	
ECS2_B	VDD33_EMI	VSS33	VDDK	VSSK	
ECS3_B	VDD33_EMI	VSS33	VDDK	VSSK	
ELB_B	VDD33_EMI	VSS33	VDDK	VSSK	
EUB_B	VDD33_EMI	VSS33	VDDK	VSSK	
EA0	VDD33_EMI	VSS33	VDDK	VSSK	
EA1	VDD33_EMI	VSS33	VDDK	VSSK	
EA2	VDD33_EMI	VSS33	VDDK	VSSK	
EA3	VDD33_EMI	VSS33	VDDK	VSSK	
EA4	VDD33_EMI	VSS33	VDDK	VSSK	
EA5	VDD33_EMI	VSS33	VDDK	VSSK	
EA6	VDD33_EMI	VSS33	VDDK	VSSK	
EA7	VDD33_EMI	VSS33	VDDK	VSSK	
EA8	VDD33_EMI	VSS33	VDDK	VSSK	
EA9	VDD33_EMI	VSS33	VDDK	VSSK	
EA10	VDD33_EMI	VSS33	VDDK	VSSK	
EA11	VDD33_EMI	VSS33	VDDK	VSSK	
EA12	VDD33_EMI	VSS33	VDDK	VSSK	
EA13	VDD33_EMI	VSS33	VDDK	VSSK	
EA14	VDD33_EMI	VSS33	VDDK	VSSK	
EA15	VDD33_EMI	VSS33	VDDK	VSSK	
EA16	VDD33_EMI	VSS33	VDDK	VSSK	
EA17	VDD33_EMI	VSS33	VDDK	VSSK	
EA18	VDD33_EMI	VSS33	VDDK	VSSK	
EA19	VDD33_EMI	VSS33	VDDK	VSSK	
EA20	VDD33_EMI	VSS33	VDDK	VSSK	
EA21	VDD33_EMI	VSS33	VDDK	VSSK	
EA22	VDD33_EMI	VSS33	VDDK	VSSK	
EA23	VDD33_EMI	VSS33	VDDK	VSSK	
EA24	VDD33_EMI	VSS33	VDDK	VSSK	
TESTMODE	VDD33	VSS33	VDDK	VSSK	
SYSRST_B	VDD33	VSS33	VDDK	VSSK	
WATCHDOG	VDD33_EMI	VSS33	VDDK	VSSK	
SRCLKENAI	VDD33	VSS33	VDDK	VSSK	
SRCLKENA	VDD33	VSS33	VDDK	VSSK	
KCOL4	VDD33	VSS33	VDDK	VSSK	
KCOL3	VDD33	VSS33	VDDK	VSSK	
KCOL2	VDD33	VSS33	VDDK	VSSK	
KCOL1	VDD33	VSS33	VDDK	VSSK	
KCOL0	VDD33	VSS33	VDDK	VSSK	
KROW4	VDD33	VSS33	VDDK	VSSK	
KROW3	VDD33	VSS33	VDDK	VSSK	
KROW2	VDD33	VSS33	VDDK	VSSK	
KROW1	VDD33	VSS33	VDDK	VSSK	

KROW0	VDD33	VSS33	VDDK	VSSK	
EINT0	VDD33	VSS33	VDDK	VSSK	
EINT1	VDD33	VSS33	VDDK	VSSK	
EINT2	VDD33	VSS33	VDDK	VSSK	
EINT3	VDD33	VSS33	VDDK	VSSK	
UTXD1	VDD33	VSS33	VDDK	VSSK	
UCTS1_B	VDD33	VSS33	VDDK	VSSK	
URTS1_B	VDD33	VSS33	VDDK	VSSK	
UTXD3	VDD33	VSS33	VDDK	VSSK	
URXD3	VDD33	VSS33	VDDK	VSSK	
URXD2	VDD33	VSS33	VDDK	VSSK	
URXD1	VDD33	VSS33	VDDK	VSSK	
UTXD2	VDD33	VSS33	VDDK	VSSK	
SYSCLK	AVDD_PLL	AVSS_PLL	AVDD_PLL	AVSS_PLL	
XIN	AVDD_RTC	AVSS_RTC	AVDD_RTC	AVSS_RTC	
XOUT	AVDD_RTC	AVSS_RTC	AVDD_RTC	AVSS_RTC	
SIMIO	VSIM				
SIMRST	VSIM				
SIMCLK	VSIM				
CHRIN					
GATEDRV					
LED_B					
LED_G					
LED_R					
LED					
VIBRATOR					
VSIM					3.3/1.8V
VRF					2.8V
VRF_SENSE					
VCORE					1.8/1.5V
VIO					2.8V
VM					2.8/1.8V
VA					2.8V
VCTXO					2.8V
VBAT_RF					
VBAT					
VBAT					
VBAT					
AVBAT					
BAT_BACKUP					
BATDET					

BATSENSE					
ISENSE					
RESET					
RSTCAP					
VREF					
VMSEL					
PWRKEY					
PGND					
DGND					
DGND					
DGND					
DGND					
VSS33					
VSS33					
VSS33					
VSS33					
VSS33					
VSS33_EMI					
VSS33_EMI					
VSS33_EMI					
VSS33_EMI					
VSS33_EMI					
VDDK					TYP 1.8V
VDDK					TYP 1.8V
VDDK					TYP 1.8V
VDDK					TYP 1.8V
VDD33					TYP 2.8V
VDD33					TYP 2.8V
VDD33					TYP 2.8V
VDD33_LCD					2.8V/1.8V
VDD33_EMI					2.8V/1.8V
VDD33_EMI					2.8V/1.8V
VDD33_EMI					2.8V/1.8V
VDD33_EMI					2.8V/1.8V
VDD33_EMI					2.8V/1.8V
AVDD_RFE					
AVDD_MBUFL					
AVDD_GSMRFRX					
AVDD_PLL					
AVDD_AFE					
AVSS_MBUFL					
AVSS_PLL					
AVSS_GSMRFRX					
AVSS_RFE					
AVSS_AFE					
AGND					

AGND_RF					
AGND_AFE					
AGND_RFE					
AVDD_RTC					

Table 3 Power Descriptions

2.4 Digital Pin Electrical Characteristics

Based on I/O power supply (VDD33) = 3.3 V
Vil (max) = 0.8 V
Vih (min) = 2.0 V

Ball	GPIO	Driving(mA)	Pull	Vol at max. Iol	Voh at max. Ioh	PU/PD Resistor(K ohm) (min, typical, max)	Cin(pF)
BPI							
BPI_BUS0		min 2, max 8		0.4	2.4		
BPI_BUS1		min 2, max 8		0.4	2.4		
BPI_BUS2		min 2, max 8		0.4	2.4		
BPI_BUS3		min 2, max 8		0.4	2.4		
BPI_BUS4		2		0.4	2.4		
BPI_BUS5		2		0.4	2.4		
BPI_BUS6	**GPIO20**	2	PD	0.4	2.4		5.2
BPI_BUS7	**GPIO21**	2	PD	0.4	2.4	40, 75, 190	5.2
BPI_BUS8	**GPIO22**	2	PU	0.4	2.4		5.2
BPI_BUS9	**GPIO23**	2	PD	0.4	2.4		5.2
BSI							
BSI_CS0		2		0.4	2.4		
BSI_DATA		2		0.4	2.4		
BSI_CLK		2		0.4	2.4		
DAI							
DAICLK	**GPIO15**	6	PU	0.4	2.4	40, 75, 190	5.2
DAIPCMOUT	**GPIO16**	6	PD	0.4	2.4	40, 75, 190	5.2
DAIPCMIN	**GPIO17**	6	PU	0.4	2.4	40, 75, 190	5.2
DAIRST	**GPIO18**	6	PU	0.4	2.4	40, 75, 190	5.2
DAISYNC	**GPIO19**	6	PU	0.4	2.4	40, 75, 190	5.2
ALERTER	**GPIO24**	4	PD	0.4	2.4	40, 75, 190	5.2
PWM	**GPIO25**	4	PD	0.4	2.4	40, 75, 190	5.2
JTAG							
JRTCK		6	PU	0.4	2.4	40, 75, 190	5.2
JTRST_B	**GPIO26**	2	PD	0.4	2.4	40, 75, 190	5.2
JTCK		input only	PU			40, 75, 190	5.2

JTDI	**GPIO27**	2	PU	0.4	2.4	40, 75, 190	5.2
JTMS	**GPIO28**	2	PU	0.4	2.4	40, 75, 190	5.2
JTDO		6	PU	0.4	2.4	40, 75, 190	5.2
SYSRST_B		input only	PU			40, 75, 190	5.2
LCD							
LCD_D8	**GPIO0**	max 16, min 2	PD	0.4	2.4	40, 75, 190	5.2
LCD_D7	**GPIO1**	max 16, min 2	PD	0.4	2.4	40, 75, 190	5.2
LCD_D6	**GPIO2**	max 16, min 2	PD	0.4	2.4	40, 75, 190	5.2
LCD_D5	**GPIO3**	max 16, min 2	PD	0.4	2.4	40, 75, 190	5.2
LCD_D4	**GPIO4**	max 16, min 2	PD	0.4	2.4	40, 75, 190	5.2
LCD_D3	**GPIO5**	max 16, min 2	PD	0.4	2.4	40, 75, 190	5.2
LCD_D2	**GPIO6**	max 16, min 2	PD	0.4	2.4	40, 75, 190	5.2
LCD_D1	**GPIO7**	max 16, min 2	PD	0.4	2.4	40, 75, 190	5.2
LCD_RSTB	**GPIO8**	max 16, min 2	PU	0.4	2.4	40, 75, 190	5.2
LCD_WR_B	**GPIO9**	max 16, min 2	PU	0.4	2.4	40, 75, 190	5.2
LCD_RD_B	**GPIO10**	max 16, min 2	PU	0.4	2.4	40, 75, 190	5.2
LCD_D0	**GPIO11**	max 16, min 2	PD	0.4	2.4	40, 75, 190	5.2
LCD_A0	**GPIO12**	max 16, min 2	PU	0.4	2.4	40, 75, 190	5.2
LCD_CS0_B	**GPIO13**	max 16, min 2	PU	0.4	2.4	40, 75, 190	5.2
LCD_CS1_B	**GPIO14**	max 16, min 2	PU	0.4	2.4	40, 75, 190	5.2
WATCHDOG	**GPIO29**	4		0.4	VMEM – 0.4		5.2
EMI							
EADV_B		max 16, min 2		0.4	VMEM – 0.4		
EWAIT		max 16, min 2	PU	0.4	VMEM – 0.4	40, 75, 190	
ECLK		max 16, min 2		0.4	VMEM – 0.4		
ECRE		max 16, min 2		0.4	VMEM – 0.4		
ED0		max 16, min 2		0.4	VMEM – 0.4		5.2
ED1		max 16, min 2		0.4	VMEM – 0.4		5.2
ED2		max 16, min 2		0.4	VMEM – 0.4		5.2
ED3		max 16, min 2		0.4	VMEM – 0.4		5.2
ED4		max 16, min 2		0.4	VMEM – 0.4		5.2
ED5		max 16, min 2		0.4	VMEM – 0.4		5.2
ED6		max 16, min 2		0.4	VMEM – 0.4		5.2
ED7		max 16, min 2		0.4	VMEM – 0.4		5.2
ED8		max 16, min 2		0.4	VMEM – 0.4		5.2
ED9		max 16, min 2		0.4	VMEM – 0.4		5.2
ED10		max 16, min 2		0.4	VMEM – 0.4		5.2
ED11		max 16, min 2		0.4	VMEM – 0.4		5.2
ED12		max 16, min 2		0.4	VMEM – 0.4		5.2
ED13		max 16, min 2		0.4	VMEM – 0.4		5.2
ED14		max 16, min 2		0.4	VMEM – 0.4		5.2
ED15		max 16, min 2		0.4	VMEM – 0.4		5.2
ERD_B		max 16, min 2		0.4	VMEM – 0.4		

EWR_B		max 16, min 2		0.4	VMEM – 0.4		
ECS0_B		max 16, min 2		0.4	VMEM – 0.4		
ECS1_B		max 16, min 2		0.4	VMEM – 0.4		
ECS2_B		max 16, min 2		0.4	VMEM – 0.4		
ECS3_B	**GPI52**	max 16, min 2	PU	0.4	VMEM – 0.4	40, 75, 190	
ELB_B		max 16, min 2		0.4	VMEM – 0.4		
EUB_B		max 16, min 2		0.4	VMEM – 0.4		
EA0	**GPIO30**	max 16, min 2	PD	0.4	VMEM – 0.4	40, 75, 190	
EA1		max 16, min 2		0.4	VMEM – 0.4		
EA2		max 16, min 2		0.4	VMEM – 0.4		
EA3		max 16, min 2		0.4	VMEM – 0.4		
EA4		max 16, min 2		0.4	VMEM – 0.4		
EA5		max 16, min 2		0.4	VMEM – 0.4		
EA6		max 16, min 2		0.4	VMEM – 0.4		
EA7		max 16, min 2		0.4	VMEM – 0.4		
EA8		max 16, min 2		0.4	VMEM – 0.4		
EA9		max 16, min 2		0.4	VMEM – 0.4		
EA10		max 16, min 2		0.4	VMEM – 0.4		
EA11		max 16, min 2		0.4	VMEM – 0.4		
EA12		max 16, min 2		0.4	VMEM – 0.4		
EA13		max 16, min 2		0.4	VMEM – 0.4		
EA14		max 16, min 2		0.4	VMEM – 0.4		
EA15		max 16, min 2		0.4	VMEM – 0.4		
EA16		max 16, min 2		0.4	VMEM – 0.4		
EA17		max 16, min 2		0.4	VMEM – 0.4		
EA18		max 16, min 2		0.4	VMEM – 0.4		
EA19		max 16, min 2		0.4	VMEM – 0.4		
EA20		max 16, min 2		0.4	VMEM – 0.4		
EA21		max 16, min 2		0.4	VMEM – 0.4		
EA22		max 16, min 2		0.4	VMEM – 0.4		
EA23		max 16, min 2		0.4	VMEM – 0.4		
EA24		max 16, min 2		0.4	VMEM – 0.4		
SRCLKENAI	**GPIO31**	2	PD	0.4	2.4	40, 75, 190	5.2
SRCLKENA		2		0.4	2.4		
Key pad							
KCOL4	**GPIO32**	6	PU	0.4	2.4	40, 75, 190	5.2
KCOL3	**GPIO33**	6	PU	0.4	2.4	40, 75, 190	5.2
KCOL2	**GPIO34**	6	PU	0.4	2.4	40, 75, 190	5.2
KCOL1	**GPIO35**	6	PU	0.4	2.4	40, 75, 190	5.2
KCOL0	**GPIO36**	6	PU	0.4	2.4	40, 75, 190	5.2
KROW4	**GPIO37**	6		0.4	2.4		5.2
KROW3	**GPIO38**	6		0.4	2.4		5.2
KROW2	**GPIO39**	6		0.4	2.4		5.2

KROW1	**GPIO40**	2		0.4	2.4		5.2
KROW0	**GPIO41**	2		0.4	2.4		5.2
EINT							
EINT0		input only	PU			40, 75, 190	5.2
EINT1		input only	PU			40, 75, 190	5.2
EINT2	**GPIO42**	2	PU	0.4	2.4	40, 75, 190	5.2
EINT3	**GPIO43**	2	PU	0.4	2.4	40, 75, 190	5.2
UART							
UTXD1	**GPIO44**	2	PU	0.4	2.4	40, 75, 190	5.2
UCTS1_B	**GPIO45**	2	PU	0.4	2.4	40, 75, 190	5.2
URTS1_B	**GPIO46**	2	PU	0.4	2.4	40, 75, 190	5.2
UTXD3	**GPIO47**	2	PU	0.4	2.4	40, 75, 190	5.2
URXD3	**GPIO48**	2	PU	0.4	2.4	40, 75, 190	5.2
URXD2	**GPIO49**	2	PU	0.4	2.4	40, 75, 190	5.2
URXD1	**GPIO50**	2	PU	0.4	2.4	40, 75, 190	5.2
UTXD2	**GPIO51**	2	PU	0.4	2.4	40, 75, 190	5.2

3 Micro-Controller Unit Subsystem

Figure 5 illustrates the block diagram of the Micro-Controller Unit Subsystem in MT6223. The subsystem utilizes a main 32-bit ARM7EJ-S RISC processor, which plays the role of the main bus master controlling the whole subsystem. The processor communicates with all the other on-chip modules via the two-level system buses: AHB Bus and APB Bus. All bus transactions originate from bus masters, while slaves can only respond to requests from bus masters. Before data transfer can be established, bus master must ask for bus ownership. This is accomplished by request-grant handshaking protocol between masters and arbiters.

The bus comprises of two-level system buses: Advanced High-Performance Bus (AHB) and Advanced Peripheral Bus (APB). All bus transactions originate from bus masters, while slaves can only respond to requests from bus masters. Before data transfer can be established, the bus master must ask for bus ownership, accomplished by request-grant handshaking protocol between masters and arbiters.

Two levels of bus hierarchy are designed to provide optimum usage for different performance requirements. Specifically, AHB Bus, the main system bus, is tailored toward high-speed requirements and provides 32-bit data path with multiplex scheme for bus interconnections. The APB Bus, on the other hand, is designed to reduce interface complexity for lower data transfer rate, and so it is isolated from high bandwidth AHB Bus by APB Bridge. APB Bus supports 16-bit addressing and both 16-bit and 32-bit data paths. APB Bus is also optimized for minimal power consumption by turning off the clock when there is no APB bus activity.

During operation, if the target slave is located on AHB Bus, the transaction is conducted directly on AHB Bus. However, if the target slave is a peripheral and is attached to the APB bus, then the transaction is conducted between AHB and APB bus through the use of APB Bridge.

The MT6223 MCU subsystem supports only memory addressing method. Therefore all components are mapped onto the MCU 32-bit address space. A Memory Management Unit is employed to allow for a central decode scheme. The MMU generates appropriate selection signals for each memory-addressed module on the AHB Bus.

In order to off-load the processor core, a DMA Controller is designated to act as a master and share the bus resources on AHB Bus to do fast data movement between modules. This controller comprises thirteen DMA channels.

The Interrupt Controller provides a software interface to manipulate interrupt events. It can handle up to 32 interrupt sources asserted at the same time. In general, it generates 2 levels of interrupt requests, FIQ and IRQ, to the processor.

A 40K Byte SRAM is provided as system memory for high-speed data access. For factory programming purposes, a Boot ROM module is also integrated. These two modules use the same Internal Memory Controller to connect to AHB Bus.

External Memory Interface supports both 8-bit and 16-bit devices. Since AHB Bus is 32-bit wide, all the data transfer will be converted into several 8-bit or 16-bit cycles depending on the data width of target device. Note that, this interface is specific to both synchronous and asynchronous components, like Flash, SRAM and parallel LCD. This interface supports also page and burst mode type of Flash.

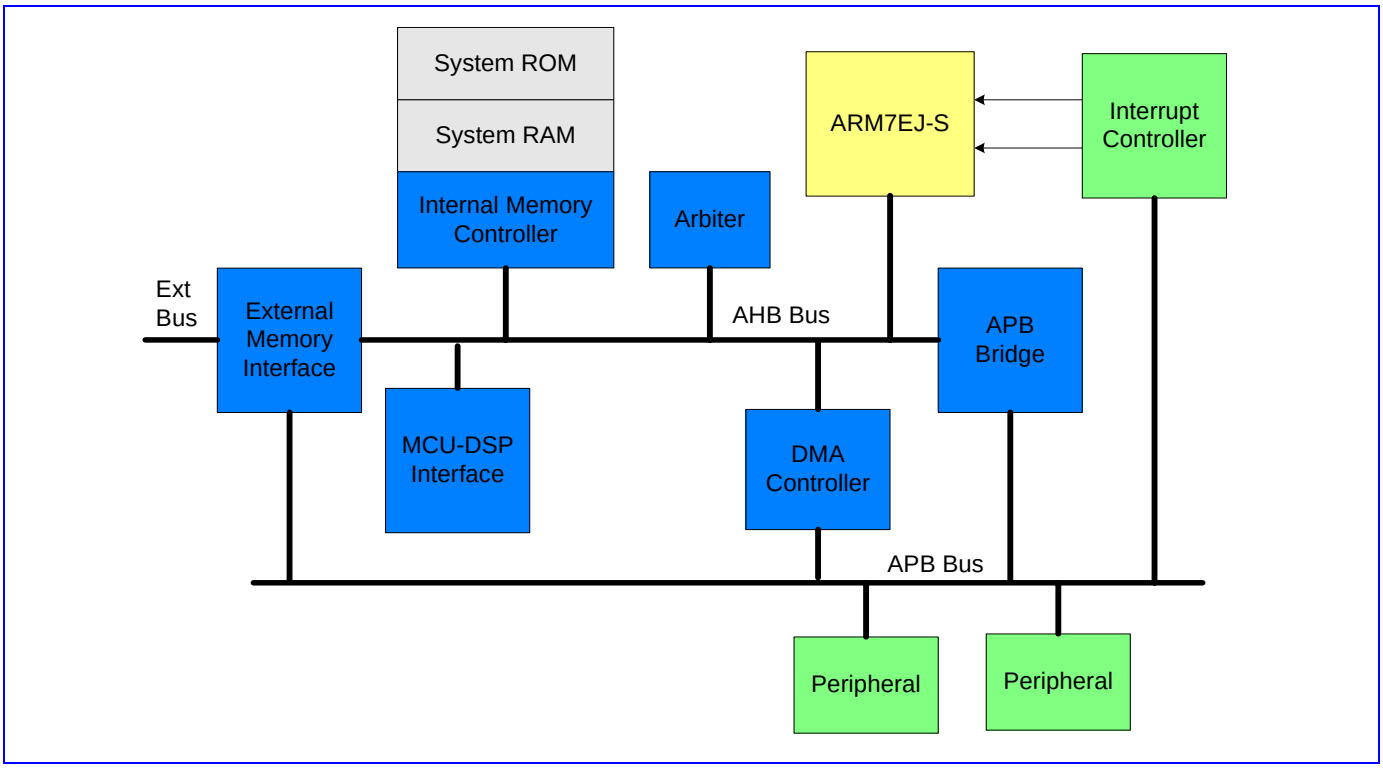


Figure 5 Block Diagram of the Micro-Controller Unit Subsystem in MT6223

3.1 Processor Core

3.1.1 General Description

The Micro-Controller Unit Subsystem in MT6223 is built up with a 32-bit RISC core, ARM7EJ-S that is based on Von Neumann architecture with a single 32-bit data bus carrying both instructions and data. The memory interface of ARM7EJ-S is totally compliant to AMBA based bus system. Basically, it can be connected to AHB Bus directly.

3.2 Memory Management

3.2.1 General Description

The processor core of MT6223, ARM7EJ-S, supports only memory addressing method for instruction fetch and data access. It manages a 32-bit address space that has addressing capability up to 4GB. System RAM, System ROM, Registers, MCU Peripherals and external components are all mapped onto such 32-bit address space, as depicted in **Figure 6**.

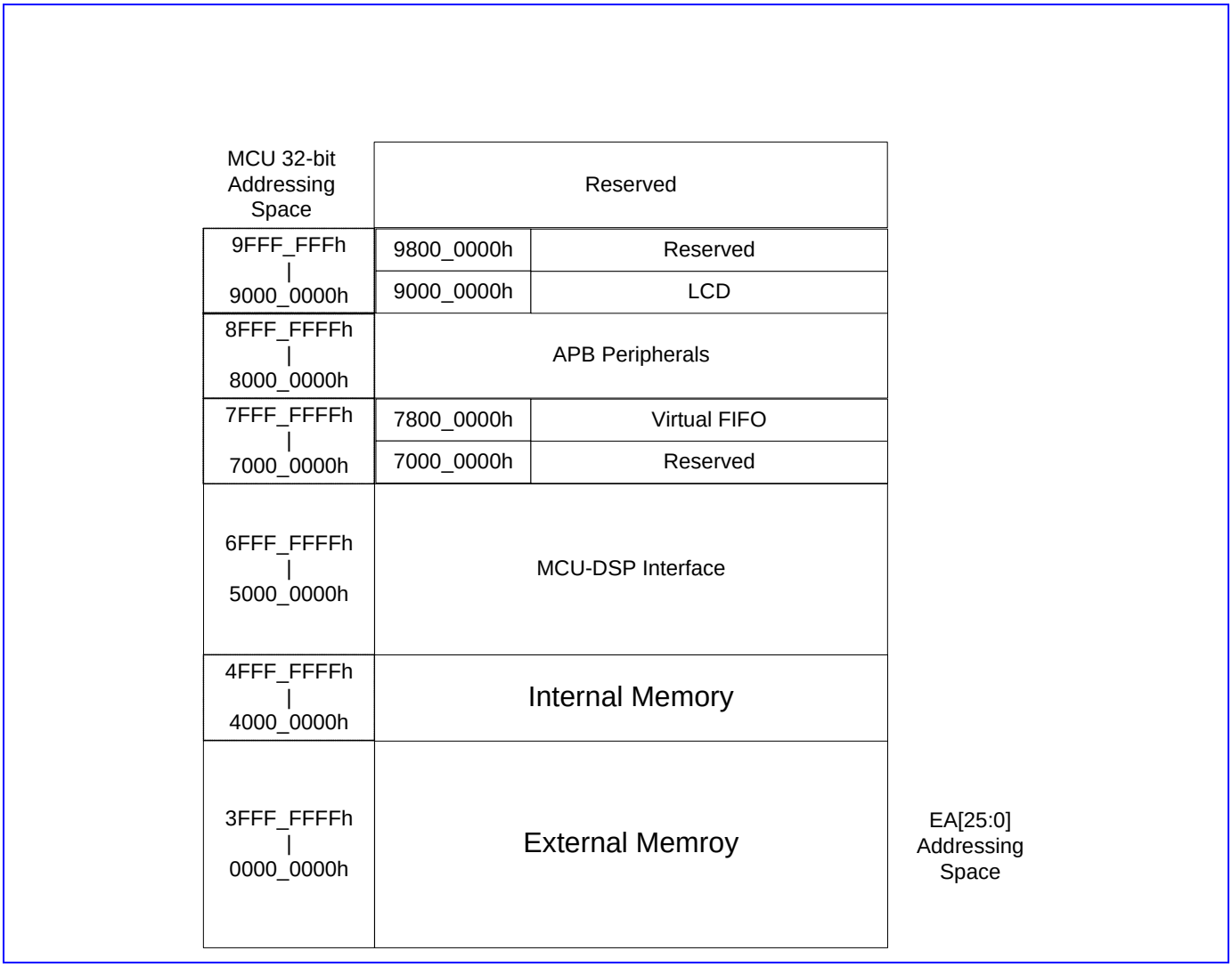


Figure 6 The Memory Layout of MT6223

The address space is organized as basis of blocks with size of 256M Bytes for each. Memory blocks MB0-MB9 are determined and currently dedicated to specific functions, as shown in **Table 4**, while the others are reserved for future usage. Essentially, the block number is uniquely selected by address line A31-A28 of internal system bus.

Memory Block	Block Address A31-A28	Address Range	Description
MB0	0h	00000000h-07FFFFFFh	Boot Code, EXT SRAM or EXT Flash/MISC
		08000000h-0FFFFFFFh	EXT SRAM or EXT Flash/MISC
MB1	1h	10000000h-17FFFFFFh	EXT SRAM or EXT Flash/MISC
		18000000h-1FFFFFFFh	EXT SRAM or EXT Flash/MISC
MB2	2h	20000000h-27FFFFFFh	Reserved
		28000000h-2FFFFFFFh	Reserved
MB3	3h	30000000h-37FFFFFFh	Reserved

		38000000h-3FFFFFFFh	Reserved
MB4	4h	40000000h-47FFFFFFh	System RAM
		48000000h-4FFFFFFFh	System ROM
MB5	5h	50000000h-5FFFFFFFh	MCU-DSP Interface
MB6	6h	60000000h-6FFFFFFFh	
MB7	7h	70000000h-77FFFFFFh	Reserved
		78000000h-7FFFFFFFh	Virtual FIFO
MB8	8h	80000000h-8FFFFFFFh	APB Slaves
MB9	9h	90000000h-97FFFFFFh	LCD
		98000000h-9FFFFFFFh	Reserved

Table 4 Definitions of Memory Blocks in MT6223

3.2.1.1 External Access

To have external access, the MT6223 outputs 26 bits (A25-A0) of address lines along with 4 selection signals that correspond to associated memory blocks. That is, MT6223 can support at most 4 MCU addressable external components. The data width of internal system bus is fixed as 32-bit wide, while the data width of the external components is fixed as 16 bit.

Since devices are usually available with variety operating grades, adaptive configurations for different applications are needed. MT6223 provides software programmable registers to configure to adapt operating conditions in terms of different wait-states.

3.2.1.2 Memory Re-mapping Mechanism

To permit system being configured with more flexible, a memory re-mapping mechanism is provided. It allows software program to swap BANK0 (ECS0#) and BANK1 (ECS1#) dynamically. Whenever the bit value of RM0 in register EMI_REMAP is changed, these two banks will be swapped accordingly. Besides, it also permits system being boot in different sequence as detailed in 3.2.1.3 Boot Sequence.

3.2.1.3 Boot Sequence

Since the ARM7EJ-S core always starts to fetch instructions from the lowest memory address at 00000000h after system has been reset, the system is designed to have a dynamic mapping architecture capable of associating Boot Code, external Flash or external SRAM with the memory block 0000_0000h – 07ff_ffffh.

By default, the Boot Code is mapped onto 0000_0000h – 07ff_ffffh after a system reset. In this special boot mode, External Memory Controller does not access external memory; instead, the EMI Controller send predefined Boot Code back to the ARM7EJS-S core, which instructs the processor to execute the program in System ROM. This configuration can be changed by programming bit value of RM1 in register EMI_REMAP directly.

MT6223 system provides one boot up scheme:

- Start up system of running codes from Boot Code for factory programming.

3.2.1.3.1 Boot Code

The Boot Code is placed together with Memory Re-Mapping Mechanism in External Memory Controller, and comprises of just two words of instructions as shown below. A jump instruction leads the processor to run the code starting at address

48000000h where the System ROM is placed.

ADDRESS	BINARY CODE	ASSEMBLY
00000000h	E51FF004h	LDR PC, 0x4
00000004h	48000000h	(DATA)

3.2.1.3.2 Factory Programming

The configuration for factory programming is shown in **Figure 7**. Usually the Factory Programming Host connects with MT6223 by way of UART interface. To have it works properly, the system should boot up from Boot Code. The down load speed can be up to 921K bps while MCU is running at 26MHz.

After system being reset, the Boot Code will guide the processor to run the Factory Programming software placed in System ROM. Then, MT6223 will start and continue to poll the UART1 port until valid information is detected. The first information received on the UART1 will be used to configure the chip for factory programming. The Flash down loader program is then transferred into System RAM or external SRAM.

Further information will be detailed in MT6223 Software Programming Specification.

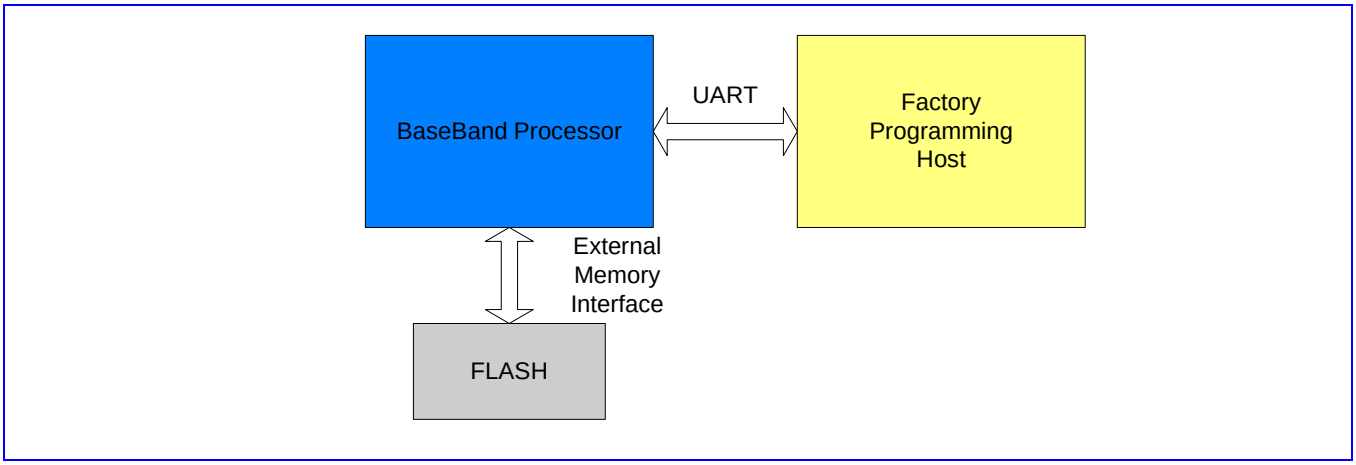


Figure 7 System configuration required for factory programming

3.2.1.4 Little Endian Mode

The MT6223 system always treats 32-bit words of memory in Little Endian format. In Little Endian mode, the lowest numbered byte in a word is stored in the least significant byte, and the highest numbered byte in the most significant position. Byte 0 of the memory system is therefore connected to data lines 7 through 0.

3.3 Bus System

3.3.1 General Description

Two levels of bus hierarchy are employed in constructing the Micro-Controller Unit Subsystem of MT6223. As depicted in **Figure 5**, AHB Bus and APB Bus serve for system backbone and peripheral buses, while an APB bridge connects these two buses. Both AHB and APB Buses operate at the same clock rate as processor core.

The APB Bridge is the only bus master resided on the APB bus. All APB slaves are mapped onto memory block MB8 in MCU 32-bit addressing space. A central address decoder is implemented inside the bridge to generate those select signals for individual peripheral. In addition, since the base address of each APB slave has been associated with select signals, the address bus on APB will contain only the value of offset address.

The maximum address space that can be allocated to a single APB slave is 64KB, i.e. 16-bit address lines. The width of data

bus is mainly constrained to 16-bit to minimize the design complexity and power consumption while some of them uses 32-bit data bus to accommodate more bandwidth. In the case where an APB slave needs large amount of transfers, the device driver can also request a DMA resource or channel to conduct a burst of data transfer. The base address and data width of each peripheral are listed in **Table 5**.

Base Address	Description	Data Width	Software Base ID
8000_0000h	Configuration Registers (Clock, Power Down, Version and Reset)	16	CONFG Base
8001_0000h	External Memory Interface	32	EMI Base
8002_0000h	Interrupt Controller	32	CIRQ Base
8003_0000h	DMA Controller	32	DMA Base
8004_0000h	Reset Generation Unit	16	RGU Base
8005_0000h	Reserved		
8006_0000h	GPRS Cipher Unit	32	GCU Base
8007_0000h	I2C	16	I2C Base
8008_0000h	Reserved		
8009_0000h	Software Debug	32	SWDBG base
8010_0000h	General Purpose Timer	16	GPT Base
8011_0000h	Keypad Scanner	16	KP Base
8012_0000h	General Purpose Inputs/Outputs	16	GPIO Base
8013_0000h	UART 1	16	UART1 Base
8014_0000h	SIM Interface	16	SIM Base
8015_0000h	Pulse-Width Modulation Outputs	16	PWM Base
8016_0000h	Alerter Interface	16	ALTER Base
8017_0000h	Security Engine for JTAG protection	32	SEJ Base
8018_0000h	UART 2	16	UART2 Base
8019_0000h	Reserved		
801a_0000h	Reserved		
801b_0000h	UART 3	16	UART3 Base
801c_0000h	Reserved		
8020_0000h	TDMA Timer	32	TDMA Base
8021_0000h	Real Time Clock	16	RTC Base

8022_0000h	Base-Band Serial Interface	32	BSI Base
8023_0000h	Base-Band Parallel Interface	16	BPI Base
8024_0000h	Automatic Frequency Control Unit	16	AFC Base
8025_0000h	Automatic Power Control Unit	32	APC Base
8026_0000h	Frame Check Sequence	16	FCS Base
8027_0000h	Auxiliary ADC Unit	16	AUXADC Base
8028_0000h	Divider/Modulus Coprocessor	32	DIVIDER Base
8029_0000h	CSD Format Conversion Coprocessor	32	CSD_ACC Base
802a_0000h	Reserved		
8030_0000h	MCU-DSP Shared Register 1	16	SHARE1 Base
8031_0000h	DSP Patch Unit 1	16	PATCH1 Base
8032_0000h	MCU-DSP Shared Register 2	16	SHARE2 Base
8033_0000h	DSP Patch Unit 2	16	PATCH2 Base
8040_0000h	Audio Front End	16	AFE Base
8041_0000h	Base-Band Front End	16	BFE Base
8050_0000h	Analog Chip Interface Controller	16	MIXED Base

Table 5 Register Base Addresses for MCU Peripherals

REGISTER ADDRESS	REGISTER NAME	SYNONYM
CONFG + 0000h	Hardware Version Register	HW_VER
CONFG + 0004h	Software Version Register	SW_VER
CONFG + 0008h	Hardware Code Register	HW_CODE
CONFG + 0404h	APB Bus Control Register	APB_CON
CONFG + 0500h	AHB Bus Control Register	AHB_CON

Table 6 APB Bridge Register Map

3.3.2 Register Definitions

CONFG+0000h Hardware Version Register HW_VERSION

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXTP				MAJREV				MINREV							
Type	RO				RO				RO				RO			

Reset	8	A	0	0

This register is used by software to determine the hardware version of the chip. The register contains a new value whenever each metal fix or major step is performed. All values are incremented by a step of 1.

MINREV Minor Revision of the chip

MAJREV Major Revision of the chip

EXTP This field shows the existence of Hardware Code Register that presents the Hardware ID while the value is other than zero.

CONFG+0004h Software Version Register SW_VERSION

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXTP				MAJREV				MINREV							
Type	RO				RO				RO				RO			
Reset	8				A				0				0			

This register is used by software to determine the software version used with this chip. All values are incremented by a step of 1.

MINREV Minor Revision of the software

MAJREV Major Revision of the software

EXTP This field shows the existence of Hardware Code Register that presents the Hardware ID when the value is other than zero.

CONFG+0008h Hardware Code Register HW_CODE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CODE3				CODE2				CODE1				CODE0			
Type	RO				RO				RO				RO			
Reset	6				2				2				3			

This register presents the Hardware ID.

CODE This version of chip is coded as 6223h.

CONFG+0404h APB Bus Control Register APB_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		APBW6		APBW4	APBW3	APBW2	APBW1	APBW0		APBR6		APBR4	APBR3	APBR2	APBR1	APBR0
Type		R/W		R/W	R/W	R/W	R/W	R/W		R/W		R/W	R/W	R/W	R/W	R/W
Reset		0		0	0	0	0	0		1		1	1	1	1	1

This register is used to control the timing of Read Cycle and Write Cycle on APB Bus. Note that APB Bridge 5 is different from other bridges. The access time is varied, and access is not completed until acknowledge signal from APB slave is asserted.

APBR0-APBR6 Read Access Time on APB Bus

0 1-Cycle Access

1 2-Cycle Access

APBW0-APBW6 Write Access Time on APB Bus

0 1-Cycle Access

1 2-Cycle Access

CONFG+0500h AHB Bus Control Register AHB_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EMI
Type																R/W
Reset																0

EMI Control the AHB-EMI interface

0 latch mode. In order to meet bus timing constraints, Additional stage of registers are inserted between AHB and EMI. While running at 52MHz, AHB-EMI interface must be set as latch mode..

1 direct couple mode. AHB and EMI are directly coupled. While running at 26MHz, AHB-EMI interface must be set as direct couple mode for better bus efficiency.

3.4 Direct Memory Access

3.4.1 General Description

A generic DMA Controller is placed on Layer 2 AHB Bus to support fast data transfers and to off-load the processor. With this controller, specific devices on AHB or APB buses can benefit greatly from quick completion of data movement from or to memory modules such as Internal System RAM or External SRAM. Such Generic DMA Controller can also be used to connect any two devices other than memory module as long as they can be addressed in memory space.

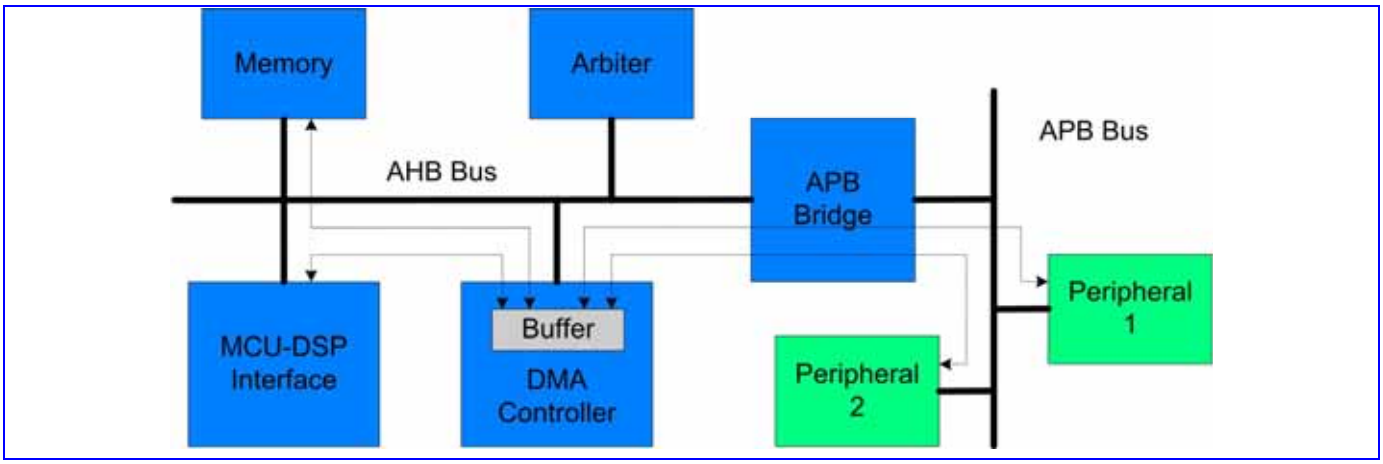


Figure 8 Variety Data Paths of DMA Transfers

Up to fourteen channels of simultaneous data transfers are supported. Each channel has a similar set of registers to be configured to different scheme as desired. If more than fourteen devices are requesting the DMA resources at the same time, software based arbitration should be employed. Once the service candidate is decided, the responsible device driver should configure the Generic DMA Controller properly in order to conduct DMA transfers. Both Interrupt and Polling based schemes in handling the completion event are supported. The block diagram of such generic DMA Controller is illustrated in the following figure.

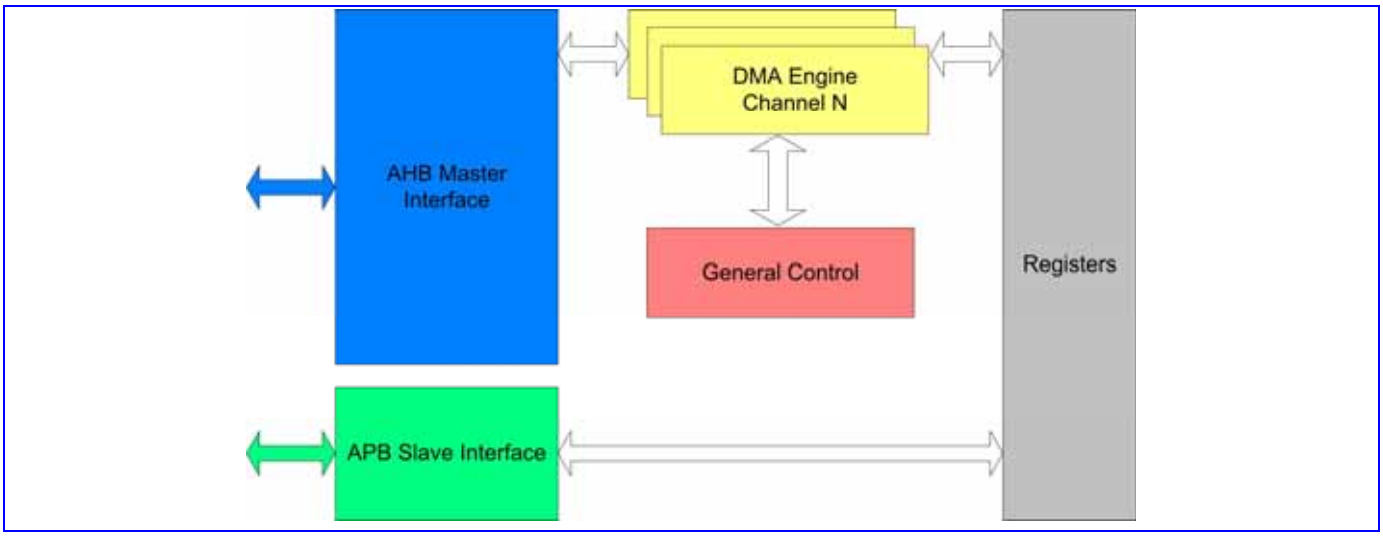


Figure 9 Block Diagram of Direct memory Access Module

3.4.1.1 Full-Size & Half-Size DMA Channels

There are three types of DMA channels in the DMA controller. The first one is called a full-size DMA channel, the second one is called a half-size DMA channel, and the last is Virtual FIFO DMA. Channels 1 is full-size DMA channels; channels 4 through 8 are half-size ones; and channels 11 through 14 are Virtual FIFO DMAs. The difference between the first two types of DMA channels is that both source and destination address are programmable in full-size DMA channels, but only the address of one side can be programmed in half-size DMA channel. In half-size channels, only either the source or destination address can be programmed, while the addresses of the other side is preset. Which preset address is used depends on the setting of MAS in DMA Channel Control Register. Refer to the Register Definition section for more detail.

3.4.1.2 Ring Buffer & Double Buffer Memory Data Movement

DMA channels 1 and 4 through 6 support ring-buffer and double-buffer memory data movement. This can be achieved by programming DMA_WPPT and DMA_WPTO, as well as setting WPEN in DMA_CON register to enable. The following figure shows how the function works. Once the transfer counter reaches the value of WPPT, the next address jumps to the WPTO address after completing the WPPT data transfer. Note that only one side can be configured as ring-buffer or double-buffer memory, and this is controlled by WPSD in DMA_CON register.

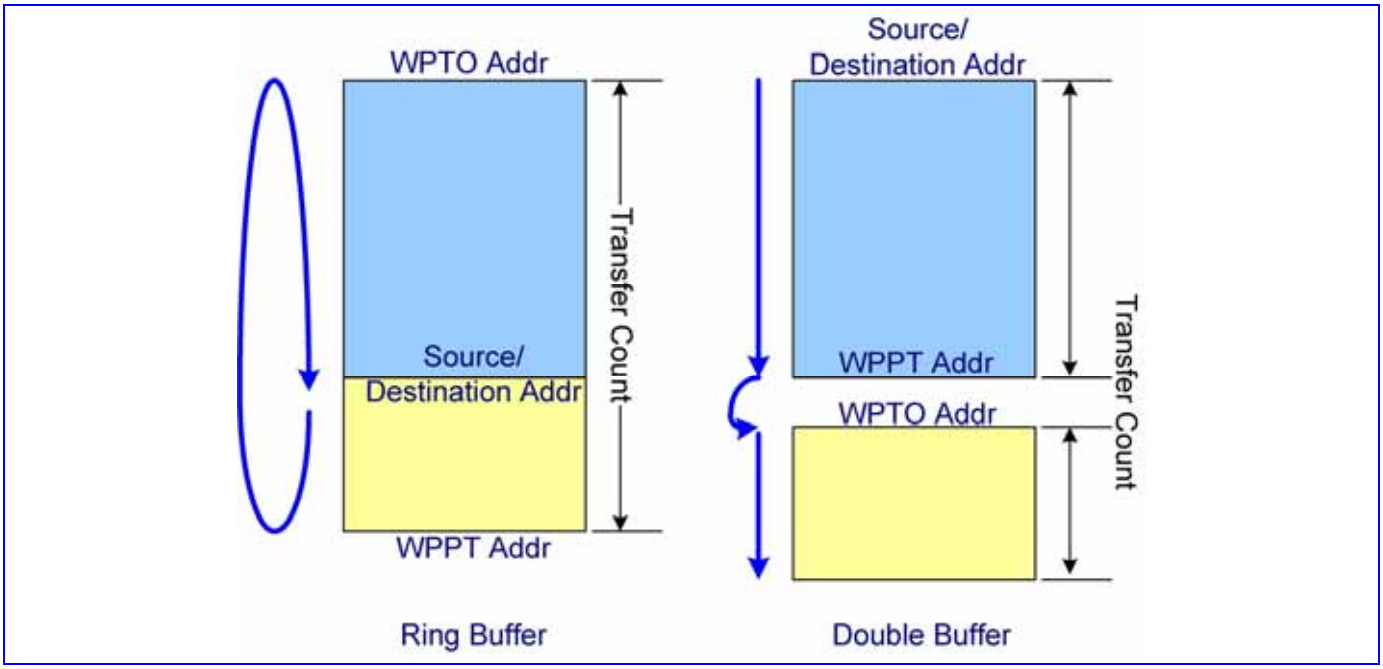


Figure 10 Ring Buffer and Double Buffer Memory Data Movement

3.4.1.3 Unaligned Word Access

The address of word access on AHB bus must be aligned to word boundary, or the 2 LSB is truncated to 00b. If programmers do not notice this, it may cause an incorrect data fetch. In the case where data is to be moved from unaligned addresses to aligned addresses, the word is usually first split into four bytes and then moved byte by byte. This results in four read and four write transfers on the bus.

To improve bus efficiency, unaligned-word access is provided in DMA4~8. While this function is enabled, DMAs move data from unaligned address to aligned address by executing four continuous byte-read access and one word-write access, reducing the number of transfers on the bus by three.

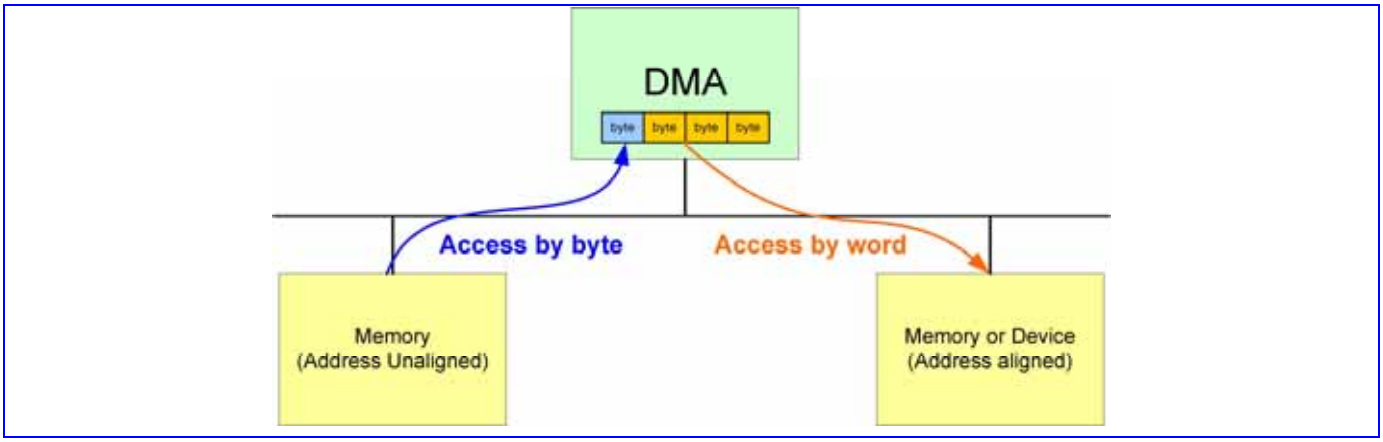


Figure 11 Unaligned Word Accesses

3.4.1.4 Virtual FIFO DMA

Virtual FIFO DMA is used to ease UART control. The difference between the Virtual FIFO DMAs and the ordinary DMAs is that Virtual FIFO DMA contains additional FIFO controller. The read and write pointers are kept in the Virtual FIFO DMA. During a read from the FIFO, the read pointer points to the address of the next data. During a write to the FIFO, the write pointer moves to the next address. If the FIFO is empty, a FIFO read is not allowed. Similarly, data is not written into the FIFO if the FIFO is full. Due to UART flow control requirements, an alert length is programmed. Once the FIFO

Space is less than this value, an alert signal is issued to enable UART flow control. The type of flow control performed depends on the setting in UART.

Each Virtual FIFO DMA can be programmed as RX or TX FIFO. This depends on the setting of DIR in DMA_CON register. If DIR is "0"(READ), it means TX FIFO. On the other hand, if DIR is "1"(WRITE), the Virtual FIFO DMA is specified as a RX FIFO.

Virtual FIFO DMA provides an interrupt to MCU. This interrupt informs MCU that there is data in the FIFO, and the amount of data is over or under the value defined in DMA_COUNT register. With this, MCU does not need to poll DMA to know when data must be removed from or put into the FIFO.

Note that Virtual FIFO DMAs cannot be used as generic DMAs, i.e. DMA1 and DMA4~8.

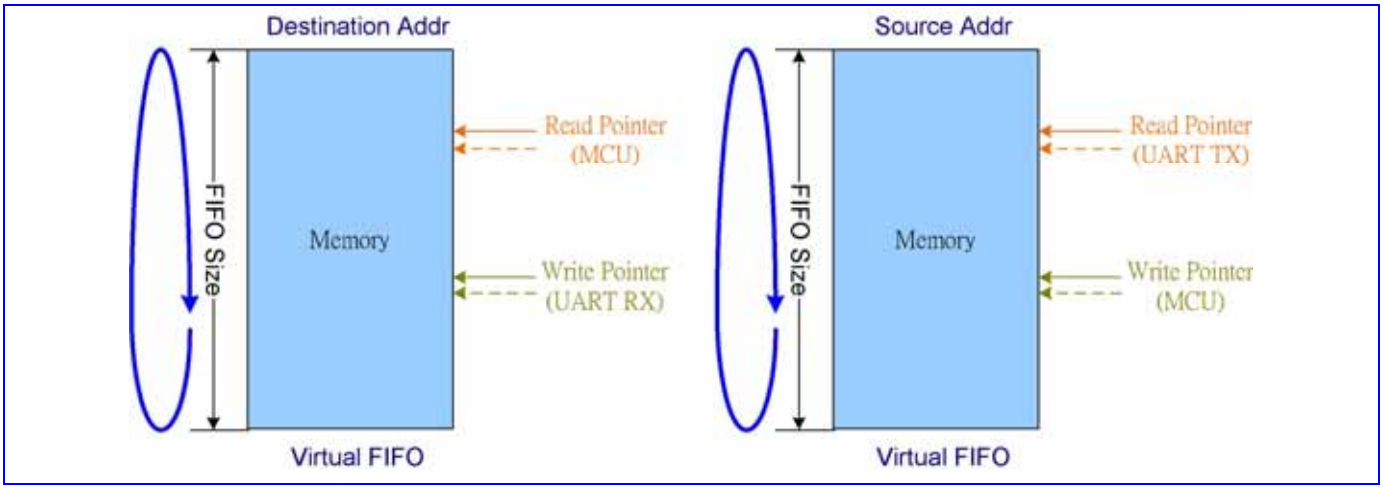


Figure 12 Virtual FIFO DMA

DMA number	Address of Virtual FIFO Access Port	Associated UART
DMA11	7800_0000h	UART1 RX / ALL UART TX
DMA12	7800_0100h	UART2 RX / ALL UART TX
DMA13	7800_0200h	UART3 RX / ALL UART TX
DMA14	7800_0300h	ALL UART TX

Table 7 Virtual FIFO Access Port

DMA number	Type	Ring Buffer	Two Buffer	Burst Mode	Unaligned Word Access
DMA1	Full Size	●	●	●	
DMA4	Half Size	●	●	●	●
DMA5	Half Size	●	●	●	●
DMA6	Half Size	●	●	●	●
DMA7	Half Size	●	●	●	●
DMA8	Half Size	●	●	●	●

DMA11	Virtual FIFO	●			
DMA12	Virtual FIFO	●			
DMA13	Virtual FIFO	●			
DMA14	Virtual FIFO	●			

Table 8 Function List of DMA channels

REGISTER ADDRESS	REGISTER NAME	SYNONYM
DMA + 0000h	DMA Global Status Register	DMA_GLBSTA
DMA + 0028h	DMA Global Bandwidth Limiter Register	DMA_GLBLIMITER
DMA + 0100h	DMA Channel 1 Source Address Register	DMA1_SRC
DMA + 0104h	DMA Channel 1 Destination Address Register	DMA1_DST
DMA + 0108h	DMA Channel 1 Wrap Point Address Register	DMA1_WPPT
DMA + 010Ch	DMA Channel 1 Wrap To Address Register	DMA1_WPTO
DMA + 0110h	DMA Channel 1 Transfer Count Register	DMA1_COUNT
DMA + 0114h	DMA Channel 1 Control Register	DMA1_CON
DMA + 0118h	DMA Channel 1 Start Register	DMA1_START
DMA + 011Ch	DMA Channel 1 Interrupt Status Register	DMA1_INTSTA
DMA + 0120h	DMA Channel 1 Interrupt Acknowledge Register	DMA1_ACKINT
DMA + 0124h	DMA Channel 1 Remaining Length of Current Transfer	DMA1_RLCT
DMA + 0128h	DMA Channel 1 Bandwidth Limiter Register	DMA1_LIMITER
DMA + 0408h	DMA Channel 4 Wrap Point Address Register	DMA4_WPPT
DMA + 040Ch	DMA Channel 4 Wrap To Address Register	DMA4_WPTO
DMA + 0410h	DMA Channel 4 Transfer Count Register	DMA4_COUNT
DMA + 0414h	DMA Channel 4 Control Register	DMA4_CON
DMA + 0418h	DMA Channel 4 Start Register	DMA4_START
DMA + 041Ch	DMA Channel 4 Interrupt Status Register	DMA4_INTSTA
DMA + 0420h	DMA Channel 4 Interrupt Acknowledge Register	DMA4_ACKINT
DMA + 0424h	DMA Channel 4 Remaining Length of Current Transfer	DMA4_RLCT
DMA + 0428h	DMA Channel 4 Bandwidth Limiter Register	DMA4_LIMITER
DMA + 042Ch	DMA Channel 4 Programmable Address Register	DMA4_PGMADDR

DMA + 0508h	DMA Channel 5 Wrap Point Address Register	DMA5_WPPT
DMA + 050Ch	DMA Channel 5 Wrap To Address Register	DMA5_WPTO
DMA + 0510h	DMA Channel 5 Transfer Count Register	DMA5_COUNT
DMA + 0514h	DMA Channel 5 Control Register	DMA5_CON
DMA + 0518h	DMA Channel 5 Start Register	DMA5_START
DMA + 051Ch	DMA Channel 5 Interrupt Status Register	DMA5_INTSTA
DMA + 0520h	DMA Channel 5 Interrupt Acknowledge Register	DMA5_ACKINT
DMA + 0524h	DMA Channel 5 Remaining Length of Current Transfer	DMA5_RLCT
DMA + 0528h	DMA Channel 5 Bandwidth Limiter Register	DMA5_LIMITER
DMA + 052Ch	DMA Channel 5 Programmable Address Register	DMA5_PGMADDR
DMA + 0608h	DMA Channel 6 Wrap Point Address Register	DMA6_WPPT
DMA + 060Ch	DMA Channel 6 Wrap To Address Register	DMA6_WPTO
DMA + 0610h	DMA Channel 6 Transfer Count Register	DMA6_COUNT
DMA + 0614h	DMA Channel 6 Control Register	DMA6_CON
DMA + 0618h	DMA Channel 6 Start Register	DMA6_START
DMA + 061Ch	DMA Channel 6 Interrupt Status Register	DMA6_INTSTA
DMA + 0620h	DMA Channel 6 Interrupt Acknowledge Register	DMA6_ACKINT
DMA + 0624h	DMA Channel 6 Remaining Length of Current Transfer	DMA6_RLCT
DMA + 0628h	DMA Channel 6 Bandwidth Limiter Register	DMA6_LIMITER
DMA + 062Ch	DMA Channel 6 Programmable Address Register	DMA6_PGMADDR
DMA + 0708h	DMA Channel 7 Wrap Point Address Register	DMA7_WPPT
DMA + 070Ch	DMA Channel 7 Wrap To Address Register	DMA7_WPTO
DMA + 0710h	DMA Channel 7 Transfer Count Register	DMA7_COUNT
DMA + 0714h	DMA Channel 7 Control Register	DMA7_CON
DMA + 0718h	DMA Channel 7 Start Register	DMA7_START
DMA + 071Ch	DMA Channel 7 Interrupt Status Register	DMA7_INTSTA
DMA + 0720h	DMA Channel 7 Interrupt Acknowledge Register	DMA7_ACKINT
DMA + 0724h	DMA Channel 7 Remaining Length of Current Transfer	DMA7_RLCT
DMA + 0728h	DMA Channel 7 Bandwidth Limiter Register	DMA7_LIMITER

DMA + 072Ch	DMA Channel 7 Programmable Address Register	DMA7_PGMADDR
DMA + 0808h	DMA Channel 8 Wrap Point Address Register	DMA8_WPPT
DMA + 080Ch	DMA Channel 8 Wrap To Address Register	DMA8_WPTO
DMA + 0810h	DMA Channel 8 Transfer Count Register	DMA8_COUNT
DMA + 0814h	DMA Channel 8 Control Register	DMA8_CON
DMA + 0818h	DMA Channel 8 Start Register	DMA8_START
DMA + 081Ch	DMA Channel 8 Interrupt Status Register	DMA8_INTSTA
DMA + 0820h	DMA Channel 8 Interrupt Acknowledge Register	DMA8_ACKINT
DMA + 0824h	DMA Channel 8 Remaining Length of Current Transfer	DMA8_RLCT
DMA + 0828h	DMA Channel 8 Bandwidth Limiter Register	DMA8_LIMITER
DMA + 082Ch	DMA Channel 8 Programmable Address Register	DMA8_PGMADDR
DMA + 0B10h	DMA Channel 11 Transfer Count Register	DMA11_COUNT
DMA + 0B14h	DMA Channel 11 Control Register	DMA11_CON
DMA + 0B18h	DMA Channel 11 Start Register	DMA11_START
DMA + 0B1Ch	DMA Channel 11 Interrupt Status Register	DMA11_INTSTA
DMA + 0B20h	DMA Channel 11 Interrupt Acknowledge Register	DMA11_ACKINT
DMA + 0B28h	DMA Channel 11 Bandwidth Limiter Register	DMA11_LIMITER
DMA + 0B2Ch	DMA Channel 11 Programmable Address Register	DMA11_PGMADDR
DMA + 0B30h	DMA Channel 11 Write Pointer	DMA11_WRPTR
DMA + 0B34h	DMA Channel 11 Read Pointer	DMA11_RDPTR
DMA + 0B38h	DMA Channel 11 FIFO Count	DMA11_FFCNT
DMA + 0B3Ch	DMA Channel 11 FIFO Status	DMA11_FFSTA
DMA + 0B40h	DMA Channel 11 Alert Length	DMA11_ALTLEN
DMA + 0B44h	DMA Channel 11 FIFO Size	DMA11_FFSIZE
DMA + 0C10h	DMA Channel 12 Transfer Count Register	DMA12_COUNT
DMA + 0C14h	DMA Channel 12 Control Register	DMA12_CON
DMA + 0C18h	DMA Channel 12 Start Register	DMA12_START
DMA + 0C1Ch	DMA Channel 12 Interrupt Status Register	DMA12_INTSTA
DMA + 0C20h	DMA Channel 12 Interrupt Acknowledge Register	DMA12_ACKINT

DMA + 0C28h	DMA Channel 12 Bandwidth Limiter Register	DMA12_LIMITER
DMA + 0C2Ch	DMA Channel 12 Programmable Address Register	DMA12_PGMADDR
DMA + 0C30h	DMA Channel 12 Write Pointer	DMA12_WRPTR
DMA + 0C34h	DMA Channel 12 Read Pointer	DMA12_RDPTR
DMA + 0C38h	DMA Channel 12 FIFO Count	DMA12_FFCNT
DMA + 0C3Ch	DMA Channel 12 FIFO Status	DMA12_FFSTA
DMA + 0C40h	DMA Channel 12 Alert Length	DMA12_ALTLEN
DMA + 0C44h	DMA Channel 12 FIFO Size	DMA12_FFSIZE
DMA + 0D10h	DMA Channel 13 Transfer Count Register	DMA13_COUNT
DMA + 0D14h	DMA Channel 13 Control Register	DMA13_CON
DMA + 0D18h	DMA Channel 13 Start Register	DMA13_START
DMA + 0D1Ch	DMA Channel 13 Interrupt Status Register	DMA13_INTSTA
DMA + 0D20h	DMA Channel 13 Interrupt Acknowledge Register	DMA13_ACKINT
DMA + 0D28h	DMA Channel 13 Bandwidth Limiter Register	DMA13_LIMITER
DMA + 0D2Ch	DMA Channel 13 Programmable Address Register	DMA13_PGMADDR
DMA + 0D30h	DMA Channel 13 Write Pointer	DMA13_WRPTR
DMA + 0D34h	DMA Channel 13 Read Pointer	DMA13_RDPTR
DMA + 0D38h	DMA Channel 13 FIFO Count	DMA13_FFCNT
DMA + 0D3Ch	DMA Channel 13 FIFO Status	DMA13_FFSTA
DMA + 0D40h	DMA Channel 13 Alert Length	DMA13_ALTLEN
DMA + 0D44h	DMA Channel 13 FIFO Size	DMA13_FFSIZE
DMA + 0E10h	DMA Channel 14 Transfer Count Register	DMA14_COUNT
DMA + 0E14h	DMA Channel 14 Control Register	DMA14_CON
DMA + 0E18h	DMA Channel 14 Start Register	DMA14_START
DMA + 0E1Ch	DMA Channel 14 Interrupt Status Register	DMA14_INTSTA
DMA + 0E20h	DMA Channel 14 Interrupt Acknowledge Register	DMA14_ACKINT
DMA + 0E28h	DMA Channel 14 Bandwidth Limiter Register	DMA14_LIMITER
DMA + 0E2Ch	DMA Channel 14 Programmable Address Register	DMA14_PGMADDR
DMA + 0E30h	DMA Channel 14 Write Pointer	DMA14_WRPTR

DMA + 0E34h	DMA Channel 14 Read Pointer	DMA14_RDPTR
DMA + 0E38h	DMA Channel 14 FIFO Count	DMA14_FFCNT
DMA + 0E3Ch	DMA Channel 14 FIFO Status	DMA14_FFSTA
DMA + 0E40h	DMA Channel 14 Alert Length	DMA14_ALTLEN
DMA + 0E44h	DMA Channel 14 FIFO Size	DMA14_FFSIZE

Table 9 DMA Controller Register Map

3.4.2 Register Definitions

Register programming tips:

- Start registers shall be cleared, when associated channels are being programmed.
- PGMADDR, i.e. programmable address, only exists in half-size DMA channels. If DIR in Control Register is high, PGMADDR represents Destination Address. Conversely, If DIR in Control Register is low, PGMADDR represents Source Address.
- Functions of ring-buffer and double-buffer memory data movement can be activated on either source side or destination side by programming DMA_WPPT & and DMA_WPTO, as well as setting WPEN in DMA_CON register high. WPSD in DMA_CON register determines the activated side.

DMA+0000h DMA Global Status Register DMA_GLBSTA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					IT14	RUN14	IT13	RUN13	IT12	RUN12	IT11	RUN11				
Type					RO	RO	RO	RO	RO	RO	RO	RO				
Reset					0	0	0	0	0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IT8	RUN8	IT7	RUN7	IT6	RUN6	IT5	RUN5	IT4	RUN4					IT1	RUN1
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO					RO	RO
Reset	0	0	0	0	0	0	0	0	0	0					0	0

This register helps software program keep track of the global status of DMA channels.

RUN_N DMA channel n status

0 Channel n is stopped or has completed the transfer already.

1 Channel n is currently running.

IT_N Interrupt status for channel n

0 No interrupt is generated.

1 An interrupt is pending and waiting for service.

DMA+0028h DMA Global Bandwidth limiter Register DMA_GLBLIMITER

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									GLBLIMITER							
Type									WO							
Reset									0							

Please refer to the expression in DMAn_LIMITER for detailed note. The value of DMA_GLBLIMITER is set to all DMA channels, from 1, 4~8, 11~14.

DMA+0n00h DMA Channel n Source Address Register DMAn_SRC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC[15:0]															
Type	R/W															
Reset	0															

The above registers contain the base or current source address that the DMA channel is currently operating on. Writing to this register specifies the base address of transfer source for a DMA channel. Before programming these registers, the software program should make sure that STR in DMAn_START is set to 0; that is, the DMA channel is stopped and disabled completely. Otherwise, the DMA channel may run out of order. Reading this register returns the address value from which the DMA is reading.

Note that n is 1

SRC **SRC**[31:0] specifies the base or current address of transfer source for a DMA channel, i.e. channel 1.

WRITE Base address of transfer source

READ Address from which DMA is reading

DMA+0n04h DMA Channel n Destination Address Register DMAn_DST

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DST[31:16]															
Type	R/W															

Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DST[15:0]															
Type	R/W															
Reset	0															

The above registers contain the base or current destination address that the DMA channel is currently operating on.. Writing to this register specifies the base address of the transfer destination for a DMA channel. Before programming these registers, the software should make sure that STR in DMAn_START is set to '0'; that is, the DMA channel is stopped and disabled completely. Otherwise, the DMA channel may run out of order. Reading this register returns the address value to which the DMA is writing.

Note that n is 1.

DST **DST**[31:0] specifies the base or current address of transfer destination for a DMA channel, i.e. channel 1.

WRITE Base address of transfer destination.

READ Address to which DMA is writing.

DMA+0n08h DMA Channel n Wrap Point Count Register DMAn_WPPT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WPPT[15:0]															
Type	R/W															
Reset	0															

The above registers are to specify the transfer count required to perform before the jump point. This can be used to support ring buffer or double buffer style memory accesses. To enable this function, two control bits, WPEN and WPSD, in DMA control register must be programmed. See the following register description for more details. If the transfercounter in the DMA engine matches this value, an address jump occurs, and the next address is the address specified in DMAn_WPTO. Before programming these registers, the software should make sure that STR in DMAn_START is set to '0', that is the DMA channel is stopped and disabled completely. Otherwise, the DMA channel may run out of order. To enable this function, WPEN in DMA_CON is set.

Note that n is 1, 4~8.

WPPT **WPPT**[15:0] specifies the amount of the transfer count from start to jumping point for a DMA channel, i.e. channel 1, 4~8.

WRITE Address of the jump point.

READ Value set by the programmer.

DMA+0n0Ch DMA Channel n Wrap To Address Register DMAn_WPTO

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WPTO[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WPTO[15:0]															
Type	R/W															
Reset	0															

The above registers specify the address of the jump destination of a given DMA transfer to support ring buffer or double buffer style memory accesses. To enable this function, set the two control bits, WPEN and WPSD, in the DMA control register . See the following register description for more details. Before programming these registers, the software should make sure that STR in DMAn_START is set to '0', that is the DMA channel is stopped and disabled completely. Otherwise, the DMA channel may run out of order. To enable this function, WPEN in DMA_CON should be set.

Note that n is 1, 4~8.

WPTO **WPTO**[31:0] specifies the address of the jump point for a DMA channel, i.e. channel 1, 4~8.

WRITE Address of the jump destination.

READ Value set by the programmer.

DMA+0n10h DMA Channel n Transfer Count Register DMAn_COUNT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LEN															
Type	R/W															
Reset	0															

This register specifies the amount of total transfer count that the DMA channel is required to perform. Upon completion, the DMA channel generates an interrupt request to the processor while ITEN in DMAn_CON is set as '1'. Note that the total size of data being transferred by a DMA channel is determined by LEN together with the SIZE in DMAn_CON, i.e. LEN x SIZE.

For virtual FIFO DMA, this register is used to configure the RX threshold and TX threshold. Interrupt is triggered while FIFO count >= RX threshold in RX path or FIFO count =< TX threshold in TX path. Note that ITEN bit in DMA_CON register shall be set, or no interrupt is issued.

Note that n is from 1, 4~8, 11~14.

LEN The amount of total transfer count

DMA+0n14h DMA Channel n Control Register DMAn_CON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								MAS						DIR	WPEN	WPSD
Type								R/W						R/W	R/W	R/W
Reset								0						0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ITEN					BURST					B2W	DRQ	DINC	SINC	SIZE	
Type	R/W					R/W					R/W	R/W	R/W	R/W	R/W	
Reset	0					0					0	0	0	0	0	

This register contains all the available control schemes for a DMA channel that is ready for software programmer to configure. Note that all these fields cannot be changed while DMA transfer is in progress or an unexpected situation may occur.

Note that n is from 1, 4~8, 11~14.

SIZE Data size within the confine of a bus cycle per transfer.

These bits confines the data transfer size between source and destination to the specified value for individual bus cycle. The size is in terms of byte and has maximum value of 4 bytes. It is mainly decided by the data width of a DMA master.

00 Byte transfer/1 byte

01 Half-word transfer/2 bytes

10 Word transfer/4 bytes

11 Reserved

SINC Incremental source address. Source addresses increase every transfer. If the setting of SIZE is Byte, Source addresses increase by 1 every single transfer. If Half-Word, increase by 2; and if Word, increase by 4.

0 Disable

1 Enable

DINC Incremental destination address. Destination addresses increase every transfer. If the setting of SIZE is Byte, Destination addresses increase by 1 every single transfer. If Half-Word, increase by 2; and Iif Word, increase by 4.

0 Disable

1 Enable

DREQ Throttle and handshake control for DMA transfer

0 No throttle control during DMA transfer or transfers occurred only between memories

1 Hardware handshake management

The DMA master is able to throttle down the transfer rate by way of request-grant handshake.

B2W Word to Byte or Byte to Word transfer for the applications of transferring non-word-aligned-address data to word-aligned-address data. Note that BURST is set to 4-beat burst while enabling this function, and the SIZE is set to Byte.

NO effect on channel 1, 11~14.

0 Disable

1 Enable

BURST Transfer Type. Burst-type transfers have better bus efficiency. Mass data movement is recommended to use this kind of transfer. However, note that burst-type transfer does not stop until all of the beats in a burst are completed or transfer length is reached. FIFO threshold of peripherals must be configured carefully while being used to move data from/to the peripherals.

What transfer type can be used is restricted by the SIZE. If SIZE is 00b, i.e. byte transfer, all of the four transfer types can be used. If SIZE is 01b, i.e. half-word transfer, 16-beat incrementing burst cannot be used. If SIZE is 10b, i.e. word transfer, only single and 4-beat incrementing burst can be used.

NO effect on channel 11 - 14.

000 Single

001 Reserved

010 4-beat incrementing burst

011 Reserved

100 8-beat incrementing burst

101 Reserved

110 16-beat incrementing burst

111 Reserved

ITEN DMA transfer completion interrupt enable.

0 Disable

1 Enable

WPSD The side using address-wrapping function. Only one side of a DMA channel can activate address-wrapping function at a time.

NO effect on channel 11 - 14.

0 Address-wrapping on source .

1 Address-wrapping on destination.

WPEN Address-wrapping for ring buffer. The next address of DMA jumps to WRAP TO address when the current address matches WRAP POINT count.

NO effect on channel 11 - 14.

0 Disable

1 Enable

DIR Directions of DMA transfer for half-size and Virtual FIFO DMA channels, i.e. channels 4~14. The direction is from the perspective of the DMA masters. WRITE means read from master and then write to the address specified in DMA_PGMADDR, and vice versa.

NO effect on channel 1.

0 Read

1 Write

MAS Master selection. Specifies which master occupies this DMA channel. Once assigned to certain master, the corresponding DREQ and DACK are connected. For half-size and Virtual FIFO DMA channels, i.e. channels 4~8 and 11~14, a predefined address is assigned as well.

00000 SIM

01000 UART1 TX

01001 UART1 RX

01010 UART2 TX

01011 UART2 RX

01100 UART3 TX

01101 UART3 RX

01110 DSP-DMA

10001 I2C TX

10010 I2C RX

DMA+0n18h DMA Channel n Start Register DMAn_START

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STR															
Type	R/W															
Reset	0															

This register controls the activity of a DMA channel. Note that prior to setting STR to "1", all the configurations should be done by giving proper value to the registers. Note also that once the STR is set to "1", the hardware does not clear it automatically no matter if the DMA channel accomplishes the DMA transfer or not. In other works, the value of **STR** stays "1" regardless of the completion of DMA transfer. Therefore, the software program should be sure to clear **STR** to "0" before restarting another DMA transfer.

Note that n is 1, 4~8, 11~14.

STR Start control for a DMA channel.

0 The DMA channel is stopped.

1 The DMA channel is started and running.

DMA+0n1Ch DMA Channel n Interrupt Status Register DMAn_INTSTA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT															
Type	RO															
Reset	0															

This register shows the interrupt status of a DMA channel. It has the same value as DMA_GLBSTA.

Note that n is from 1, 4~8, 11~14.

INT Interrupt Status for DMA Channel

0 No interrupt request is generated.

1 One interrupt request is pending and waiting for service.

DMA+0n20h DMA Channel n Interrupt Acknowledge Register DMAn_ACKINT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACK															
Type	WO															
Reset	0															

This register is used to acknowledge the current interrupt request associated with the completion event of a DMA channel by software program. Note that this is a write-only register, and any read to it returns a value of “0”.

Note that n is from 1, 4~8, 11~14.

ACK Interrupt acknowledge for the DMA channel

0 No effect

1 Interrupt request is acknowledged and should be relinquished.

DMA+0n24h DMA Channel n Remaining Length of Current Transfer DMAn_RLCT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLCT															
Type	RO															
Reset	0															

This register is to reflect the left amount of the transfer.

Note that n is from 1, 4~8.

DMA+0n28h DMA Bandwidth limiter Register DMAn_LIMITER

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LIMITER							
Type									R/W							
Reset									0							

This register is to suppress the Bus utilization of the DMA channel. The value is from 0 to 255. 0 means no limitation, and 255 means totally banned. The value between 0 and 255 means certain DMA can have permission to use AHB every (4 X n) AHB clock cycles.

Note that it is not recommended to limit the Bus utilization of the DMA channels because this increases the latency of response to the masters, and the transfer rate decreases as well. Before using it, programmer must make sure that the bus masters have some protective mechanism to avoid entering the wrong states.

Note that n is from 1, 4~8, 11~14.

LIMITER from 0 to 255. 0 means no limitation, 255 means totally banned, and others mean Bus access permission every (4 X n) AHB clock.

DMA+0n2Ch DMA Channel n Programmable Address Register DMAn_PGMADDR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PGMADDR[31:16]															
Type	R/W															

Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PGMADDR[15:0]															
Type	R/W															
Reset	0															

The above registers specify the address for a half-size DMA channel. This address represents a source address if DIR in DMA_CON is set to 0, and represents a destination address if DIR in DMA_CON is set to 1. Before being able to program these register, the software should make sure that STR in DMAn_START is set to '0', that is the DMA channel is stopped and disabled completely. Otherwise, the DMA channel may run out of order.

Note that n is from 4~8, 11~14.

PGMADDR **PGMADDR**[31:0] specifies the addresses for a half-size or a Virtual FIFO DMA channel, i.e. channel 4~8, 11 ~14.

WRITE Address of the jump destination.

READ Current address of the transfer.

DMA+0n30h DMA Channel n Virtual FIFO Write Pointer Register DMAn_WRPTR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WRPTR[31:16]															
Type	RO															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WRPTR[15:0]															
Type	RO															

Note that n is from 11 to 14.

WRPTR Virtual FIFO Write Pointer.

DMA+0n34h DMA Channel n Virtual FIFO Read Pointer Register DMAn_RDPTR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDPTR[31:16]															
Type	RO															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDPTR[15:0]															
Type	RO															

Note that n is from 11 to 14.

RDPTR Virtual FIFO Read Pointer.

DMA+0n38h DMA Channel n Virtual FIFO Data Count Register DMAn_FFCNT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FFCNT															
Type	RO															

Note that n is from 11 to 14.

FFCNT To display the number of data stored in FIFO. 0 means FIFO empty, and FIFO is full if FFCNT is equal to FFSIZE.

DMA+0n3Ch DMA Channel n Virtual FIFO Status Register DMAn_FFSTA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														ALT	EMPTY	FULL
Type														RO	RO	RO
Reset														0	1	0

Note that n is from 11 to 14.

FULL To indicate FIFO is full.

0 Not Full

1 Full

EMPTY To indicate FIFO is empty.

0 Not Empty

1 Empty

ALT To indicate FIFO Count is larger than ALTLEN. DMA issues an alert signal to UART to enable UART flow control.

0 Not reach alert region.

1 Reach alert region.

DMA+0n40h DMA Channel n Virtual FIFO Alert Length Register DMAn_ALTLEN

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ALTLEN					
Type											R/W					
Reset											0					

Note that n is from 11 to 14.

ALTLEN Specifies the Alert Length of Virtual FIFO DMA. Once the remaining FIFO space is less than ALTLEN, an alert signal is issued to UART to enable flow control. Normally, ALTLEN shall be larger than 16 for UART application.

DMA+0n44h DMA Channel n Virtual FIFO Size Register DMAn_FFSIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FFSIZE															
Type	R/W															
Reset	0															

Note that n is from 11 to 14.

FFSIZE Specifies the FIFO Size of Virtual FIFO DMA.

3.5 Interrupt Controller

3.5.1 General Description

Figure 13 錯誤! 找不到參照來源。 outlines the major functionality of the MCU Interrupt Controller. The interrupt controller processes all interrupt sources coming from external lines and internal MCU peripherals. Since ARM7EJ-S core supports two levels of interrupt latency, this controller generates two request signals: FIQ for fast, low latency interrupt request and IRQ for more general interrupts with lower priority.

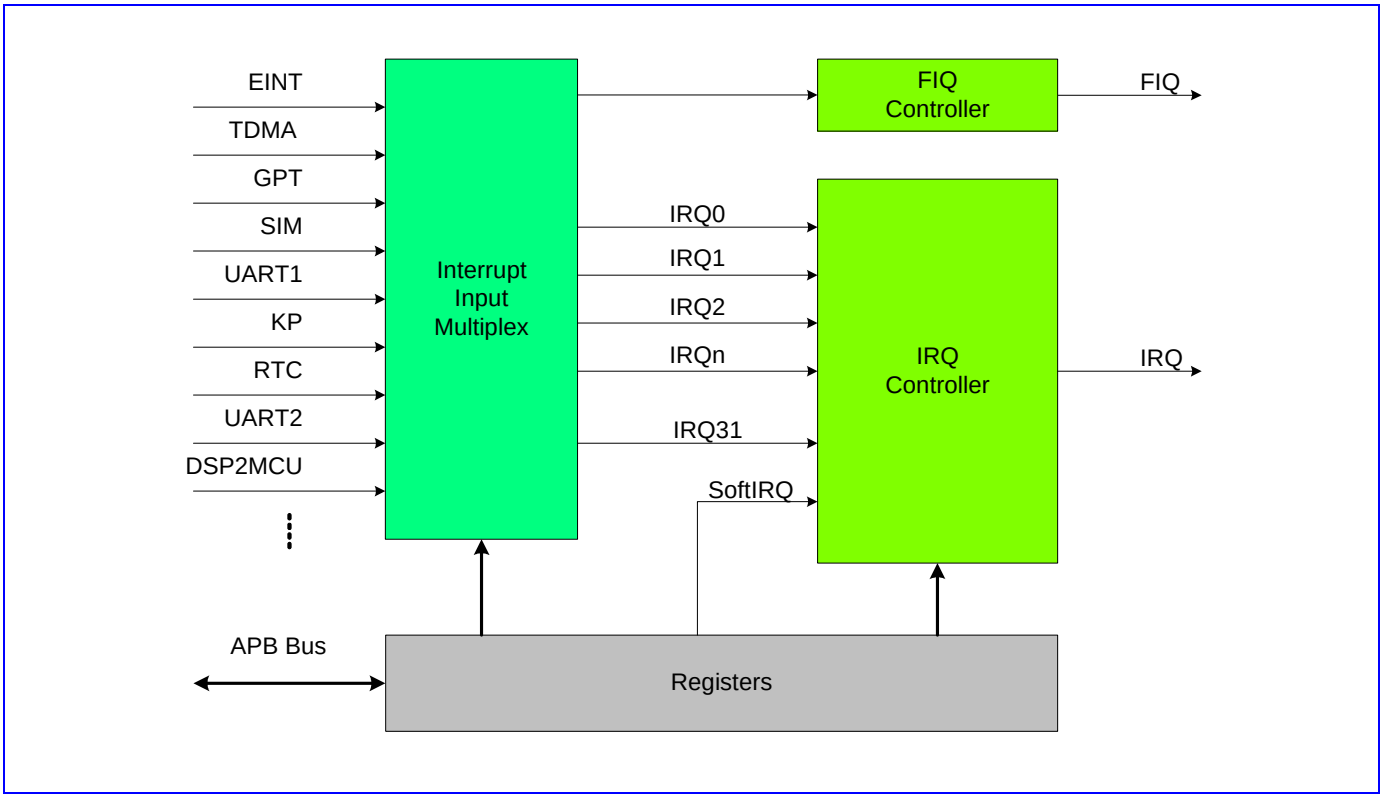


Figure 14 Block Diagram of the Interrupt Controller

One and only one of the interrupt sources can be assigned to FIQ Controller and have the highest priority in requesting timing critical service. All the others share the same IRQ signal by connecting them to IRQ Controller. The IRQ Controller manages up 32 interrupt lines of IRQ0 to IRQ31 with fixed priority in descending order.

The Interrupt Controller provides a simple software interface by mean of registers to manipulate the interrupt request shared system. IRQ Selection Registers and FIQ Selection Register determine the source priority and connecting relation among sources and interrupt lines. IRQ Source Status Register allows software program to identify the source of interrupt that generates the interrupt request. IRQ Mask Register provides software to mask out undesired sources some time. End of Interrupt Register permits software program to indicate to the controller that a certain interrupt service routine has been finished.

Binary coded version of IRQ Source Status Register is also made available for software program to helpfully identify the interrupt source. Note that while taking advantage of this, it should also take the binary coded version of End of Interrupt Register coincidently.

One and only one of the interrupt sources can be assigned to FIQ Controller and have the highest priority in requesting timing critical service. All the others should share the same IRQ signal by connecting them to IRQ Controller. The IRQ Controller manages up 32 interrupt lines of IRQ0 to IRQ31 with fixed priority in descending order.

The Interrupt Controller provides a simple software interface by mean of registers to manipulate the interrupt request shared system. IRQ Selection Registers and FIQ Selection Register determine the source priority and connecting relation among sources and interrupt lines. IRQ Source Status Register allows software program to identify the source of interrupt that generates the interrupt request. IRQ Mask Register provides software to mask out undesired sources some time. End of Interrupt Register permits software program to indicate the controller that a certain interrupt service routine has been finished.

Binary coded version of IRQ Source Status Register is also made available for software program to helpfully identify the interrupt source. Note that while using this register, the controller also needs to use the corresponding binary coded version of

End of Interrupt Register for response.

The essential Interrupt Table of ARM7EJ-S core is shown as **Figure 10.**

Address	Description
00000000h	System Reset
00000018h	IRQ
0000001Ch	FIQ

Table 10 Interrupt Table of ARM7EJ-S

3.5.1.1 Interrupt Source Masking

Interrupt controller provides the function of Interrupt Source Masking by the way of programming MASK register. Any of them can be masked individually.

However, because of the bus latency, the masking takes effect no earlier than 3 clock cycles later. In this time, the to-be-masked interrupts could come in and generate an IRQ pulse to MCU, and then disappear immediately. This IRQ forces MCU going to Interrupt Service Routine and polling Status Register (IRQ_STA or IRQ_STA2), but the register shows there is no interrupt. This might cause MCU malfunction.

There are two ways for programmer to protect their software.

1. Return from ISR (Interrupt Service Routine) immediately while the Status register shows no interrupt.
2. Set I bit of MCU before doing Interrupt Masking, and then clear it after Interrupt Masking done.

Both avoid the problem, but the first item recommended to have in the ISR.

Interrupt controller provides the function of Interrupt Source Masking by the way of programming MASK register. Any of them can be masked individually.

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There are two ways for programmers to protect their software.

1. Return from ISR (Interrupt Service Routine) immediately while the Status register shows no interrupt.
2. Set I bit of MCU before performing Interrupt Masking, and then clear it after Interrupt Masking done.

Both can avoid the problem, but it is always recommended to use the first method list above.

3.5.1.2 External Interrupt

This interrupt controller also integrates an External Interrupt Controller that can support up to 4 interrupt requests coming from external sources, the EINT0~3, and 4 WakeUp interrupt requests, i.e. EINT4~7, coming from peripherals used to inform system to resume the system clock.

The four external interrupts can be used for different kind of applications, mainly for event detections: detection of hand free connection, detection of hood opening, detection of battery charger connection.

Since the external event may be unstable in a certain period, a de-bounce mechanism is introduced to ensure the functionality. The circuitry is mainly used to verify that the input signal remains stable for a programmable number of periods of the clock. When this condition is satisfied, for the appearance or the disappearance of the input, the output of the de-bounce logic

changes to the desired state. Note that, because it uses the 32 KHz slow clock for performing the de-bounce process, the parameter of de-bounce period and de-bounce enable takes effect no sooner than one 32 KHz clock cycle (~31.25us) after the software program sets them. However, the polarities of EINTs are clocked with the system clock. Any changes to them take effect immediately.

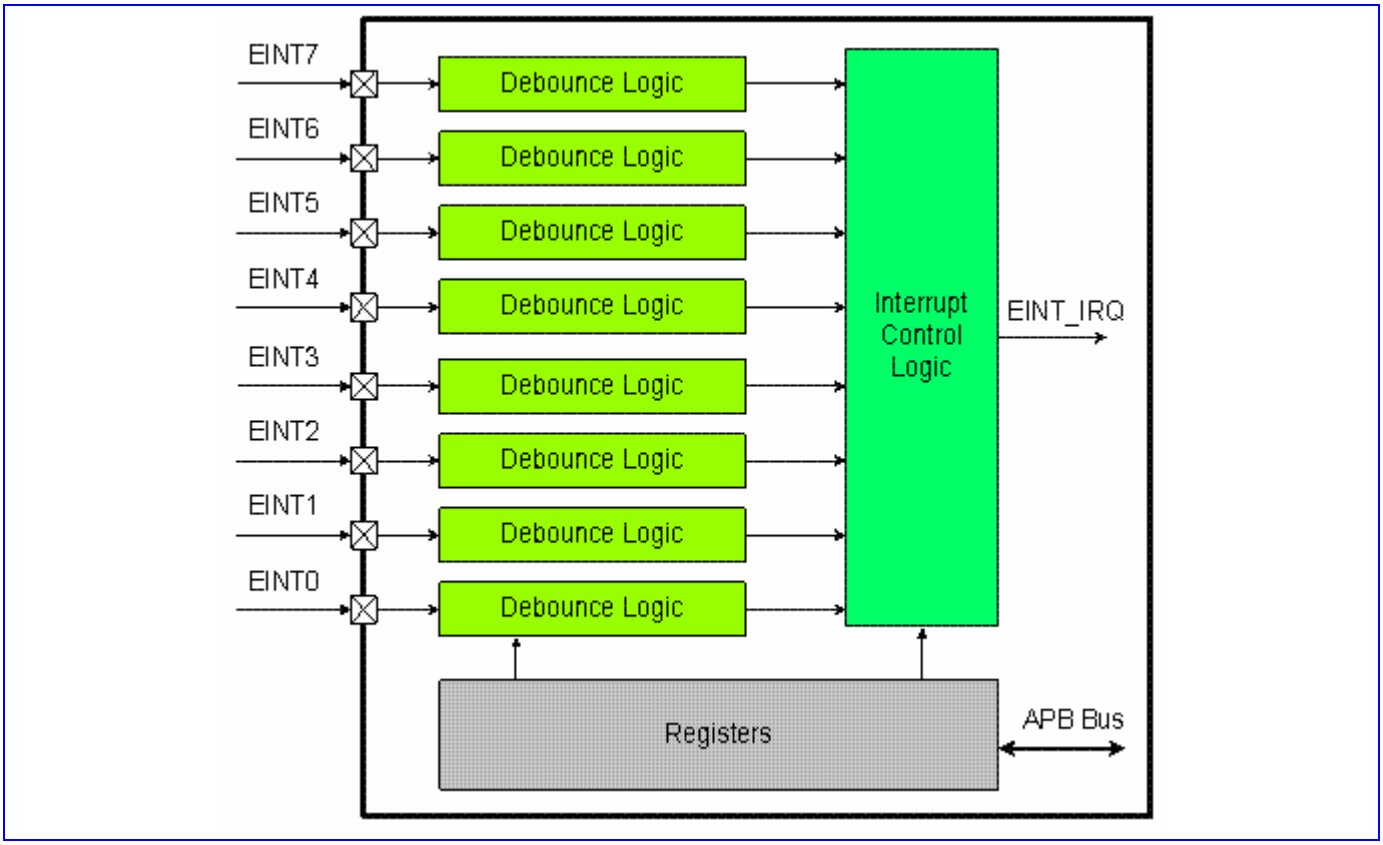


Figure 15 Block diagram of External Interrupt Controller

3.5.1.3 External Interrupt Input Pins

EINT	Edge / Level HW Debounce	SOURCE PIN	SUPPLEMENT
EINT0	Edge / Level Yes	EINT0	1. GPIOs should be in the input mode and are effected by GPIO data input inversion registers. 2. GPIOxx_M is the GPIO mode control registers, please refer to GPIO segment.
EINT1	Edge / Level Yes	EINT1	
EINT2	Edge / Level Yes	if(GPIO42_M==1) then EINT2=GPIO42 else EINT2=1	
EINT3	Edge / Level Yes	if(GPIO43_M==1) then EINT3=GPIO43 else EINT3=1	
EINT4	Edge / Level	if(GPIO26_M==2) then EINT4=GPIO26	

	Yes		else EINT4=1
EINT5	Edge / Level	if(GPIO27_M==2)	then EINT5=GPIO27
	Yes		else EINT5=1
EINT6	Edge / Level	if(GPIO28_M==2)	then EINT6=GPIO28
	Yes		else EINT6=1
EINT7	Edge / Level		CHR_DET from PMU
	Yes		

REGISTER ADDRESS	REGISTER NAME	SYNONYM
CIRQ + 0000h	IRQ Selection 0 Register	IRQ_SEL0
CIRQ + 0004h	IRQ Selection 1 Register	IRQ_SEL1
CIRQ + 0008h	IRQ Selection 2 Register	IRQ_SEL2
CIRQ + 000Ch	IRQ Selection 3 Register	IRQ_SEL3
CIRQ + 0010h	IRQ Selection 4 Register	IRQ_SEL4
CIRQ + 0014h	IRQ Selection 5 Register	IRQ_SEL5
CIRQ + 0018h	FIQ Selection Register	FIQ_SEL
CIRQ + 001Ch	IRQ Mask Register	IRQ_MASK
CIRQ + 0020h	IRQ Mask Disable Register	IRQ_MASK_DIS
CIRQ + 0024h	IRQ Mask Enable Register	IRQ_MASK_EN
CIRQ + 0028h	IRQ Status Register	IRQ_STA
CIRQ + 002Ch	IRQ End of Interrupt Register	IRQ_EOI
CIRQ + 0030h	IRQ Sensitive Register	IRQ_SENS
CIRQ + 0034h	IRQ Software Interrupt Register	IRQ_SOFT
CIRQ + 0038h	FIQ Control Register	FIQ_CON
CIRQ + 003Ch	FIQ End of Interrupt Register	FIQ_EOI
CIRQ + 0040h	Binary Coded Value of IRQ_STATUS	IRQ_STA2
CIRQ + 0044h	Binary Coded Value of IRQ_EOI	IRQ_EOI2
CIRQ + 0100h	EINT Status Register	EINT_STA
CIRQ + 0104h	EINT Mask Register	EINT_MASK
CIRQ + 0108h	EINT Mask Disable Register	EINT_MASK_DIS

CIRQ + 010Ch	EINT Mask Enable Register	EINT_MASK_EN
CIRQ + 0110h	EINT Interrupt Acknowledge Register	EINT_INTACK
CIRQ + 0114h	EINT Sensitive Register	EINT_SENS
CIRQ + 0120h	EINT0 De-bounce Control Register	EINT0_CON
CIRQ + 0130h	EINT1 De-bounce Control Register	EINT1_CON
CIRQ + 0140h	EINT2 De-bounce Control Register	EINT2_CON
CIRQ + 0150h	EINT3 De-bounce Control Register	EINT3_CON
CIRQ + 0160h	EINT4 De-bounce Control Register	EINT4_CON
CIRQ + 0170h	EINT5 De-bounce Control Register	EINT5_CON
CIRQ + 0180h	EINT6 De-bounce Control Register	EINT6_CON
CIRQ + 0190h	EINT7 De-bounce Control Register	EINT7_CON

Table 11 Interrupt Controller Register Map

3.5.2 Register Definitions

CIRQ+0000h IRQ Selection 0 Register IRQ_SEL0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ5					IRQ4					IRQ3			
Type			R/W					R/W					R/W			
Reset			5					4					3			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		IRQ2					IRQ1					IRQ0				
Type		R/W					R/W					R/W				
Reset		2					1					0				

CIRQ+0004h IRQ Selection 1 Register IRQ_SEL1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQB					IRQA					IRQ9			
Type			R/W					R/W					R/W			
Reset			B					A					9			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		IRQ8					IRQ7					IRQ6				
Type		R/W					R/W					R/W				

Reset		8	7	6

CIRQ+0008h IRQ Selection 2 Register IRQ_SEL2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ11					IRQ10					IRQF			
Type			R/W					R/W					R/W			
Reset			11					10					F			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		IRQE					IRQD					IRQC				
Type		R/W					R/W					R/W				
Reset		E					D					C				

CIRQ+000Ch IRQ Selection 3 Register IRQ_SEL3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ17					IRQ16					IRQ15			
Type			R/W					R/W					R/W			
Reset			17					16					15			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		IRQ14					IRQ13					IRQ12				
Type		R/W					R/W					R/W				
Reset		14					13					12				

CIRQ+0010h IRQ Selection 4 Register IRQ_SEL4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			IRQ1D					IRQ1C					IRQ1B			
Type			R/W					R/W					R/W			
Reset			1D					1C					1B			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		IRQ1A					IRQ19					IRQ18				
Type		R/W					R/W					R/W				
Reset		1A					19					18				

CIRQ+0014h IRQ Selection 5 Register IRQ_SEL5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							IRQ1F					IRQ1E				
Type							R/W					R/W				
Reset							1F					1E				

CIRQ+0018h FIQ Selection Register FIQ_SEL

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												FIQ				
Type												R/W				
Reset												0				

The IRQ/FIQ Selection Registers provide system designers with a flexible routing scheme to make various mappings of priority among interrupt sources possible. It allows the interrupt sources to be mapped onto interrupt requests of either FIQ or IRQ. While only one interrupt source can be assigned to FIQ, the other ones should share IRQ by mapping them onto IRQ0 to IRQ1F, which are connected to IRQ controller. The priority of IRQ0-IRQ1F is fixed, i.e. IRQ0 > IRQ1 > IRQ2 > … > IRQ1E > IRQ1F. During the software configuration process, the Interrupt Source Code of desired interrupt source should be written into source field of the corresponding IRQ_SEL0-IRQ_SEL4/FIQ_SEL. 5-bit Interrupt Source Codes for all interrupt sources are fixed and defined in **Table 12.** The IRQ/FIQ Selection Registers provide system designers with a flexible routing scheme to make various mappings of priority among interrupt sources possible. The registers allow the interrupt sources to be mapped onto interrupt requests of either FIQ or IRQ. While only one interrupt source can be assigned to FIQ, the other ones share IRQs by mapping them onto IRQ0 to IRQ1F connected to IRQ controller. The priority sequence of IRQ0~IRQ1F is fixed, i.e. IRQ0 > IRQ1 > IRQ2 > … > IRQ1E > IRQ1F. During the software configuration process, the Interrupt Source Code of desired interrupt source should be written into source field of the corresponding IRQ_SEL0-IRQ_SEL4/FIQ_SEL. Five-bit Interrupt Source Codes for all interrupt sources are fixed and defined.

Interrupt Source	STA2 (Hex)	STA
MFIQ	0	00000001
TDMA_CTIRQ1	1	00000002
TDMA_CTIRQ2	2	00000004
DSP1_to_CPU	3	00000008
SIM	4	00000010

DMA	5	00000020
TDMA	6	00000040
UART1	7	00000080
KeyPad	8	00000100
UART2	9	00000200
GPTimer	A	00000400
EINT	B	00000800
RTC	E	00004000
LCD	10	00010000
UART3	11	00020000
MIRQ	12	00040000
WDT	13	00080000
SWDBG	14	00100000
I^2C	1b	08000000
DSP2_to_CPU	1f	80000000

Table 12 Interrupt Source Code for Interrupt Sources

FIQ, IRQ0-1F The 5-bit content of this field would be the Interrupt Source Code shown in Table 12 indicating that the certain interrupt source uses the associated interrupt line to generate fast interrupt requests. The 5-bit content of this field corresponds to an Interrupt Source Code shown above.

CIRQ+001Ch IRQ Mask Register IRQ_MASK

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ1F	IRQ1E	IRQ1D	IRQ1C	IRQ1B	IRQ1A	IRQ19	IRQ18	IRQ17	IRQ16	IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF	IRQE	IRQD	IRQC	IRQB	IRQA	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

This register contains a mask bit for each interrupt line in IRQ Controller. The register allows each interrupt source IRQ0 to IRQ1F to be disabled or masked separately under software control. After a system reset, all bit values are set to 1 to indicate that interrupt requests are prohibited.

This register contains mask bit for each interrupt line in IRQ Controller. It allows each interrupt source of IRQ0 to IRQ1F to be disabled or masked out separately under software control. After System Reset, all bit values will be set to '1' to indicate that interrupt requests are prohibited.

IRQ0-1F Mask control for the associated interrupt source in the IRQ controller Mask Control for the Associated Interrupt Source in IRQ Controller

0 Interrupt is enabled

1 Interrupt is disabled

CIRQ+0020h IRQ Mask Clear Register IRQ_MASK_CLR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ1F	IRQ1E	IRQ1D	IRQ1C	IRQ1B	IRQ1A	IRQ19	IRQ18	IRQ17	IRQ16	IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF	IRQE	IRQD	IRQC	IRQB	IRQA	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C

This register is used to clear bits in IRQ Mask Register. When writing to this register, the data bits that are HIGH cause the corresponding bits in IRQ Mask Register to be cleared. Data bits that are LOW have no effect on the corresponding bits in IRQ Mask Register.

This register is used to clear bits in the IRQ Mask Register. When writing to this register, the data bits that are high will cause the corresponding bits in the IRQ Mask Register to be cleared. Data bits that are low have no effect on the corresponding bits in the IRQ Mask Register

IRQ0-1F Clear corresponding bits in IRQ Mask Register.

0 No effect

1 Disable the corresponding MASK bit

CIRQ+0024h IRQ Mask SET Register IRQ_MASK_SET

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ1F	IRQ1E	IRQ1D	IRQ1C	IRQ1B	IRQ1A	IRQ19	IRQ18	IRQ17	IRQ16	IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10
Type	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF	IRQE	IRQD	IRQC	IRQB	IRQA	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
Type	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S

This register is used to set bits in the IRQ Mask Register. When writing to this register, the data bits that are HIGH cause the corresponding bits in IRQ Mask Register to be set. Data bits that are LOW have no effect on the corresponding bits in IRQ Mask Register.

This register is used to set bits in the IRQ Mask Register. When writing to this register, the data bits that are high will cause the corresponding bits in the IRQ Mask Register to be set. Data bits that are low have no effect on the corresponding bits in the IRQ Mask Register

IRQ0-1F Set corresponding bits in IRQ Mask Register.

0 No effect

1 Enable corresponding MASK bit

CIRQ+0028h IRQ Source Status Register IRQ_STA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ1F	IRQ1E	IRQ1D	IRQ1C	IRQ1B	IRQ1A	IRQ19	IRQ18	IRQ17	IRQ16	IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF	IRQE	IRQD	IRQC	IRQB	IRQA	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This Register allows software to poll which interrupt line has generated an IRQ interrupt request. A bit set to 1 indicates a corresponding active interrupt line. Only one flag is active at a time. The IRQ_STA is type of read-clear; write access has no effect on the content.

This Register allows software to poll which interrupt line generates the IRQ interrupt request. A bit set to '1' indicates a corresponding active interrupt line. Only one flag is active at a time. The IRQ_STA is type of READ-Clear, write access will have no effect to the content.

IRQ0-1F Interrupt indicator for the associated interrupt source. Interrupt Indication for the Associated Interrupt Source

0 The associated interrupt source is non-active.

1 The associated interrupt source is asserted.

CIRQ+002Ch IRQ End of Interrupt Register IRQ_EOI

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ1F	IRQ1E	IRQ1D	IRQ1C	IRQ1B	IRQ1A	IRQ19	IRQ18	IRQ17	IRQ16	IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF	IRQE	IRQD	IRQC	IRQB	IRQA	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register provides a mean for software to relinquish and to refresh the interrupt controller. Writing a 1 to a specific bit position results in an End of Interrupt command issued internally to the corresponding interrupt line.

This register provides a mean for software to relinquish and refresh the Interrupt Controller. Writing a '1' to the specific bit position will result in an End of Interrupt Command internally to the corresponding interrupt line.

IRQ0-1F End of Interrupt command for the associated interrupt line. End of Interrupt Command for the Associated Interrupt Line

0 No service is currently in progress or pending

1 Interrupt request is in-service

CIRQ+0030h IRQ Sensitive Register IRQ_SENS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ1F	IRQ1E	IRQ1D	IRQ1C	IRQ1B	IRQ1A	IRQ19	IRQ18	IRQ17	IRQ16	IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF	IRQE	IRQD	IRQC	IRQB	IRQA	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

All interrupt lines of IRQ Controller, IRQ0~IRQ1F can be programmed as either edge or level sensitive. By default, all the interrupt lines are edge sensitive and should be active LOW. Once a interrupt line is programmed as edge sensitive, an interrupt request is triggered only at the falling edge of interrupt line, and the next interrupt is not accepted until the EOI command is given. However, level sensitive interrupts trigger is according to the signal level of the interrupt line. Once the interrupt line become from HIGH to LOW, an interrupt request is triggered, and another interrupt request is triggered if the signal level remains LOW after an EOI command. Note that in edge sensitive mode, even if the signal level remains LOW after EOI command, another interrupt request is not triggered. That is because edge sensitive interrupt is only triggered at the falling edge.

All interrupt lines of IRQ Controller, IRQ0-IRQ1F can be programmed as either edge or level sensitive. By default, all the interrupt lines are edge sensitive and should be active LOW. Once a interrupt line is programmed as edge sensitive, an interrupt request is triggered only at the falling edge of interrupt line, and the next interrupt will not be taken until the EOI command is given. However, level sensitive interrupt triggering is according to the signal level of the interrupt line. Once the interrupt line become from High to Low, an interrupt request is triggered, and another interrupt request will be triggered if the signal level remain Low after EOI command. Please note that in edge sensitive mode, even if the signal level remains Low after EOI command, another interrupt request will not be triggered. This is because edge sensitive interrupt is only triggered at the falling edge.

IRQ0-1F Sensitivity type of the associated Interrupt Source Sensitive Type of the Associated Interrupt Source

0 Edge sensitivity with active LOW

1 Level sensitivity with active LOW

CIRQ+0034h IRQ Software Interrupt Register IRQ_SOFT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IRQ1F	IRQ1E	IRQ1D	IRQ1C	IRQ1B	IRQ1A	IRQ19	IRQ18	IRQ17	IRQ16	IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQF	IRQE	IRQD	IRQC	IRQB	IRQA	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Setting “1” to the specific bit position generates a software interrupt for corresponding interrupt line before mask. This register is used for debug purpose.

IRQ0-IRQ1F Software Interrupt

CIRQ+0038h FIQ Control Register FIQ_CON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SENS	MASK
Type															R/W	R/W
Reset															0	1

This register provides a means for software program to control the FIQ cController.

MASK Mask control for the FIQ Interrupt Source

0 Interrupt is enabled

1 Interrupt is disabled

SENS Sensitivity type of the FIQ Interrupt Source

0 Edge sensitivity with active LOW

1 Level sensitivity with active LOW

CIRQ+003Ch FIQ End of Interrupt Register FIQ_EOI

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EOI
Type																WO
Reset																0

This register provides a means for software to relinquish and to refresh the FIQ controller. Writing a '1' to the specific bit position results in an End of Interrupt command issued internally to the corresponding interrupt line.

This register provides a mean for software to relinquish and refresh the FIQ Controller. Writing a '1' to the specific bit position will result in an End of Interrupt Command internally to the corresponding interrupt line.

EOI End of Interrupt command

CIRQ+0040h Binary Coded Value of IRQ_STATUS IRQ_STA2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								NOIRQ				STAS				
Type								RO				RO				
Reset								0				0				

This Register is a binary coded version of IRQ_STA. It is used by the software program to poll which interrupt line has generated the IRQ interrupt request in a much easier way. Any read to it has the same result as reading IRQ_STA. The IRQ_STA2 is also read-only; write access has no effect on the content. Note that IRQ_STA2 should be coupled with IRQ_EOI2 while using it.

This Register is a binary coded version of IRQ_STA. It is used for software program to poll and see which interrupt line generated the IRQ interrupt request in a much easier way. Any read to it has the same result as reading IRQ_STA. The IRQ_STA2 is also READ-ONLY, write access has no effect to the content. Note that, IRQ_STA2 should be coupled with IRQ_EOI2 while using it.

STSA Binary coded value of IRQ_STA

NOIRQ Indicating if there is an IRQ or not. If there is no IRQ, this bit will be HIGH, and the value of STSA should be 0_0000b.

CIRQ+0044h Binary Coded Value of IRQ_EOI IRQ_EOI2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												EOI				
Type												WO				
Reset												0				

This register is a binary coded version of IRQ_EOI. It provides an easier way for software program to relinquish and to refresh the interrupt controller. Writing a specific code results in an End of Interrupt command issued internally to the corresponding interrupt line. Note that IRQ_EOI2 should be coupled with IRQ_STA2 while using it.

This register is a binary coded version of IRQ_EOI. It provides an easier way for software program to relinquish and refresh the Interrupt Controller. Writing a specific code will result in an End of Interrupt Command internally to the corresponding interrupt line. Note that, IRQ_EOI2 should be coupled with IRQ_STA2 while using it.

EOI Binary coded value of IRQ_EOI

CIRQ+0100h EINT Interrupt Status Register EINT_STA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EINT7	EINT6	EINT5	EINT4	EINT3	EINT2	EINT1	EINT0
Type									RO	RO	RO	RO	RO	RO	RO	RO
Reset									0	0	0	0	0	0	0	0

This register keeps up with current status of which EINT Source generated the interrupt request. If EINT sources are set to edge sensitive, EINT_IRQ will be de-asserted while this register is read.

EINT0-EINT7 Interrupt Status

0 No Interrupt request is generated

1 Interrupt request is pending

CIRQ+0104h EINT Interrupt Mask Register EINT_MASK

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EINT7	EINT6	EINT5	EINT4	EINT3	EINT2	EINT1	EINT0

Type									R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset									1	1	1	1	1	1	1	1

This register controls whether or not EINT Source is allowed to generate an interrupt request. Setting a "1" to the specific bit position prohibits the external interrupt line from becoming active.

This register controls whether if EINT Source is allowed to generate interrupt request. Setting a "1" to the specific bit position prohibits the External Interrupt Line to active accordingly.

EINT0-EINT7 Interrupt Mask

0 Interrupt request is enabled.

1 Interrupt request is disabled.

CIRQ+0108h EINT Interrupt Mask Clear Register EINT_MASK_CLR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EINT7	EINT6	EINT5	EINT4	EINT3	EINT2	EINT1	EINT0
Type									W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C

This register is used to clear individual mask bits. Only the bits set to 1 are in effect, and interrupt masks for which the mask bit is set are cleared (set to 0). Otherwise the interrupt mask bit retains its original value.

This register is used to individually clear mask bit. Only the bits set to 1 are in effect, and these mask bits will set to 0. Otherwise mask bits keep original value.

EINT0-EINT7 Disable Mask mask for the associated external interrupt source

0 No effect.

1 Disable the corresponding MASK bit.

CIRQ+010Ch EINT Interrupt Mask Set Register EINT_MASK_SET

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EINT7	EINT6	EINT5	EINT4	EINT3	EINT2	EINT1	EINT0
Type									W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S

This register is used to set individual mask bits. Only the bits set to 1 are in effect, and interrupt masks for which the mask bit is set are set to 1. Otherwise the interrupt mask bit retains its original value.

This register is used to individually set mask bit. Only the bits set to 1 are in effect, and these mask bits will set to 1. Otherwise mask bits keep original value.

EINT0-EINT7 Disable mask for the associated external interrupt source.

0 No effect.

1 Enable corresponding MASK bit.

CIRQ+0110h EINT Interrupt Acknowledge Register EINT_INTACK

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EINT7	EINT6	EINT5	EINT4	EINT3	EINT2	EINT1	EINT0
Type									WO	WO	WO	WO	WO	WO	WO	WO
Reset									0	0	0	0	0	0	0	0

Writing “1” to the specific bit position acknowledge the interrupt request correspondingly to the external interrupt line source.

Writing “1” to the specific bit position means to acknowledge the interrupt request correspondingly to the External Interrupt Line source.

EINT0-EINT7 Interrupt acknowledgement

0 No effect.

1 Interrupt Request is acknowledged.

CIRQ+0114h EINT Sensitive Register EINT_SENS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EINT7	EINT6	EINT5	EINT4	EINT3	EINT2	EINT1	EINT0
Type									R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset									1	1	1	1	1	1	1	1

Sensitivity type of external interrupt source.

EINT0-7 Sensitive Type of the associated external interrupt source

0 Edge sensitivity.

1 Level sensitivity.

CIRQ+01m0h EINTn De-bounce Control Register EINTn_CON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN				POL	CNT										
Type	R/W				R/W	R/W										
Reset	0				0	0										

These registers control the de-bounce logic for external interrupt sources in order to minimize the possibility of false activations.

These registers control the de-bounce logic for external interrupt sources in order to minimize the possibility of false activations. Note that n is from 0 to 7, and m is n plus+ 2.

CNT De-bounce duration in terms of numbers of 32KHz clock cycles

POL Activation type of the EINT source

0 Negative polarity

1 Positive polarity

EN De-bounce control circuit

0 Disable

1 Enable

3.6 External Memory Interface

3.6.1 General Description

MT6223 incorporates a powerful and flexible memory controller, External Memory Interface, to connect with a variety of memory components. This controller provides one generic access scheme for FLASH Memory, SRAM and PSRAM. Up to 8 memory banks can be supported simultaneously, BANK0-BANK7, with a maximum size of 64MB each

Since most of the FLASH Memory, SRAM and PSRAM have similar AC requirements, a generic configuration scheme to interface them is desired. This way, the software program can treat different components by simply specifying certain predefined parameters. All these parameters are based on cycle time of system clock.

The interface definition based on such scheme is listed in **Table 13**. Note that, this interface always operates data in Little Endian format for all types of accesses.

Signal Name	Type	Description
EA[25:0]	O	Address Bus

ED[15:0]	I/O	Data Bus
EWR#	O	Write Enable Strobe
ERD#	O	Read Enable Strobe
ELB#	O	Lower Byte Strobe
EUB#	O	Upper Byte Strobe
ECS# [7:0]	O	BANK0~BANK7 Selection Signal
EPDN	O	PSRAM Power Down Control Signal
ECLK	O	Burst Mode FLASH Memory Clock Signal
EADV#	O	Burst Mode FLASH Memory Address Latch Signal
EWAIT	I	Wait Signal Input

Table 13 **External Memory Interface of MT6223 for Asynchronous/Synchronous Type Components**

This controller can also handle parallel type of LCD. By connecting with them, 8080 type of control method is supported. The interface definition is detailed in **Table 14**.

Bus Type	ECS7#	EA25	ERD#	EWR#	ED[15:0]
8080 series	CS#	A0	RD#	WR#	D[15:0]

Table 14 Configuration for LCD Parallel Interface

REGISTER ADDRESS	REGISTER NAME	SYNONYM
EMI + 0000h	EMI Control Register for BANK0	EMI_CONA
EMI + 0008h	EMI Control Register for BANK1	EMI_CONB
EMI + 0010h	EMI Control Register for BANK2	EMI_CONC
EMI + 0018h	EMI Control Register for BANK3	EMI_COND
EMI + 0020h	EMI Control Register for BANK4	EMI_CONE
EMI + 0028h	EMI Control Register for BANK5	EMI_CONF
EMI + 0030h	EMI Control Register for BANK6	EMI_CONG
EMI + 0038h	EMI Control Register for BANK7	EMI_CONH
EMI + 0040h	EMI Remap Control Register	EMI_REMAP
EMI + 0044h	EMI General Control Register	EMI_GEN
EMI + 0050h	Code Cache and Code Prefetch Control Register	PREFETCH_CON
EMI + 0078h	EMI A/D Mux Control Register	EMI_ADMUX

Table 15 External Memory Interface Register Map

3.6.2 Register Definitions

EMI+0000h EMI Control Register for BANK0 EMI_CONA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	C2WS		C2WH		C2RS				ADVW	ADVR		PRLT			BMODE	PMODE
Type	R/W		R/W		R/W				R/W	R/W		R/W			R/W	R/W
Reset	0		0		0				1	1		0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DW	RBLN	HPI	WST					BW	WAIT	PSIZE	RLT				
Type	R/W	R/W	R/W	R/W					R/W	R/W	R/W	R/W				
Reset	0	1	0	0					0	0	0	7				

EMI+0008h EMI Control Register for BANK1 EMI_CONB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	C2WS		C2WH		C2RS				ADVW	ADVR		PRLT			BMODE	PMODE
Type	R/W		R/W		R/W				R/W	R/W		R/W			R/W	R/W
Reset	0		0		0				1	1		0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DW	RBLN	HPI	WST					BW	WAIT	PSIZE	RLT				
Type	R/W	R/W	R/W	R/W					R/W	R/W	R/W	R/W				
Reset	0	1	0	0					0	0	0	7				

EMI+0010h EMI Control Register for BANK2 EMI_CONC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	C2WS		C2WH		C2RS				ADVW	ADVR		PRLT			BMODE	PMODE
Type	R/W		R/W		R/W				R/W	R/W		R/W			R/W	R/W
Reset	0		0		0				1	1		0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DW	RBLN	HPI	WST					BW	WAIT	PSIZE	RLT				
Type	R/W	R/W	R/W	R/W					R/W	R/W	R/W	R/W				

Reset	0	1	0	0					0	0	0	7				

EMI+0018h EMI Control Register for BANK3 EMI_COND

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	C2WS		C2WH		C2RS				ADVW	ADVR		PRLT			BMODE	PMODE
Type	R/W		R/W		R/W				R/W	R/W		R/W			R/W	R/W
Reset	0		0		0				1	1		0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DW	RBLN	HPI	WST					BW	WAIT	PSIZE	RLT				
Type	R/W	R/W	R/W	R/W					R/W	R/W	R/W	R/W				
Reset	0	1	0	0					0	0	0	7				

EMI+0020h EMI Control Register for BANK4 EMI_CONE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	C2WS		C2WH		C2RS				ADVW	ADVR		PRLT			BMODE	PMODE
Type	R/W		R/W		R/W				R/W	R/W		R/W			R/W	R/W
Reset	0		0		0				1	1		0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DW	RBLN	HPI	WST					BW	WAIT	PSIZE	RLT				
Type	R/W	R/W	R/W	R/W					R/W	R/W	R/W	R/W				
Reset	0	1	0	0					0	0	0	7				

EMI+0028h EMI Control Register for BANK5 EMI_CONF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	C2WS		C2WH		C2RS				ADVW	ADVR		PRLT			BMODE	PMODE
Type	R/W		R/W		R/W				R/W	R/W		R/W			R/W	R/W
Reset	0		0		0				1	1		0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DW	RBLN	HPI	WST					BW	WAIT	PSIZE	RLT				
Type	R/W	R/W	R/W	R/W					R/W	R/W	R/W	R/W				
Reset	0	1	0	0					0	0	0	7				

EMI+0030h EMI Control Register for BANK6 EMI_CONG

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	C2WS		C2WH		C2RS				ADVW	ADVR		PRLT			BMODE	PMODE
Type	R/W		R/W		R/W				R/W	R/W		R/W			R/W	R/W
Reset	0		0		0				1	1		0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DW	RBLN	HPI	WST					BW	WAIT	PSIZE	RLT				
Type	R/W	R/W	R/W	R/W					R/W	R/W	R/W	R/W				
Reset	0	1	0	0					0	0	0	7				

EMI+0038h EMI Control Register for BANK7 EMI_CONH

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	C2WS		C2WH		C2RS				ADVW	ADVR		PRLT			BMODE	PMODE
Type	R/W		R/W		R/W				R/W	R/W		R/W			R/W	R/W
Reset	0		0		0				1	1		0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DW	RBLN	HPI	WST					BW	WAIT	PSIZE	RLT				
Type	R/W	R/W	R/W	R/W					R/W	R/W	R/W	R/W				
Reset	0	1	0	0					0	0	0	7				

For each bank (BANK0-BANK7), a dedicated control register is associated with the bank controller. These registers have the timing parameters that help the controller to convey memory access into proper timing waveform. Note that, except for parameter ADVW, ADVR, BMODE, PMODE, DW, RBLN, HPI and PSIZE, all the other parameters specified explicitly are based on system clock speed in terms of cycle count.

RLT Read Latency Time

Specifying the parameter RLT turns effectively to insert wait-states in bus transfer to requesting agent. Such parameter should be chosen carefully to meet the common parameter tACC (access time) for device in read operation. Example is shown below.

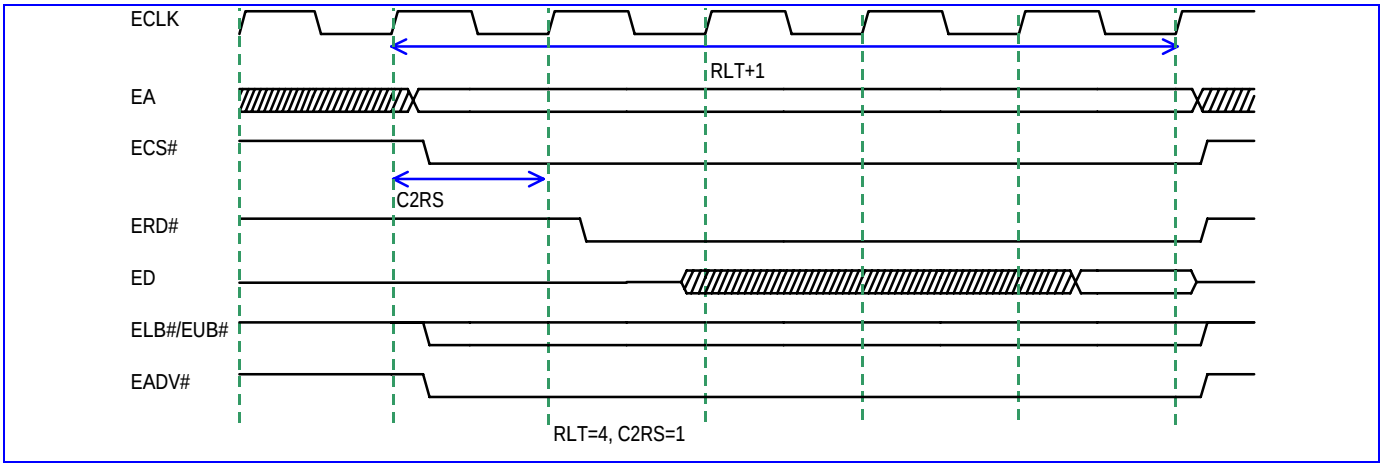


Figure 16 Read Wait State Timing Diagram (ADVR=1)

Access Time	Read Latency Time		
	13MHz	26MHz	52MHz
60ns	0	1	3
90ns	1	2	4
120ns	1	3	6

Table 16 Reference value of Read Latency Time for variant memory devices

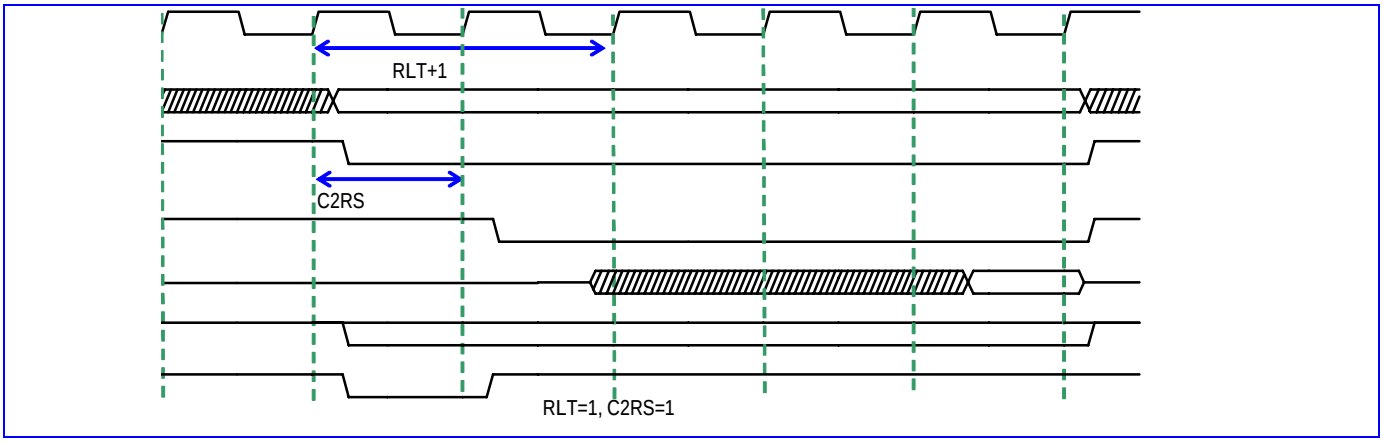


Figure 17 Read Wait State Timing Diagram (ADVR=0)

PMODE Page Mode Control

If target device supports page mode operations, the Page Mode Control can be enabled. Read in Page Mode is determined by set of parameters: PRLT and PSIZE.

0 disable page mode operation

1 enable page mode operation

BMODE Burst Mode Control

If target device supports burst mode operations, the Burst Mode Control can be enabled. Read in Burst Mode is determined by set of parameters: PRLT and PSIZE.

0 disable burst mode operation

1 enable burst mode operation

PRLT Read Latency within the Same Page or in Burst Mode Operation

Since page/burst mode operation only helps to eliminate read latency in subsequent burst within the same page, it doesn't matter with the initial latency at all. Thus, it should still adopt RLT parameter for initial read or burst read between different pages though PMODE or BMODE is set "1".

000 zero wait state

001 one wait state

010 two wait state

011 three wait state

100 four wait state

101 five wait state

110 six wait state

111 seven wait state

PSIZE Page/Burst Size for Page/Burst Mode Operation

These bit positions describe the page/burst size that the Page/Burst Mode enabled device will behave.

0 8 byte, EA[25:3] remains the same

1 16 byte, EA[25:4] remains the same

WST Write Wait State

Specifying the parameters to extend adequate setup and hold time for target component in write operation. Those parameters also effectively insert wait-states in bus transfer to requesting agent. Example is shown in **Figure 18** and **Table 17**.

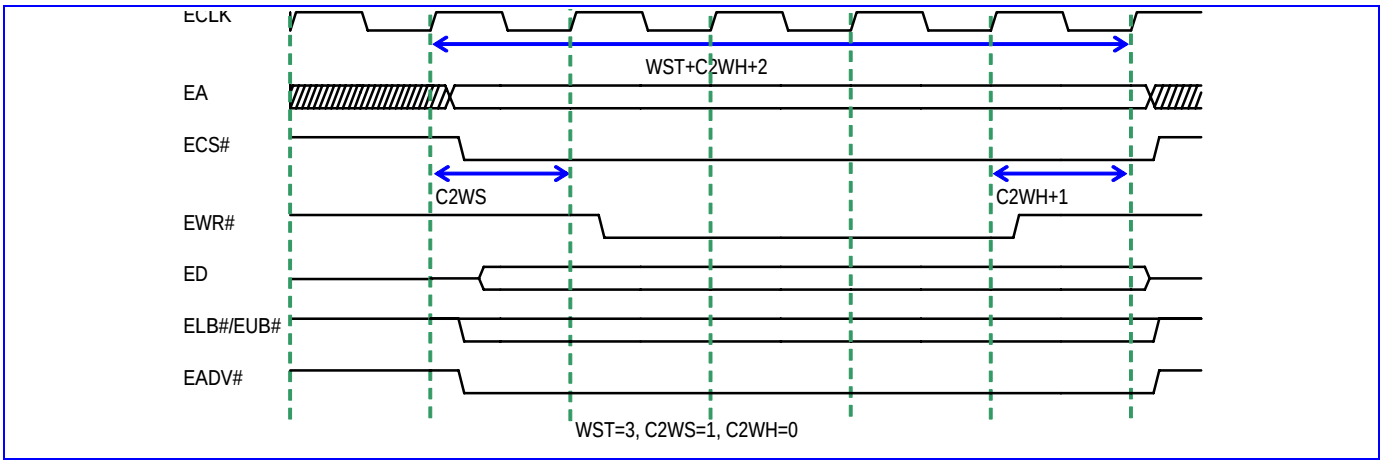


Figure 18 Write Wait State Timing Diagram (ADVW=1)

Write Pulse Width (Write Data Setup Time)	Write Wait State		
	13MHz	26MHz	52MHz

30ns	0	0	1
60ns	0	1	3
90ns	1	2	4

Table 17 Reference value of Write Wait State for variant memory devices

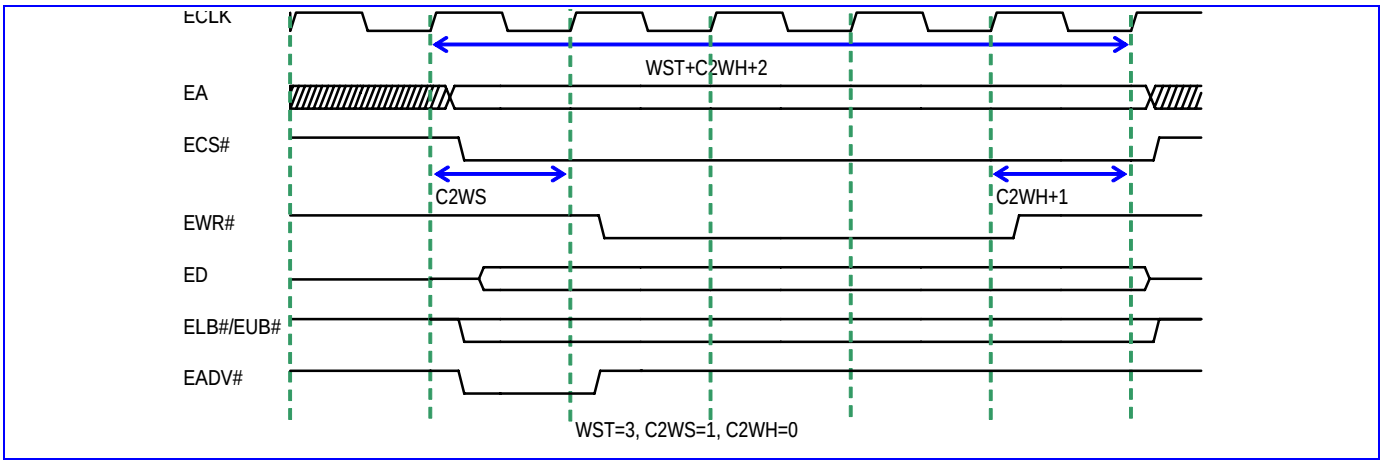


Figure 19 Write Wait State Timing Diagram (ADVW=0)

RBLN Read Byte Lane Enable

0 all byte lanes held high during system reads

1 all byte lanes held low during system reads

DW Data Width

Since the data width of internal system bus is fixed as 32-bit wide, any access to external components might be converted into more than one cycles, depending on transfer size and the parameter DW for the specific component. In general, this bit position of certain component is cleared to '0' upon system reset and is programmed during the system initialization process prior to begin access to it. Note that, dynamic changing this parameter will cause unexpected result.

0 16-bit device

1 8-bit device

HPI HPI Mode Control

ADVR Read Address Valid

0 EADV# will be toggled to latch the valid address in read operation

1 EADV# will be held low for entire read operation

ADVW Write Address Valid

0 EADV# will be toggled to latch the valid address in write operation

1 EADV# will be held low for entire write operation

C2RS Chip Select to Read Strobe Setup Time

C2WH Chip Select to Write Strobe Hold Time

C2WS Chip Select to Write Strobe Setup Time

EMI+0040h EMI Re-map Control Register EMI_REMAP

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RM1	RM0
Type															R/W	R/W
Reset															BOOT	0

This register accomplishes the Memory Re-mapping Mechanism. Basically, it provides the kernel software program or system designer a capability of changing memory configuration dynamically. Three kinds of configuration are permitted.

RM[1:0] Re-mapping control for Boot Code, BANK0 and BANK1, refer to **Table 18**.

RM[1:0]	Address 0000_0000h – 0x07ff_ffffh	Address 0800_0000h – 0x0fff_ffffh
00	Boot Code	BANK1
01	BANK1	BANK0
10	BANK0	BANK1
11	BANK1	BANK0

Table 18 Memory Map Configuration

EMI+0044h EMI General Control Register EMI_GEN

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CKSR	CKE2	CKE4	CKE8	CONSR	CONE2	CONE4	CONE8	EASR	EAE2	EAE4	EAE8	EDSR	EDE2	EDE4	EDE8
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/w
Reset	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRCEN	PRCCNT				EXTGUARD		EDA	FLUSH	WPOL	PDNE	CKE		CKDLY		
Type	R/W	R/W				R/W		R/W	R/W	R/W	R/W	R/W		R/W		
Reset	0	0				0		1	1	0	0	0		0		

This register is general control that can alter the behavior of all bank controllers according to specific features below.

PRCEN Pseudo SRAM Write Protection Control

0 Disable

1 Enable

PRCCNT Pseudo SRAM Dummy Cycle Insertion Count

EXTGUARD Extra Guard Cycle Insertion between Contiguous Read/Write Access

EDA ED[15:0] Activity

0 Drive ED Bus only on write access

1 Always drive ED Bus except for read access

FLUSH Instruction Cache Write Flush Control

WPOL FLASH, SRAM, PSRAM and CellularRAM Wait Signal Inversion Control

0 Wait if EWAIT = 0.

1 Wait if EWAIT = 1.

PDNE Pseudo SRAM Power Down Mode Control

CKE Burst Mode FLASH Memory Clock Enable Control

CKDLY Burst Mode FLASH Memory Clock Delay Control

CKSR ECLK Pad Slew Rate Control

CKEx ECLK Pad Driving Control

CONSR EADV#, ECS#, EWR#, ERD#, EUB# and ELB# Pad Slew Rate Control

CONEx EADV#, ECS#, EWR#, ERD#, EUB# and ELB# Pad Driving Control

EASR EA[25:0] Pad Slew Rate Control

EAEx EA[25:0] Pad Driving Control

EDSR ED[15:0] Pad Slew Rate Control

EDEx ED[15:0] Pad Driving Control

EMI+0050h Code Cache and Code Prefetch Control Register PREFETCH_CON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0						DWRP8	DPREF	DCACH
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W						R/W	RW	R/W
Reset	0	0	0	0	0	0	0	0						0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0						IWRP8	IPREF	ICACH
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W						R/W	RW	R/W
Reset	0	0	0	0	0	0	0	0						0	0	0

This register is used to control the functions of Code/Data Cache and Code/Data Prefetch. The Code/Data Cache is a low latency memory that can store up to 16 most recently used instruction codes/data. While an instruction/data fetch hits the one in the code/data cache, not only the access time could be minimized, but also the singling to off chip ROM or FLASH Memory could be relieved. In addition, it can also store up to 16 prefetched instruction codes/data while Code/Data Prefetch function is enabled. The Code/Data Prefetch is a sophisticated controller that can predict and fetch the instruction codes/data in advance based on previous code/data fetching sequence. As the Code/Data Prefetch always performs the fetch staffs during the period that the EMI interface is in IDLE state. The bandwidth to off chip memory could be fully utilized. On the other hand, if the instruction/data fetch hits the one of prefetched codes/data, the access time could be minimized and then enhance the overall system performance.

xWRP8 Prefetch Size

0 8 bytes

1 16 bytes

xBn Prefetchable/Cacheable Area

There bit positions determine the prefetchable and cacheable region in which the instruction/data could be cached or prefetched.

xPREF Prefetch Enable

xCACH Cache Enable

EMI+0078h EMI A/D Mux Control Register EMI_ADMUX

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														A2ADVH		MODE
Type														R/W		R/W
Reset														1		XADMUX

MODE A/D Mux memory I/F selection signal. The default value depends on the value of pin GPIO20 at reset.

0 Non-A/D Mux Mode

1 A/D Mux Mode

A2ADVH Address Valid to Address Hold Time

Special note:

:➔The special wire connection between CRE and Addr[25].

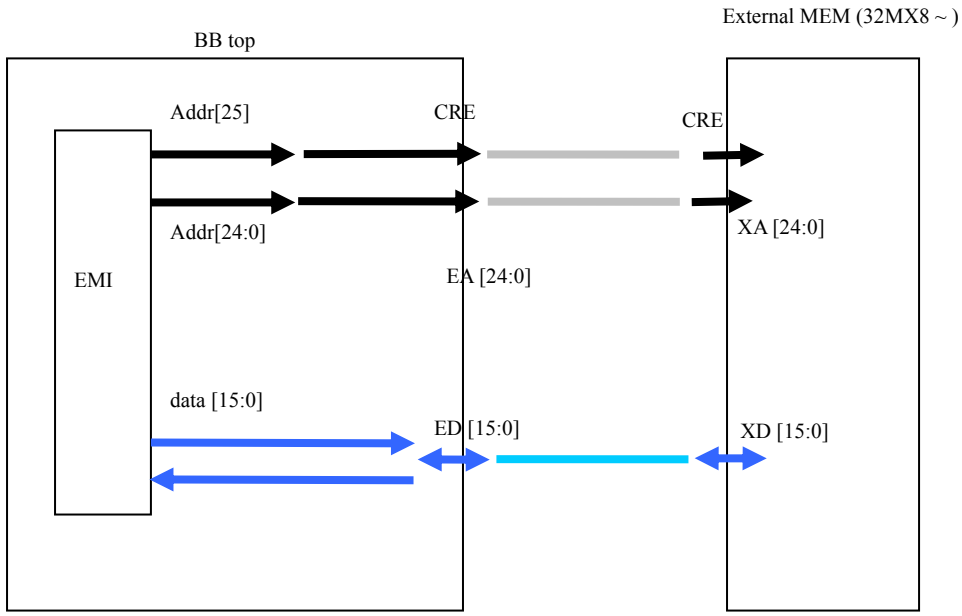
The BB-chip address pin for EMI are EA[24:0], but the system need to support the memory type in the table. If memory is 16-bits mode (data-pin), the max size can reach 512Mbit, but if the memory is 8-bits mode , the max size will be 128Mbits (limited by address pin[24:0]).

Max size support 512Mbit (64Mbyte)

Memory type	Addr-pin	Data-pin	Ad/da-pin(ADMUX-type)	
32Mx16 (ADMUX)	[24:16]	X	[15:0]	
32Mx16(NonADMUX)	[24:0]	[15:0]	X	

32Mx8(only NonADMUX)	[24:0]	[7:0]	X	

1. 8-bits mode (data-pin) ext-MEM , MT6223 can access 32M address location, and support hardware configure by CRE pin (from addr[25]).



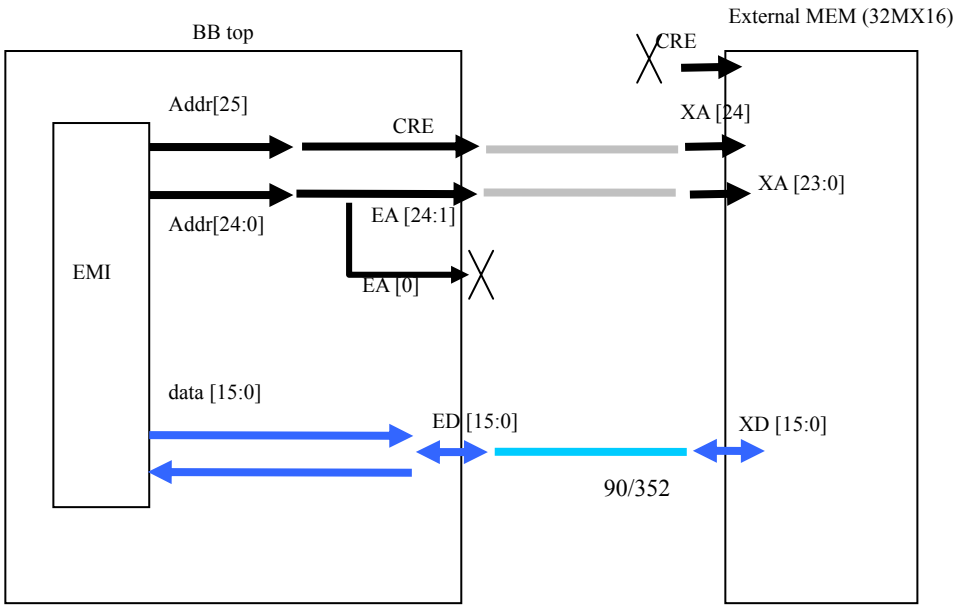
2. 16-bits mode (data-pin) ext-MEM :

(A) If max memory size is 32Mbyte(16MX16)

MT6223 can access 16M address location, and support hardware configure by CRE pin (from addr[25]).

(B) If max memory size is 64Mbyte(32MX16)

MT6223 can access 32M address location, and **only support software configure (without hardware configure, because no extra pin-out for CRE pin)**.



3.7 Internal Memory Interface

3.7.1 System RAM

MT6223 provides one 40K Bytes size of on-chip memory modules acting as System RAM for data access with low latency. Such a module is composed of one high speed synchronous SRAM with AHB Slave Interface connected to the system backbone AHB Bus, as shown in **Figure 20**. The synchronous SRAM operates on the same clock as the AHB Bus and is organized as 32 bits wide with 4 byte-write signals capable for byte operations.

3.7.2 System ROM

The 15K Bytes System ROM is primarily used to store software program for Factory Programming and security-related routines. This module is composed of high-speed ROM with an AHB Slave Interface connected to a system backbone AHB, shown in **Figure 20**. The module operates on the same clock as the AHB and has a 32-bit wide organization.

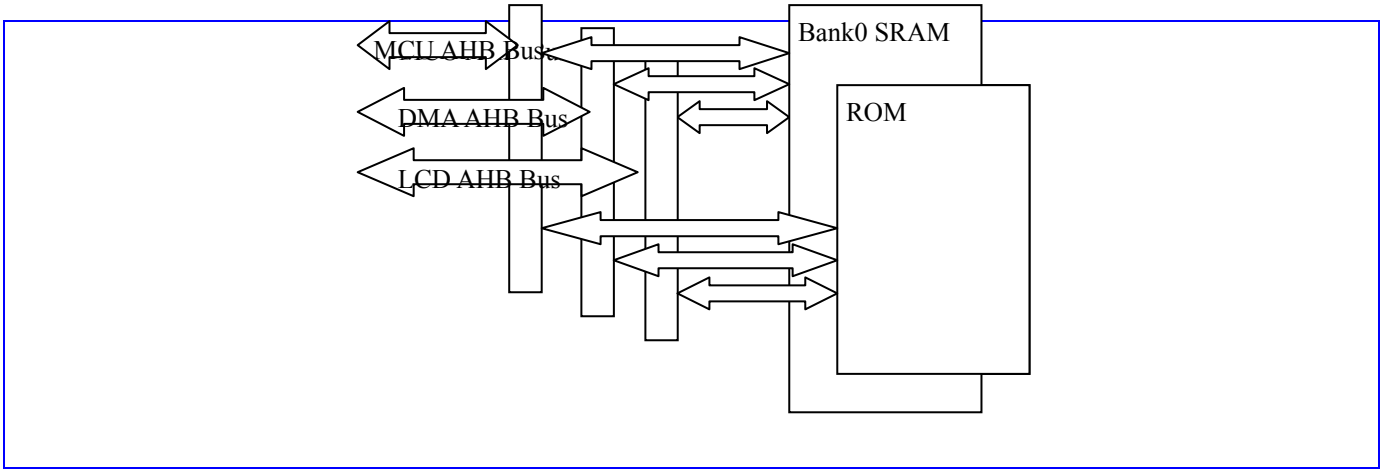


Figure 20: Block Diagram of the Internal Memory Controller

3.8 Alerter

3.8.1 General Description

The output of the Alerter has two sources: one is the enhanced PWM output signal, implemented within the Alerter module; the other is the PDM signal that comes from the DSP domain directly. The output source can be selected via the register ALERTER_CON.

The enhanced PWM has three modes of operation and can generate a signal with programmable frequency and tone volume. The frequency and volume are determined by four registers: ALERTER_CNT1, ALERTER_THRES, ALERTER_CNT2, and ALERTER_CON. ALERTER_CNT1 and ALERTER_CNT2 are the initial counting values for the internal counters counter1 and counter2, respectively.

POWERDOWN signal is applied to power down the Alerter module. When Alerter is deactivated (POWERDOWN=1), the output is in a low state. The waveform of Alerter from the enhanced PWM source in different modes is shown in **Figure 21**.

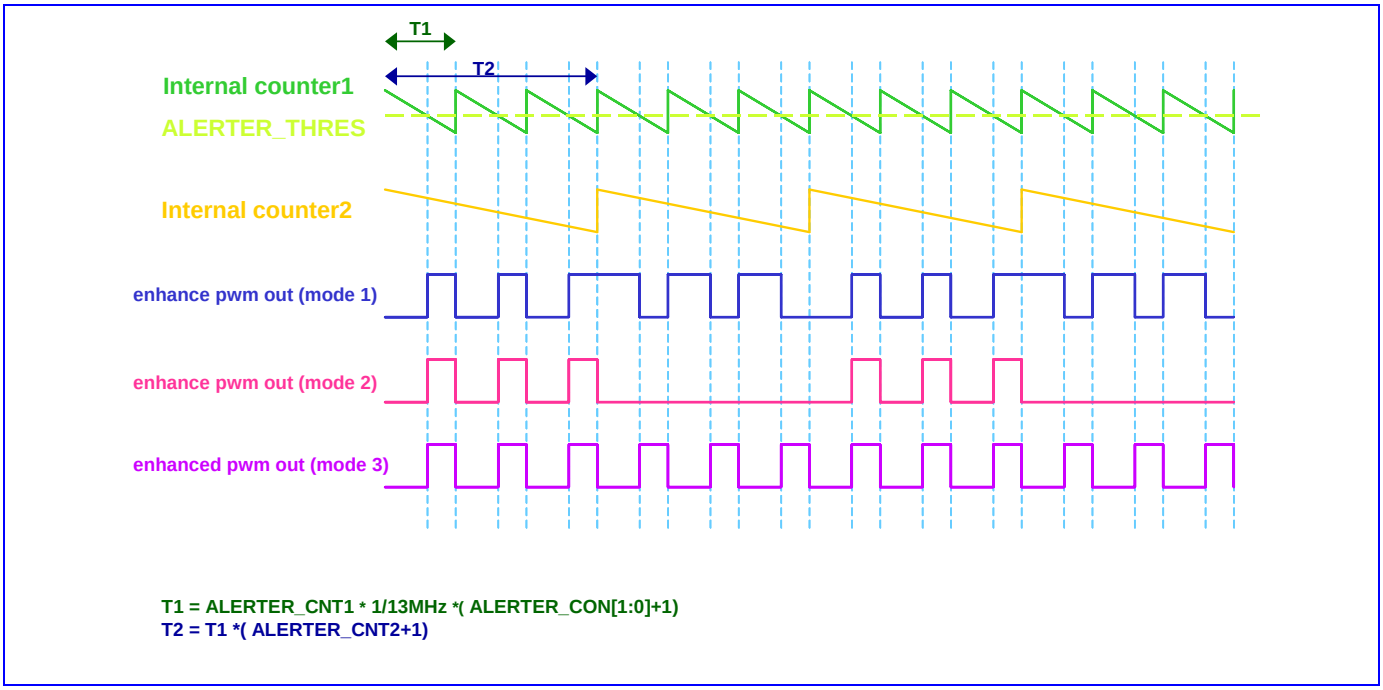


Figure 21 Alerter Waveform

In Mode 1, the polarity of the Alerter output signal, given the relationship between internal counter1 and the programmed threshold, is inverted each time internal counter2 reaches zero.

In Mode 2, each time the internal counter2 reaches zero, the Alerter output signal toggles between the normal PWM signal (i.e. the signal is low for an internal counter1 value greater than or equals to ALERTER_THRES; high when the internal counter1 value is less than ALERTER_THRES) and low state.

In Mode 3, the value of internal counter2 has no effect on output signal. That is, the alerter output signal is low as long as the internal counter 1 value is above the programmed threshold, and is high when the internal counter1 is less than ALERTER_THRES, regardless of internal counter2's value.

The output signal frequency is given by:

$$\begin{cases} \dfrac{13000000}{2\times(ALERTER\_CON[1:0]+1)\times(ALERTER\_CNT1+1)\times(ALERTER\_CNT2+1)} & \text{for mode 1 and mode 2} \\ \dfrac{13000000}{(ALERTER\_CNT1+1)\times(ALERTER\_CON[1:0])} & \text{for mode 3} \end{cases}.$$

The volume of the output signal is given by: $\dfrac{ALERTER\_THRES}{ALERTER\_CNT1+1}$.

3.8.2 Register Definitions

ALTER+0000h Alerter counter1 value register ALERTER_CNT1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ALERTER_CNT1 [15:0]															
Type	R/W															
Reset	FFFFh															

ALERTER_CNT1 Alerter max counter's value. Initial value of internal counter1. In any mode, if ALERTER_CNT1 is written when the internal counter1 is counting, the new start value does not take effect until the next countdown period; i.e. after internal counter1 reaches zero.

ALTER+0004h Alerter threshold value register ALERTER_THRES

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ALERTER_THRES [15:0]															
Type	R/W															
Reset	0															

ALERTER_THRES Threshold value. When the internal counter1 value is greater than or equals to ALERTER_THRES, the Alerter output signal is low; when counter1 is less than ALERTER_THRES, the Alerter output signal is high.

ALTER+0008h Alerter counter2 value register ALERTER_CNT2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ALERTER_CNT2 [5:0]					
Type											R/W					
Reset											111111b					

ALERTER_CNT2 Initial value for internal counter2. The internal counter2 decreases by one each time the internal counter1 counts down to zero; internal counter1 is a nested counter.

ALTER+000Ch Alerter control register ALERTER_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TYPE				MODE			CLK [1:0]	
Type								R/W				R/W			R/W	
Reset								0				0			0	

CLK Select the PWM Waveform clock.

- 00 13 MHz
- 01 13/2 MHz
- 10 13/4 MHz
- 11 13/8 MHz

MODE Select the Alerter mode.

- 00 Mode 1 selected
- 01 Mode 2 selected
- 10 Mode 3 selected

TYPE Select the ALERTER output source from PWM or PDM.

- 0 Output generated from PWM path.

1 Output generated from PDM path.

Note: When the Alerter module is powered down, its output must be kept in low state.

Figure 22 shows the Alerter waveform with the register values.

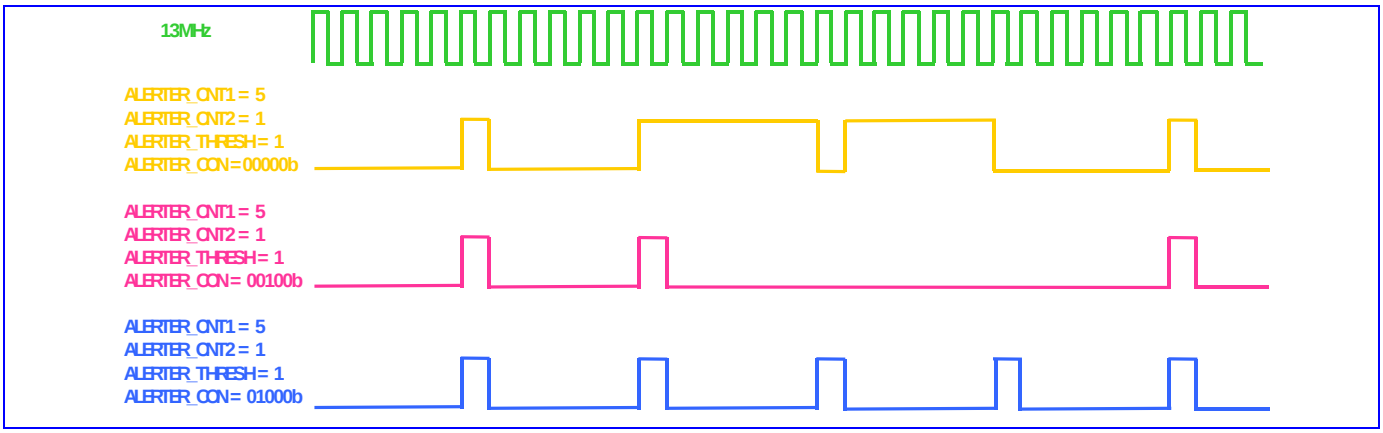


Figure 22 Alerter Output Signal from Enhanced PWM with Register Value Present

3.9 SIM Interface

The MT6223 contains a dedicated smart card interface to allow the MCU access to the SIM card. It can operate via 5 terminals, using SIMVCC, SIMSEL, SIMRST, SIMCLK and SIMDATA.

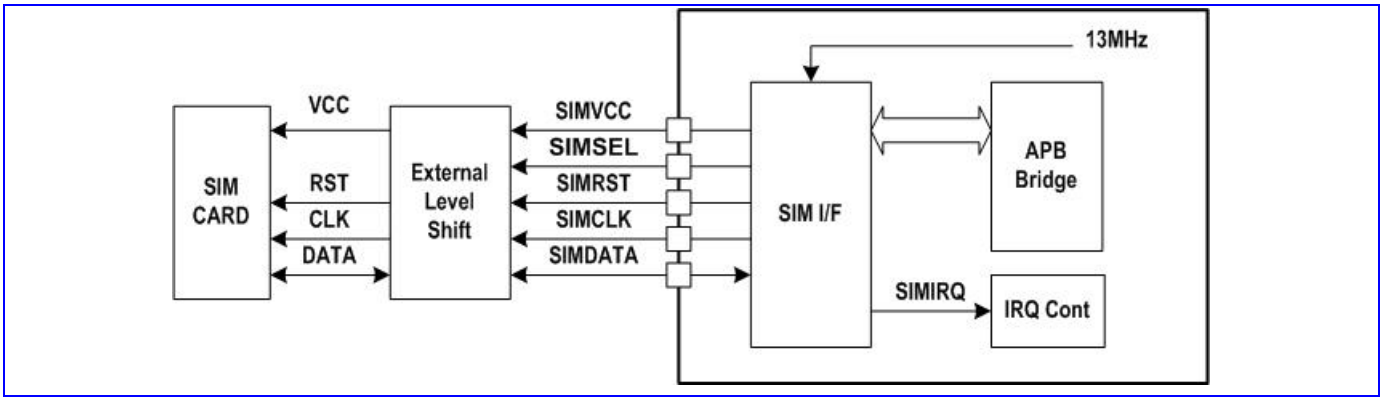


Figure 23 SIM Interface Block Diagram

The SIMVCC is used to control the external voltage supply to the SIM card and SIMSEL determines the regulated smart card supply voltage. SIMRST is used as the SIM card reset signal. Besides, SIMDATA and SIMCLK are used for data exchange purpose.

Basically, the SIM interface acts as a half duplex asynchronous communication port and its data format is composed of ten consecutive bits: a start bit in state Low, eight information bits, and a tenth bit used for parity checking. The data format can be divided into two modes as follows:

Direct Mode (ODD=SDIR=SINV=0)

SB D0 D1 D2 D3 D4 D5 D6 D7 PB

SB: Start Bit (in state Low)

Dx: Data Byte (LSB is first and logic level ONE is High)

PB: Even Parity Check Bit

Indirect Mode (ODD=SDIR=SINV=1)

SB N7 N6 N5 N4 N3 N2 N1 N0 PB

SB: Start Bit (in state Low)

Nx: Data Byte (MSB is first and logic level ONE is Low)

PB: Odd Parity Check Bit

If the receiver gets a wrong parity bit, it will respond by pulling the SIMDATA Low to inform the transmitter and the transmitter will retransmit the character.

When the receiver is a SIM Card, the error response starts 0.5 bits after the PB and it may last for 1~2 bit periods.

When the receiver is the SIM interface, the error response starts 0.5 bits after the PB and lasts for 1.5 bit period.

When the SIM interface is the transmitter, it will take totally 14 bits guard period whether the error response appears. If the receiver shows the error response, the SIM interface will retransmit the previous character again else it will transmit the next character.

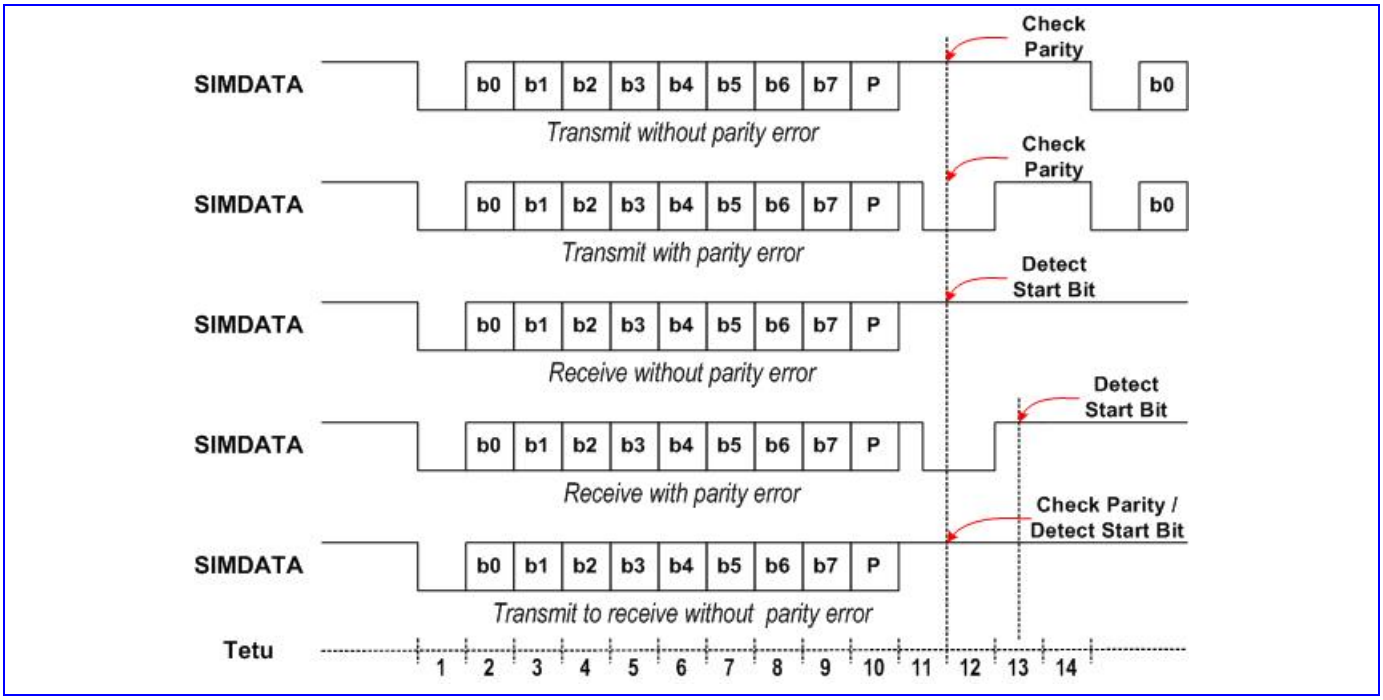


Figure 24 SIM Interface Timing Diagram

3.9.1 Register Definitions

SIM+0000h SIM module control register SIM_CONT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														WRST	CSTOP	SIMON
Type														W	R/W	R/W
Reset														0	0	0

SIMON SIM card power-up/power-down control

0 Initiate the card deactivation sequence

1 Initiate the card activation sequence

CSTOP Enable clock stop mode. Together with CPOL in SIM_CNF register, it determines the polarity of the SIMCLK in this mode.

0 Enable the SIMCLK output.

1 Disable the SIMCLK output

WRST SIM card warm reset control

SIM+0004h SIM module configuration register SIM_CONF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						HFEN	T0EN	T1EN	TOUT	SIMSEL	ODD	SDIR	SINV	CPOL	TXACK	RXACK
Type						R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset						0	0	0	0	0	0	0	0	0	0	0

RXACK SIM card reception error handshake control

0 Disable character receipt handshaking

1 Enable character receipt handshaking

TXACK SIM card transmission error handshake control

0 Disable character transmission handshaking

1 Enable character transmission handshaking

CPOL SIMCLK polarity control in clock stop mode

0 Make SIMCLK stop in LOW level

1 Make SIMCLK stop in HIGH level

SINV Data Inverter.

0 Not invert the transmitted and received data

1 Invert the transmitted and received data

SDIR Data Transfer Direction

0 LSB is transmitted and received first

1 MSB is transmitted and received first

ODD Select odd or even parity

0 Even parity

1 Odd parity

SIMSEL SIM card supply voltage select

0 SIMSEL pin is set to LOW level

1 SIMSEL pin is set to HIGH level

TOUT SIM work waiting time counter control

0 Disable Time-Out counter

1 Enable Time-Out counter

T1EN T=1 protocol controller control

0 Disable T=1 protocol controller

1 Enable T=1 protocol controller

T0EN T=0 protocol controller control

0 Disable T=0 protocol controller

1 Enable T=0 protocol controller

HFEN Hardware flow control

0 Disable hardware flow control

1 Enable hardware flow control

SIM +0008h SIM Baud Rate Register SIM_BRR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						ETU[8:0]									SIMCLK[1:0]	
Type						R/W									R/W	
Reset						372d									01	

SIMCLK Set SIMCLK frequency

00 13/2 MHz

01 13/4 MHz

10 13/8 MHz

13/32 MHz

ETU Determines the duration of elementary time unit in unit of SIMCLK

SIM +0010h SIM interrupt enable register SIM_IRQEN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						EDCERR	T1END	RXERR	T0END	SIMOFF	ATRERR	TXERR	TOUT	OVRUN	RXTIDE	TXTIDE
Type						R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset						0	0	0	0	0	0	0	0	0	0	0

For all these bits

0 Interrupt is disabled

1 Interrupt is enabled

SIM +0014h SIM module status register SIM_STS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						EDCERR	T1END	RXERR	T0END	SIMOFF	ATRERR	TXERR	TOUT	OVRUN	RXTIDE	TXTIDE
Type						R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R	R
Reset						—	—	—	—	—	—	—	—	—	—	—

TXTIDE Transmit FIFO tide mark reached interrupt occurred

RXTIDE Receive FIFO tide mark reached interrupt occurred

OVRUN Transmit/Receive FIFO overrun interrupt occurred

TOUT Between character timeout interrupt occurred

TXERR Character transmission error interrupt occurred

ATRERR ATR start time-out interrupt occurred

SIMOFF Card deactivation complete interrupt occurred

T0END Data Transfer handled by T=0 Controller completed interrupt occurred

RXERR Character reception error interrupt occurred

T1END Data Transfer handled by T=1 Controller completed interrupt occurred

EDCERR T=1 Controller CRC error occurred

SIM +0020h SIM retry limit register SIM_RETRY

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						TXRETRY								RXRETRY		
Type						R/W								R/W		
Reset						3h								3h		

RXRETRY Specify the max. numbers of receive retries that are allowed when parity error has occurred.

TXRETRY Specify the max. numbers of transmit retries that are allowed when parity error has occurred.

SIM +0024h SIM FIFO tide mark register SIM_TIDE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TXTIDE[3:0]								RXTIDE[3:0]			
Type					R/W								R/W			
Reset					0h								0h			

RXTIDE Trigger point for RXTIDE interrupt

TXTIDE Trigger point for TXTIDE interrupt

SIM +0030h Data register used as Tx/Rx Data Register SIM_DATA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DATA[7:0]							
Type									R/W							
Reset									—							

DATA Eight data digits. These correspond to the character being read or written

SIM +0034h SIM FIFO count register SIM_COUNT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												COUNT[4:0]				
Type												R/W				
Reset												0h				

COUNT The number of characters in the SIM FIFO when read, and flushes when written.

SIM +0040h SIM activation time register SIM_ATIME

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ATIME[15:0]															
Type	R/W															
Reset	AFC7h															

ATIME The register defines the duration, in SIM clock cycles, of the time taken for each of the three stages of the card activation process

SIM +0044h SIM deactivation time register SIM_DTIME

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DTIME[11:0]											
Type					R/W											
Reset					3E7h											

DTIME The register defines the duration, in 13MHz clock cycles, of the time taken for each of the three stages of the card deactivation sequence

SIM +0048h Character to character waiting time register SIM_WTIME

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WTIME[15:0]															
Type	R/W															

Reset	983h

WTIME Maximum interval between the leading edge of two consecutive characters in 4 ETU unit

SIM +004Ch Block to block guard time register SIM_GTIME

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													GTIME			
Type													R/W			
Reset													10d			

GTIME Minimum interval between the leading edge of two consecutive characters sent in opposite directions in ETU unit

SIM +0050h Block to error signal time register SIM_ETIME

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ETIME					
Type													R/W			
Reset													15d			

ETIME The register defines the interval, in 1/16 ETU unit, between the end of transmitted parity bit and time to check parity error signal sent from SIM card.

SIM +0060h SIM command header register: INS SIM_INS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								INSD	SIMINS[7:0]							
Type								R/W	R/W							
Reset								0h	0h							

SIMINS This field should be identical to the INS instruction code. When writing to this register, the T=0 controller will be activated and data transfer will be initiated.

INSD

0 T=0 controller receives data from the SIM card

1 T=0 controller sends data to the SIM card

SIM +0064h SIM command header register: P3 SIM_P3 (ICC_LEN)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								SIMP3[8:0]								
Type								R/W								
Reset								0h								

SIMP3 This field should be identical to the P3 instruction code. It should be written prior to the SIM_INS register. While the data transfer is going on, this field shows the no. of the remaining data to be sent or to be received

SIM +0068h SIM procedure byte register: SW1 SIM_SW1 (ICC_LEN)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SIMSW1[7:0]							
Type									R							
Reset									0h							

SIMSW1 This field holds the last received procedure byte for debug purpose. When the T0END interrupt occurred, it keeps the SW1 procedure byte.

SIM +006Ch SIM procedure byte register: SW2 SIM_SW2 (ICC_EDC)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SIMSW2[7:0]							
Type									R							
Reset									0h							

SIMSW2 This field holds the SW2 procedure byte

3.9.2 SIM Card Insertion and Removal

The detection of physical connection to the SIM card and card removal is done by the external interrupt controller or by GPIO.

3.9.3 Card Activation and Deactivation

The card activation and deactivation sequence both are controlled by H/W. The MCU initiates the activation sequence by writing a “1” to bit 0 of the SIM_CON register, and then the interface performs the following activation sequence:

- Assert SIMRST LOW
- Set SIMVCC at HIGH level and SIMDATA in reception mode
- Enable SIMCLK clock
- De-assert SIMRST HIGH (required if it belongs to active low reset SIM card)

The final step in a typical card session is contact deactivation in order that the card is not electrically damaged. The deactivation sequence is initiated by writing a “0” to bit 0 of the SIM_CONT register, and then the interface performs the following deactivation sequence:

- Assert SIMRST LOW
- Set SCIMCLK at LOW level
- Set SIMDATA at LOW level

- Set SIMVCC at LOW level

3.9.4 Answer to Reset Sequence

After card activation, a reset operation results in an answer from the card consisting of the initial character TS, followed by at most 32 characters. The initial character TS provides a bit synchronization sequence and defines the conventions to interpret data bytes in all subsequent characters.

On reception of the first character, TS, MCU should read this character, establish the respective required convention and reprogram the related registers. These processes should be completed prior to the completion of reception of the next character. And then, the remainder of the ATR sequence is received, read via the SIM_DATA in the selected convention and interpreted by the S/W.

The timing requirement and procedures for ATR sequence are handled by H/W and shall meet the requirement of ISO 7816-3 as shown in **Figure 25**.

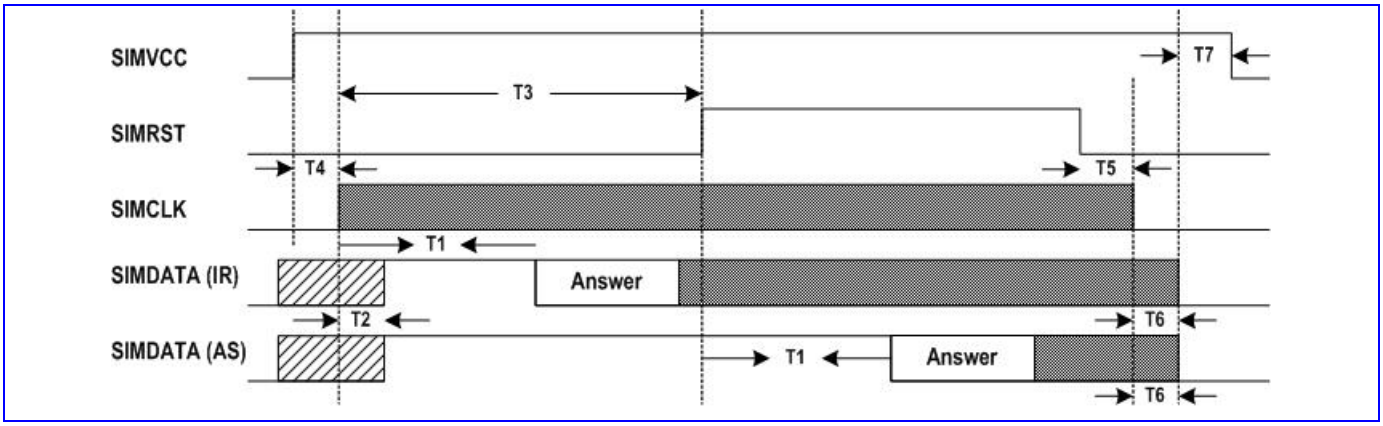


Figure 25 Answer to Reset Sequence

Time	Value	Comment
T1	> 400 SIMCLK	SIMCLK start to ATR appear
T2	< 200 SIMCLK	SIMCLK start to SIMDATA in reception mode
T3	> 40000 SIMCLK	SIMCLK start to SIMRST High
T4	—	SIMVCC High to SIMCLK start
T5	—	SIMRST Low to SIMCLK stop
T6	—	SIMCLK stop to SIMDATA Low
T7	—	SIMDATA Low to SIMVCC Low

Table 19 Answer to Reset Sequence Time-Out Condition

3.9.5 SIM Data Transfer

Two transfer modes are provided, either in software controlled byte by byte fashion or in a block fashion using T=0 controller and DMA controller. In both modes, the time-out counter could be enabled to monitor the elapsed time between two consecutive bytes.

3.9.5.1 Byte Transfer Mode

This mode is used during ATR and PPS procedure. In this mode, the SIM interface only ensures error free character transmission and reception.

Receiving Character

Upon detection of the start-bit sent by SIM card, the interface transforms into reception mode and the following bits are shifted into an internal register. If no parity error is detected or character-receive handshaking is disabled, the received-character is written into the SIM FIFO and the SIM_COUNT register is increased by one. Otherwise, the SIMDATA line is held low at 0.5 etu after detecting the parity error for 1.5 etus, and the character is re-received. If a character fails to be received correctly for the RXRETRY times, the receive-handshaking is aborted and the last-received character is written into the SIM FIFO, the SIM_COUNT is increased by one and the RXERR interrupt is generated

When the number of characters held in the receive FIFO exceeds the level defined in the SIM_TIDE register, a RXTIDE interrupt is generated. The number of characters held in the SIM FIFO can be determined by reading the SIM_COUNT register and writing to this register will flush the SIM FIFO.

Sending Character

Characters that are to be sent to the card are first written into the SIM FIFO and then automatically transmitted to the card at timed intervals. If character-transmit handshaking is enabled, the SIMDATA line is sampled at 1 etu after the parity bit. If the card indicates that it did not receive the character correctly, the character is retransmitted a maximum of TXRETRY times before a TXERR interrupt is generated and the transmission is aborted. Otherwise, the succeeding byte in the SIM FIFO is transmitted.

If a character fails to be transmitted and a TXERR interrupt is generated, the interface needs to be reset by flushing the SIM FIFO before any subsequent transmit or receive operation.

When the number of characters held in the SIM FIFO falls below the level defined in the SIM_TIDE register, a TXTIDE interrupt is generated. The number of characters held in the SIM FIFO can be determined by reading the SIM_COUNT register and writing to this register will flush the SIM FIFO.

3.9.5.2 Block Transfer Mode

Basically, the SIM interface is designed to work in conjunction with the T=0 protocol controller and the DMA controller during non-ATR and non-PPS phase, though it is still possible for software to service the data transfer manually like in byte transfer mode if necessary and thus the T=0 protocol should be controlled by software.

The T=0 controller is accessed via four registers representing the instruction header bytes INS and P3, and the procedure bytes SW1 and SW2. These registers are:

SIM_INS, SIM_P3

SIM_SW1, SIM_SW2

During characters transfer, SIM_P3 holds the number of characters to be sent or to be received and SIM_SW1 holds the last received procedure byte including NULL, ACK, NACK and SW1 for debug purpose.

Data Receive Instruction

Data Receive Instructions receive data from the SIM card. It is instantiated as the following procedure.

```
Enable the T=0 protocol controller by setting the T0EN bit to 1 in SIM_CONF register
Program the SIM_TIDE register to 0x0000 (TXTIDE = 0, RXTIDE = 0)
Program the SIM_IRQEN to 0x019C (Enable RXERR, TXERR, T0END, TOUT and OVRUN interrupts)
Write CLA, INS, P1, P2 and P3 into SIM FIFO
```

Program the DMA controller :

DMA*n*_MSBSRC and DMA*n*_LSBSRC : address of SIM_DATA register

DMA*n*_MSBDST and DMA*n*_LSBDST : memory address reserved to store the received characters

DMA*n*_COUNT : identical to P3 or 256 (if P3 == 0)

DMA*n*_CON : 0x0078

Write P3 into SIM_P3 register and then INS into SIM_INS register (Data Transfer is initiated now)

Enable the Time-out counter by setting the TOUT bit to 1 in SIM_CONF register

Start the DMA controller by writing 0x8000 into the DMA*n*_START register to

Upon completion of the Data Receive Instruction, T0END interrupt will be generated and then the Time-out counter should be disabled by setting the TOUT bit back to 0 in SIM_CONF register.

If error occurs during data transfer (RXERR, TXERR, OVRUN or TOUT interrupt is generated), the SIM card should be deactivated first and then activated prior subsequent operations.

Data Send Instruction

Data Send Instructions send data to the SIM card. It is instantiated as the following procedure.

Enable the T=0 protocol controller by setting the T0EN bit to 1 in SIM_CONF register

Program the SIM_TIDE register to 0x0100 (TXTIDE = 1, RXTIDE = 0)

Program the SIM_IRQEN to 0x019C (Enable RXERR, TXERR, T0END, TOUT and OVRUN interrupts)

Write CLA, INS, P1, P2 and P3 into SIM FIFO

Program the DMA controller :

DMA*n*_MSBSRC and DMA*n*_LSBSRC : memory address reserved to store the transmitted characters

DMA*n*_MSBDST and DMA*n*_LSBDST : address of SIM_DATA register

DMA*n*_COUNT : identical to P3

DMA*n*_CON : 0x0074

Write P3 into SIM_P3 register and then (0x0100 | INS) into SIM_INS register (Data Transfer is initiated now)

Enable the Time-out counter by setting the TOUT bit to 1 in SIM_CONF register

Start the DMA controller by writing 0x8000 into the DMA*n*_START register

Upon completion of the Data Send Instruction, T0END interrupt will be generated and then the Time-out counter should be disabled by setting the TOUT bit back to 0 in SIM_CONF register.

If error occurs during data transfer (RXERR, TXERR, OVRUN or TOUT interrupt is generated), the SIM card should be deactivated first and then activated prior subsequent operations.

3.10 Keypad Scanner

3.10.1 General Description

The keypad can be divided into two parts: one is the keypad interface including 6 columns and 5 rows with one dedicated power-key, as shown in **Fig. 1** 錯誤! 找不到參照來源。錯誤! 找不到參照來源。; the other is the key detection block which provides key pressed, key released and de-bounce mechanisms. Each time the key is pressed or released, i.e. something different in the 5 x 6 matrix or power-key, the key detection block senses the change and recognizes if a key has been pressed

or released. Whenever the key status changes and is stable, a KEYPAD IRQ is issued. The MCU can then read the key(s) pressed directly in KP_HI_KEY, KP_MID_KEY and KP_LOW_KEY registers. To ensure that the key pressed information is not missed, the status register in keypad is not read-cleared by APB read command. The status register can only be changed by the key-pressed detection FSM.

This keypad can detect one or two key-pressed simultaneously with any combination. Fig. 2 shows one key pressed condition. Fig. 3 (a) and Fig. 3 (b) illustrate two keys pressed cases. Since the key press detection depends on the HIGH or LOW level of the external keypad interface, if keys are pressed at the same time and there exists a key that is on the same column and the same row with the other keys, the pressed key cannot be correctly decoded. For example, if there are three key presses: key1 = (x1, y1), key2 = (x2, y2), and key3 = (x1, y2), then both key3 and key4 = (x2, y1) are detected, and therefore they cannot be distinguished correctly. Hence, the keypad can detect only one or two keys pressed simultaneously at any combination. More than two keys pressed simultaneously in a specific pattern retrieve the wrong information.

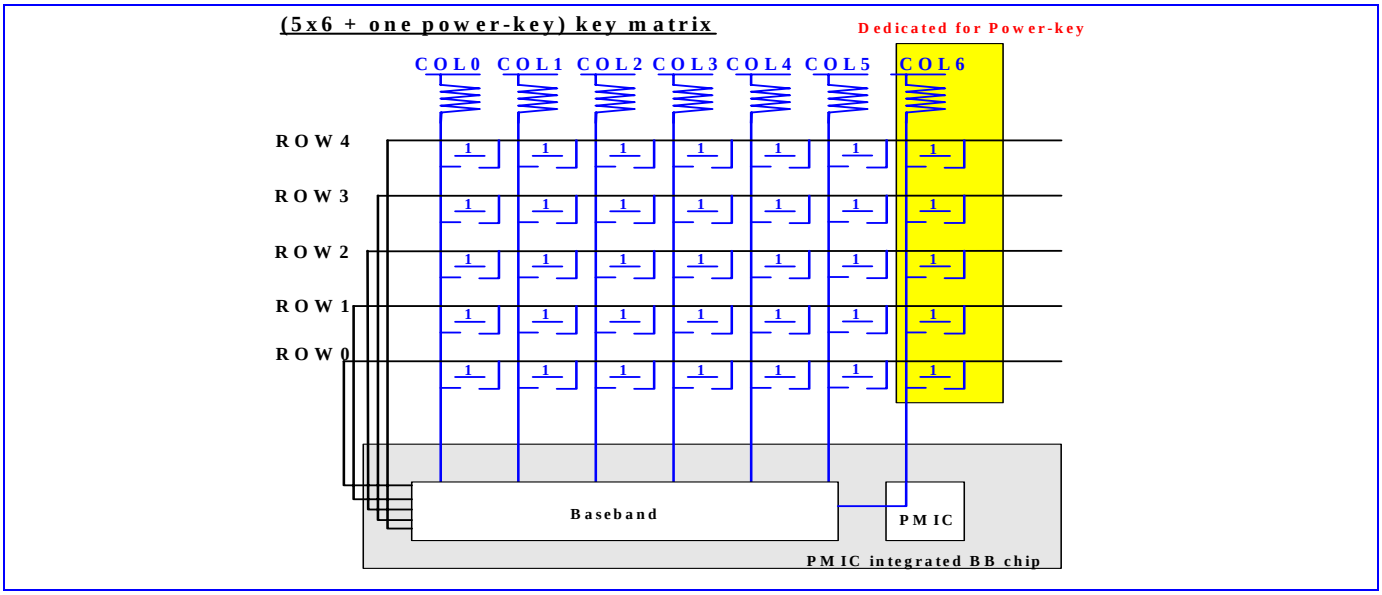


Fig. 1 5x6 matrix with one power-key

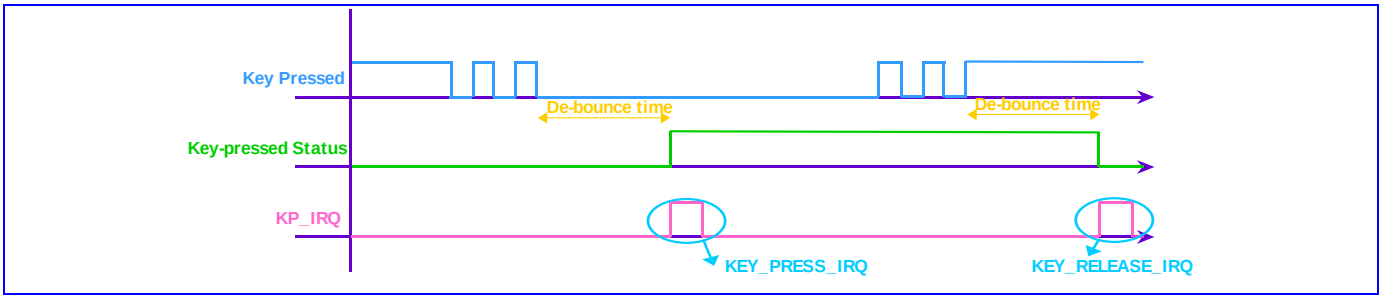


Fig. 2. One key pressed with de-bounce mechanism denoted

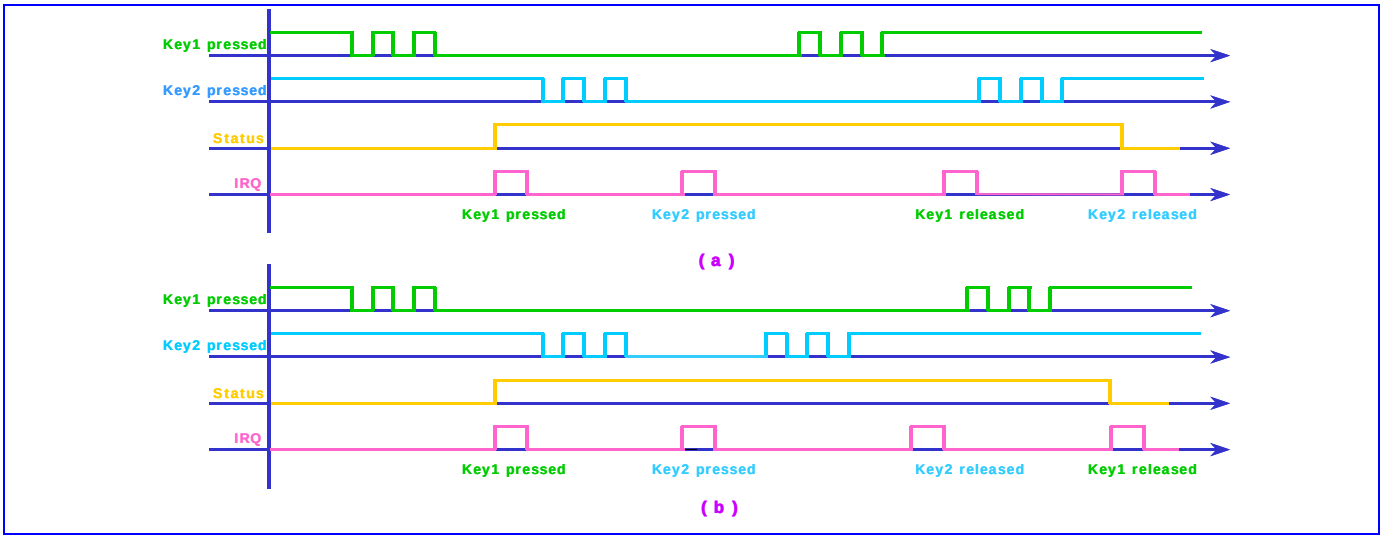


Fig. 3**. (a)** Two keys pressed, case 1 **(b)** Two keys pressed, case 2

3.10.2 Register Definitions

KP +0000h Keypad status KP_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STA
Type																RO
Reset																0

STA This register indicates the keypad status. The register is not cleared by the read operation.

0 No key pressed

1 Key pressed

KP +0004h Keypad scanning output, the lower 16 keys KP_LOW_KEY

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEYS [15:0]															
Type	RO															
Reset	FFFFh															

KP +0008h Keypad scanning output, the medium 16 keys KP_MID_KEY

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEYS [31:16]															
Type	RO															
Reset	FFFFh															

KP+000Ch Keypad scanning output, the higher 4 keys KP_HIGH_KEY

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														KEYS[34:32]		
Type														RO		
Reset														7'h		

These two registers list the status of 35 keys on the keypad but KEY[6], KEY[13], KEY[20], KEY[27], KEY[34] is dedicated for power key. When the MCU receives the KEYPAD IRQ, both two registers must be read. If any key is pressed, the relative bit is set to 0.

KEYS Status list of the 35 keys.

KP +00010h De-bounce period setting KP_DEBOUNCE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DEBOUNCE [13:0]													
Type			R/W													
Reset			400h													

This register defines the waiting period before key press or release events are considered stale.

DEBOUNCE De-bounce time = KP_DEBOUNCE/32 ms.

3.11 LCD Interface

MT6223 contains a versatile LCD controller which is optimized for multimedia applications. This controller supports many types of LCD modules and contains a rich feature set to enhance the functionality. These features are:

- Up to 320 x 240 resolution
- Supports 8-bpp (RGB332), 12-bpp (RGB444), 16-bpp (RGB565), 18-bit (RGB666) and 24-bit (RGB888) color depths
- 2 Layers Overlay with individual vertical and horizontal size, vertical and horizontal offset, source key, opacity and display rotation control(90°,180°, 270°, mirror and mirror then 90°, 180° and 270°)
- Color Look-Up Table

For parallel LCD modules, this special LCD controller can reuse external memory interface or use dedicated 8/9-bit parallel interface to access them and 8080 type interface is supported. It can transfer the display data from the internal SRAM or external SRAM/Flash Memory to the off-chip LCD modules.
For serial LCD modules, this interface performs parallel to serial conversion and both 8- and 9- bit serial interface is supported. The 8-bit serial interface uses four pins – LSCE#, LSDA, LSCK and LSA0 – to enter commands and data. Meanwhile, the 9-bit serial interface uses three pins – LSCE#, LSDA and LSCK – for the same purpose. Data read is not available with the serial interface and data entered must be 8 bits.

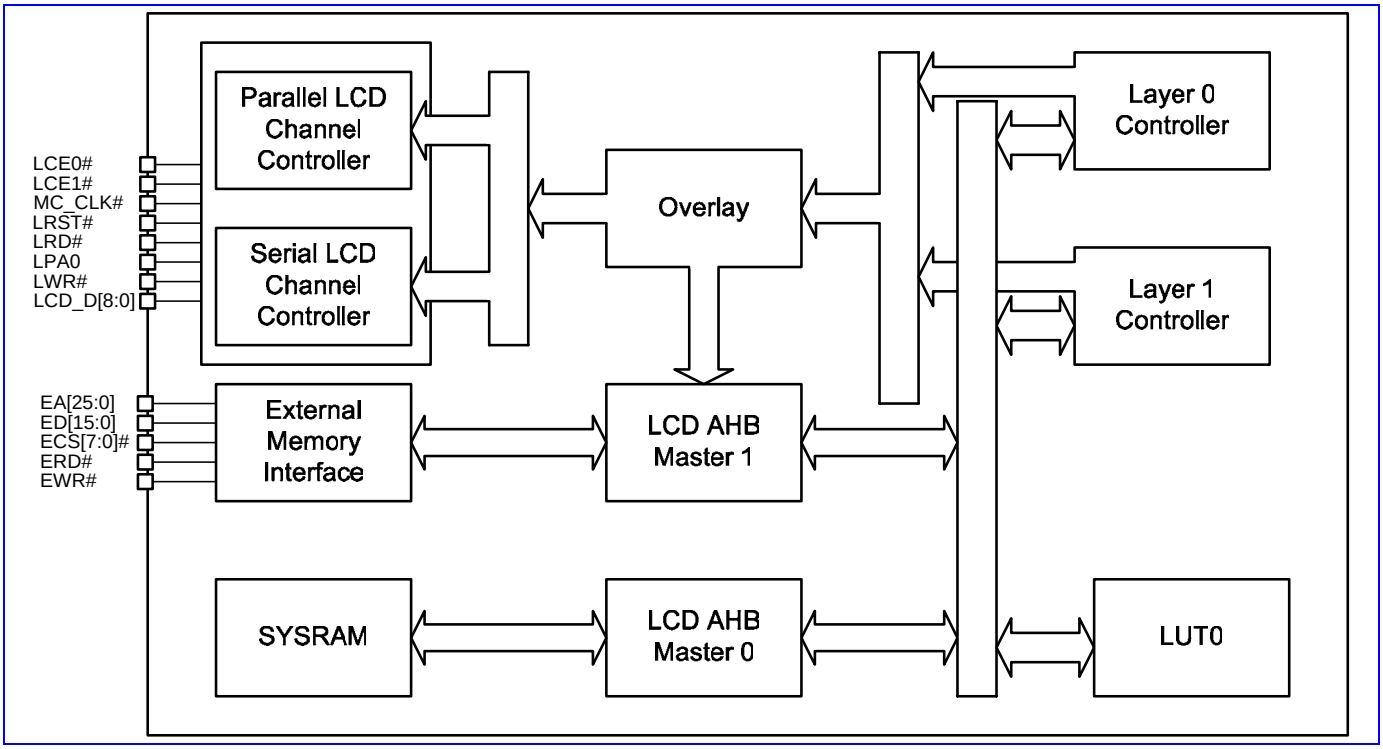


Figure 26 LCD Interface Block Diagram

Figure 27 shows the timing diagram of this serial interface. When the block is idle, LSCK is forced LOW and LSCE# is forced HIGH. Once the data register contains data and the interface is enabled, LSCE# is pulled LOW and remain LOW for the duration of the transmission.

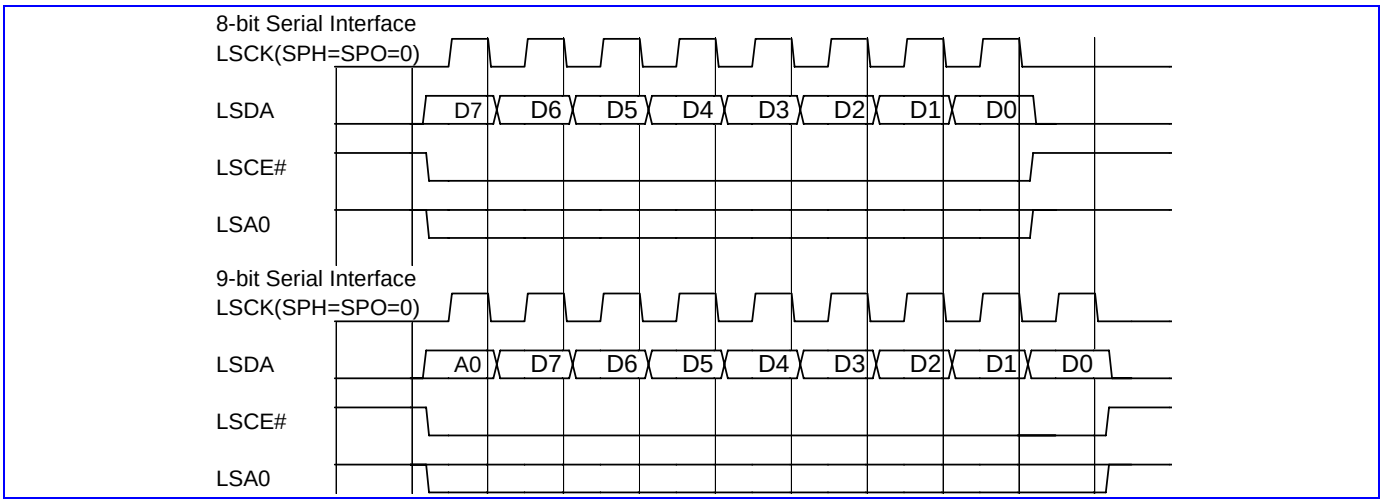


Figure 27 LCD Interface Transfer Timing Diagram

In addition, MT6223C provide another feature, that is, LCD controller can be used for memory card. Only MC_CLK and LCD_D[4:0] is used for MSDC interface. LCD controller generates MC_CLK when writing or reading offset 6000h. Figure 28 illustrating the timing of memory card interface. The timing of memory card data and clock is shared with LCD_PCNF0. Please see detailed description in register definition. MC_CLK is shared with BPI_BUS2 and BPI_BUS3, and the MC_CLK output is enabled by ACIF_CON0[15:14]. To control memory cards, extra ACIF_CON0 settings are required. LCD_D0~LCD_D4 has nature of pull-down when in input mode, which may violate MSDC access nature (ex. Most SD card expect data to be high when in idle). Besides the MC_CLK output enable setting, in order to accommodate MSDC nature, PD (pull-down) of LCD_D0 to LCD_D4 should be disabled by use of ACIF_CON0[12]. As for more detail of ACIF_CON0 setting, please refer to GPIO functional specification.

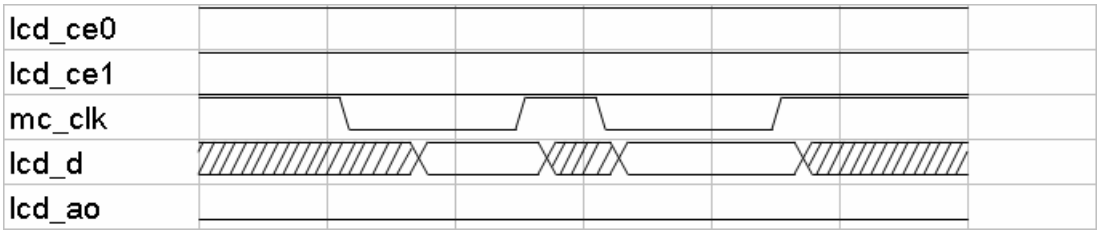


Figure 28 MSDC Interface Timing

LCD interface can control 2 LCMs and 1 memory card at the same time, users can select the types of LCM0 and LCM1 be serial or parallel. The data pins are shared by serial, parallel interfaces and MSDC interface, which are shown as below.

LCD IO	*D8*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
Parallel IF	*PD8*	*PD7*	*Pd6*	*PD5*	*PD4*	*PD3*	*PD2*	*PD1*	*PD0*
Serial IF	*SCLK*	*SDA*	*SA0*						
MSDC IF					*MCCM*	*MCDA3*	*MCDA2*	*MCDA1*	*MCDA0*

3.11.1 Register Definitions

LCD +0000h LCD Interface Status Register LCD_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RUN
Type																R
Reset																0

RUN LCD Interface Running Status

LCD +0004h LCD Interface Interrupt Enable Register LCD_INTEN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CPL
Type																R/W
Reset																0

CPL LCD Frame Transfer Complete Interrupt Control

LCD +0008h LCD Interface Interrupt Status Register LCD_INTSTA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CPL
Type																R
Reset																0

CPL LCD Frame Transfer Complete Interrupt

LCD +000Ch LCD Interface Frame Transfer Register LCD_START

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	START															
Type	R/W															
Reset	0															

START Start Control of LCD Frame Transfer

LCD +0010h LCD Parallel/Serial Interface Reset Register LCD_RSTB

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RSTB
Type																R/W

Reset																1

RSTB Parallel/Serial LCD Module Reset Control

LCD +0014h LCD Serial Interface Configuration Register LCD _SCNF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	26M	13M					CSP1	CSP0				8/9	DIV		SPH	SPO
Type	R/W	R/W					R/W	R/W				R/W	R/W		R/W	R/W

SPO Clock Polarity Control
SPH Clock Phase Control
DIV Serial Clock Divide Select Bits
8/9 8-bit or 9-bit Interface Selection
CSP0 Serial Interface Chip Select 0 Polarity Control
CSP1 Serial Interface Chip Select 1 Polarity Control

LCD +0018h LCD Parallel Interface Configuration Register 0 LCD_PCNF0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	C2WS		C2WH		C2RS											
Type	R/W		R/W		R/W											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	26M	13M	DW	WST								RLT				
Type	R/W	R/W	R/W	R/W								R/W				

RLT Read Latency Time. It controls the low period for LCD chip-select or MSDC clock when read.
WST Write Wait State Time. It controls the low period for LCD chip-select or MSDC clock when write.
DW 8-bit data width.
0 parallel 9-bit interface
1 parallel 8-bit interface
C2RS Chip Select (LPCE#) to Read Strobe (LRD#) Setup Time for LCD Interface
C2WH Chip Select (LPCE#) to Write Strobe (LWR#) Hold Time for LCD Interface; Data to Clock (MC_CLK#) Hold Time for MSDC Interface.
C2WS Chip Select (LPCE#) to Write Strobe (LWR#) Setup Time for LCD Interface

LCD +001Ch LCD Parallel Interface Configuration Register 1 LCD_PCNF1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	C2WS		C2WH		C2RS											
Type	R/W		R/W		R/W											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	26M	13M	DW	WST								RLT				
Type	R/W	R/W	R/W	R/W								R/W				

RLT Read Latency Time
WST Write Wait State Time
DW 8-bit data width.
0 parallel 9-bit interface
1 parallel 8-bit interface
C2RS Chip Select (LPCE#) to Read Strobe (LRD#) Setup Time
C2WH Chip Select (LPCE#) to Write Strobe (LWR#) Hold Time
C2WS Chip Select (LPCE#) to Write Strobe (LWR#) Setup Time

LCD +0020h LCD IO Configuration Register LCD_IOCNF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name															CE1_SEL	CE0_SEL
Type															R/W	R/W
Reset															0	0

Since parallel interface and serial interface share the same IO channel, this register field is used to select which interface controls IO channel 0 and 1.

CE0_SEL Select parallel interface or serial interface for CE0
- 0 parallel interface selected (LCD_PCNF0 selected)
- 1 serial interface selected (LCD_SCNF0 selected)

CE1_SEL Select parallel interface or serial interface for CE1
- 0 parallel interface selected (LCD_PCNF1 selected)
- 1 serial interface selected (LCD_SCNF1 selected)

LCD +4000/4100h LCD Parallel Interface Data Register 0 LCD_PDAT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DATA							
Type									R/W							

DATA Writing to LCD+4100 will drive LPA0 low while sending this data out in parallel BANK0, otherwise will drive LPA0 high

LCD +5000/5100h LCD Parallel Interface Data Register 1 LCD_PDAT1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DATA							
Type									R/W							

DATA Writing to LCD+5100 will drive LPA0 low while sending this data out in parallel BANK1, otherwise will drive LPA0 high

LCD +6000h MSDC Data Register 1 MSDC_DAT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DATA							
Type									R/W							

DATA Writing or reading LCD+6000 will generate msdc clock output, but LCD_A0 is low.

LCD +9000/9100h LCD Serial Interface Data Register 0 LCD_SDAT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DATA							
Type									W							

DATA Writing to LCD+9000 will drive LSA0 low while sending this data out in serial BANK0, otherwise will drive LSA0 high

LCD +8000/8100h LCD Serial Interface Data Register 1 LCD_SDAT1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DATA							
Type									W							

DATA Writing to LCD+8000 will drive LSA0 low while sending this data out in serial BANK1, otherwise will drive LSA0 high

LCD +0040h Main Window Size Register LCD_MWINSIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ROW									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							COLUMN									
Type							R/W									

COLUMN Virtual Image Window Column Size

ROW Virtual Image Window Row Size

LCD +0050h Region of Interest Window Control Register LCD_WROICON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN0	EN1					PERIOD									
Type	R/W	R/W					R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COM_MSB	ENC	W2M	DISCON	COMMAND					FORMAT						
Type	R/W	R/W	R/W	R/W	R/W					R/W						

FORMAT LCD Module Data Format

0000000	8bit	1cycle/1pixel	RGB3.3.2	RRRGGGBB
0000001		1cycle/1pixel	RGB3.3.2	BBGGGRRR
0001000		3cycle/2pixel	RGB4.4.4	RRRRGGGG BBBBRRRR GGGGBBBB
0001011		3cycle/2pixel	RGB4.4.4	GGGGRRRR RRRRBBBB BBBBGGGG
0010000		2cycle/1pixel	RGB5.6.5	RRRRRGGG GGGBBBBB
0010011		2cycle/1pixel	RGB5.6.5	GGGRRRRR BBBBBGGG
0011000		3cycle/1pixel	RGB6.6.6	RRRRRRXX GGGGGGXX BBBBBBXX
0011100		3cycle/1pixel	RGB6.6.6	XXRRRRRR XXGGGGGG XXBBBBBB
0100000		3cycle/1pixel	RGB8.8.8	RRRRRRRR GGGGGGGG BBBBBBBB
1000000	9bit	1cycle/1pixel	RGB3.3.2	RRRGGGBBX
1000001		1cycle/1pixel	RGB3.3.2	BBGGGRRRX
1001100		3cycle/2pixel	RGB4.4.4	XRRRRGGGG XBBBBRRRR XGGGGBBBB
1001101		3cycle/2pixel	RGB4.4.4	XBBBBGGGG XRRRRBBBB XGGGGRRRR

1001000		3cycle/2pixel	RGB4.4.4	RRRRGGGGX BBBBRRRRX GGGGBBBBX
1001001		3cycle/2pixel	RGB4.4.4	BBBBGGGGX RRRRBBBBX GGGGRRRRX
1010000		2cycle/1pixel	RGB5.6.5	RRRRRGGGX GGGBBBBBX
1010001		2cycle/1pixel	RGB5.6.5	BBBBBGGGX GGGRRRRRX
1011000		2cycle/1pixel	RGB6.6.6	RRRRRRGGG GGGBBBBBB
1011011		2cycle/1pixel	RGB6.6.6	BBBBBBGGG GGGRRRRRR
1100000		3cycle/1pixel	RGB8.8.8	RRRRRRRRX GGGGGGGGX BBBBBBBBX
1100011		3cycle/1pixel	RGB8.8.8	BBBBBBBBX GGGGGGGGX RRRRRRRRX

COMMAND Number of Commands to be sent to LCD module

DISCON Block Write Enable Control. By setting both DISCON and W2M to 1, this LCD accelerator will update the ROI window within the MAIN Window

W2M Enable Data Address Increasing After Each Data Transfer. When this bit enabled, the data width would be forced to 16-bit no matter how LCD_WROICON[6] is set.

COM_MSB Command put in MSB, which means that zero is padded at LSB bit. Otherwise, command is put in LSB.

ENC Command Transfer Enable Control

PERIOD Waiting Period Between Two Consecutive Data Transfers

ENn Layer Window Enable Control

LCD +0054h Region of Interest Window Offset Register LCD_WROIOFS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							Y-OFFSET									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							X-OFFSET									
Type							R/W									

X-OFFSET ROI Window Column Offset

Y-OFFSET ROI Window Row Offset

LCD +0058h Region of Interest Window Command Start Address Register LCD_WROICADD

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADDR															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADDR															
Type	R/W															

ADDR ROI Window Command Address

LCD +005Ch Region of Interest Window Data Start Address Register LCD_WROIDADD

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADDR															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADDR															
Type	R/W															

ADDR ROI Window Data Address

LCD +0060h Region of Interest Window Size Register LCD_WROISIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ROW									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							COLUMN									
Type							R/W									

COLUMNROI Window Column Size

ROW ROI Window Row Size

LCD +0070h Layer 0 Window Control Register LCD_L0WINCON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRCKEY															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC	KEYEN	ROTATE			PLAEN		OPAEN	OPA							SWP
Type	R/W	R/W	R/W			R/W		R/W	R/W							R/W

SWP Swap high byte and low byte of pixel data

OPA Opacity Value Setting

OPAEN Opacity Enable Control

PLAEN Color Palette Enable Control

ROTATE Rotation Configuration

- 000 0 degree rotation
- 001 90 degree rotation anti-counterclockwise
- 010 180 degree rotation anti-counterclockwise
- 011 270 degree rotation anti-counterclockwise
- 100 Horizontal flip
- 101 Horizontal flip then 90 degree rotation anti-counterclockwise
- 110 Horizontal flip then 180 degree rotation anti-counterclockwise
- 111 Horizontal flip then 270 degree rotation anti-counterclockwise

KEYEN Source Key Enable Control

SRC Disable auto-increment of the source pixel address

SRCKEY Source Key Value

LCD +0074h Layer 0 Window Display Offset Register LCD_L0WINOFS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							Y-OFFSET									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							X-OFFSET									
Type							R/W									

Y-OFFSET Layer 0 Window Row Offset

X-OFFSET Layer 0 Window Column Offset

+0078h Layer 0 Window Display Start Address Register LCD_L0WINADD

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADDR															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADDR															
Type	R/W															

ADDR Layer 0 Window Data Address

LCD +007Ch Layer 0 Window Size LCD_L0WINSIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ROW									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							COLUMN									
Type							R/W									

ROW Layer 0 Window Row Size

COLUMN Layer 0 Window Column Size

LCD +0080h Layer 1 Window Control Register LCD_L1WINCON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRCKEY															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC	KEYEN	ROTATE			PLAEN		OPAEN	OPA							SWP
Type	R/W	R/W	R/W			R/W		R/W	R/W							R/W

SWP Swap high byte and low byte of pixel data

OPA Opacity Value Setting

OPAEN Enable Opacity Control

PLAEN Color Palette Enable Control

ROTATE Rotation Configuration

- 000 0 degree rotation
- 001 90 degree rotation
- 010 180 degree rotation
- 011 270 degree rotation
- 100 Vertical flip
- 101 Reserved
- 110 Horizontal flip
- 111 Reserved

KEYEN Source Key Enable Control

SRC Disable auto-increment of the source pixel address

SRCKEY Source-Key

LCD +0084h Layer 1 Window Display Offset Register LCD_L1WINOFS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							Y-OFFSET									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name							X-OFFSET
Type							R/W

X-OFFSET Layer 1 Window Row Offset

Y-OFFSET Layer 1 Window Column Offset

LCD +0088h Layer 1 Window Display Start Address Register LCD_L1WINADD

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADDR															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADDR															
Type	R/W															

ADDR Layer 1 Window Data Address

LCD +008Ch Layer 1 Window Size LCD_L1WINSIZE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							ROW									
Type							R/W									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							COLUMN									
Type							R/W									

COLUMNLayer 1 Window Column Size

ROW Layer 1 Window Row Size

LCD +C000h~C1FCh LCD Interface Color Palette LUT 0 Registers LCD_PAL0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LUT0															
Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LUT0															
Type	R/W															

LUT0 These Bits Set LUT0 Data in RGB565 Format

LCD +C200h~C23C LCD Interface Command/Parameter Registers LCD_COMD

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	C0								COMM							
Type	R/W								R/W							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	C0								COMM							
Type	R/W								R/W							

COMM Command Data and Parameter Data for LCD Module

C0 Write to ROI Command Address if C0 = 1, otherwise write to ROI Data Address

3.12 UART

3.12.1 General Description

The baseband chipset houses three UARTs. The UARTs provide full duplex serial communication channels between

baseband chipset and external devices.

The UART has M16C450 and M16550A modes of operation, which are compatible with a range of standard software drivers. The extensions have been designed to be broadly software compatible with 16550A variants, but certain areas offer no consensus.

In common with the M16550A, the UART supports word lengths **from five to eight bits**, **an optional parity bit** and one or two stop bits, and is fully programmable by an 8-bit CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided. The UART also includes two DMA handshake lines, used to indicate when the FIFOs are ready to transfer data to the CPU. Interrupts can be generated from any of the 10 sources.

Note: The UART has been designed so that all internal operations are synchronized by the CLK signal. This synchronization results in minor timing differences between the UART and the industry standard 16550A device, which means that the core is not clock for clock identical to the original device.

After a hardware reset, the UART is in M16C450 mode. Its FIFOs can be enabled and the UART can then enter M16550A mode. The UART adds further functionality beyond M16550A mode. Each of the extended functions can be selected individually under software control.

The UART provides more powerful enhancements than the industry-standard 16550:

- Hardware flow control. This feature is very useful when the ISR latency is hard to predict and control in the embedded applications. The MCU is relieved of having to fetch the received data within a fixed amount of time.
- Output of an IR-compatible electrical pulse with a width 3/16 of that of a regular bit period.

Note: In order to enable any of the enhancements, the Enhanced Mode bit, EFR[4], must be set. If EFR[4] is not set, IER[7:5], FCR[5:4], ISR[5:4] and MCR[7:6] cannot be written. The Enhanced Mode bit ensures that the UART is backward compatible with software that has been written for 16C450 and 16550A devices.

Figure 29 shows the block diagram of the UART device.

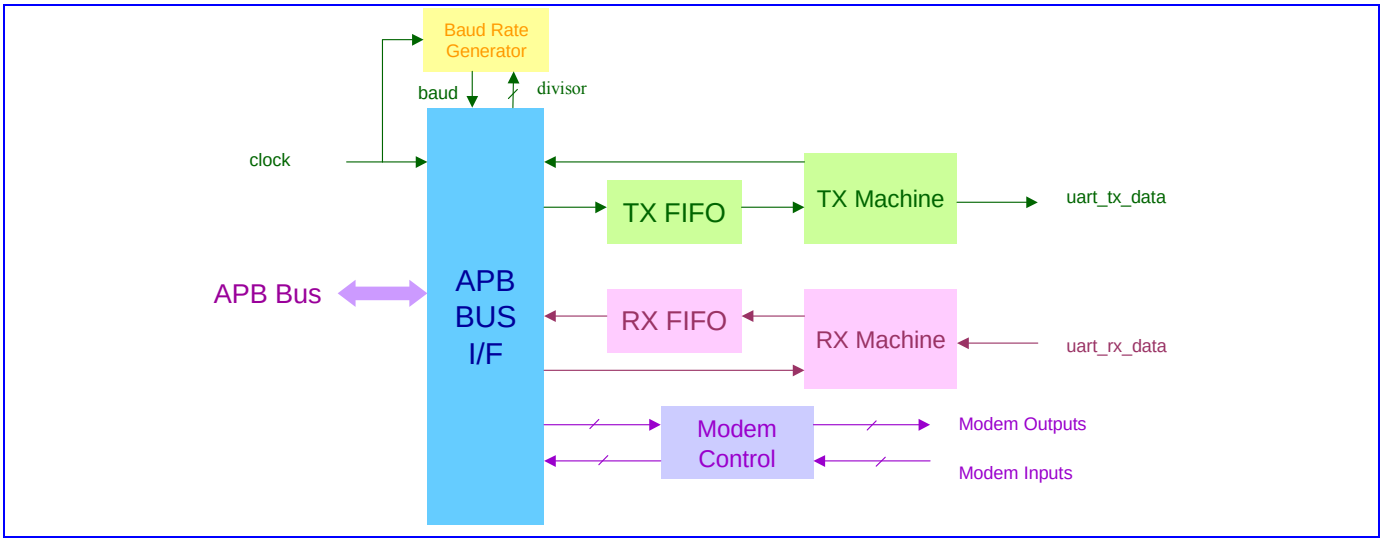


Figure 29 Block Diagram of UART

3.12.2 Register Definitions

n = 1, 2, 3; for uart1, uart2 and uart3 respectively.

UARTn+0000h RX Buffer Register UARTn_RBR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RBR[7:0]							
Type									RO							

RBR RX Buffer Register. Read-only register. The received data can be read by accessing this register.

Modified when LCR[7] = 0.

UARTn+0000h TX Holding Register UARTn_THR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									THR[7:0]							
Type									WO							

THR TX Holding Register. Write-only register. The data to be transmitted is written to this register, and then sent to the PC via serial communication.

Modified when LCR[7] = 0.

UARTn+0004h Interrupt Enable Register UARTn_IER

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CTSI	RTSI	XOFFI	X	EDSSI	ELSI	ETBEI	ERBFI
Type									R/W							
Reset									0							

IER By storing a '1' to a specific bit position, the interrupt associated with that bit is enabled. Otherwise, the interrupt is disabled.

IER[3:0] are modified when LCR[7] = 0.

IER[7:4] are modified when LCR[7] = 0 & EFR[4] = 1.

CTSI Masks an interrupt that is generated when a rising edge is detected on the CTS modem control line.

Note*:* This interrupt is only enabled when hardware flow control is enabled.

0 Unmask an interrupt that is generated when a rising edge is detected on the CTS modem control line.

1 Mask an interrupt that is generated when a rising edge is detected on the CTS modem control line.

RTSI Masks an interrupt that is generated when a rising edge is detected on the RTS modem control line.

Note*:* This interrupt is only enabled when hardware flow control is enabled.

0 Unmask an interrupt that is generated when a rising edge is detected on the RTS modem control line.

1 Mask an interrupt that is generated when a rising edge is detected on the RTS modem control line.

XOFFI Masks an interrupt that is generated when an XOFF character is received.

Note*:* This interrupt is only enabled when software flow control is enabled.

0 Unmask an interrupt that is generated when an XOFF character is received.

1 Mask an interrupt that is generated when an XOFF character is received.

EDSSI When set ("1"), an interrupt is generated if DDCD, TERI, DDSR or DCTS (MSR[4:1]) becomes set.

0 No interrupt is generated if DDCD, TERI, DDSR or DCTS (MSR[4:1]) becomes set.

1 An interrupt is generated if DDCD, TERI, DDSR or DCTS (MSR[4:1]) becomes set.

ELSI When set ("1"), an interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.

0 No interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.

1 An interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.

ETBEI When set ("1"), an interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level.

0 No interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level.

1 An interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level

ERBFI When set ("1"), an interrupt is generated if the RX Buffer contains data.

0 No interrupt is generated if the RX Buffer contains data.

1 An interrupt is generated if the RX Buffer contains data.

UARTn+0008h Interrupt Identification Register UARTn_IIR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFOE		ID4	ID3	ID2	ID1	ID0	NINT
Type									RO							
Reset									0	0	0	0	0	0	0	1

IIR Identify if there are pending interrupts; ID4 and ID3 are presented only when EFR[4] = 1.

The following table gives the IIR[5:0] codes associated with the possible interrupts:

IIR[5:0]	Priority Level	Interrupt	Source
000001	-	No interrupt pending	
000110	1	Line Status Interrupt	BI, FE, PE or OE set in LSR
000100	2	RX Data Received	RX Data received or RX Trigger Level reached.
001100	2	RX Data Timeout	Timeout on character in RX FIFO.
000010	3	TX Holding Register Empty	TX Holding Register empty or TX FIFO Trigger Level reached.

000000	4	Modem Status change	DDCD, TERI, DDSR or DCTS set in MSR
010000	5	Software Flow Control	XOFF Character received
100000	6	Hardware Flow Control	CTS or RTS Rising Edge

Table 20 The IIR[5:0] codes associated with the possible interrupts

Line Status Interrupt: A RX Line Status Interrupt (IIR[5:0`] == 000110b) is generated if ELSI (IER[2]) is set and any of BI, FE, PE or OE (LSR[4:1]) becomes set. The interrupt is cleared by reading the Line Status Register.

RX Data Received Interrupt: A RX Received interrupt (IER[5:0] == 000100b) is generated if EFRBI (IER[0]) is set and either RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached. The interrupt is cleared by reading the RX Buffer Register or the RX FIFO (if enabled).

RX Data Timeout Interrupt:

When virtual FIFO mode is disabled, RX Data Timeout Interrupt is generated if all of the following apply:

FIFO contains at least one character;

The most recent character was received longer than four character periods ago (including all start, parity and stop bits);

The most recent CPU read of the FIFO was longer than four character periods ago.

The timeout timer is restarted on receipt of a new byte from the RX Shift Register, or on a CPU read from the RX FIFO.

The RX Data Timeout Interrupt is enabled by setting EFRBI (IER[0]) to 1, and is cleared by reading RX FIFO.

When virtual FIFO mode is enabled, RX Data Timeout Interrupt is generated if all of the following apply:

FIFO is empty;

The most recent character was received longer than four character periods ago (including all start, parity and stop bits);

The most recent CPU read of the FIFO was longer than four character periods ago.

The timeout timer is restarted on receipt of a new byte from the RX Shift Register.

RX Holding Register Empty Interrupt: A TX Holding Register Empty Interrupt (IIR[5:0] = 000010b) is generated if ETRBI (IER[1]) is set and either the TX Holding Register or, if FIFOs are enabled, the TX FIFO becomes empty. The interrupt is cleared by writing to the TX Holding Register or TX FIFO if FIFO enabled.

Modem Status Change Interrupt: A Modem Status Change Interrupt (IIR[5:0] = 000000b) is generated if EDSSI (IER[3]) is set and either DDCD, TERI, DDSR or DCTS (MSR[3:0]) becomes set. The interrupt is cleared by reading the Modem Status Register.

Software Flow Control Interrupt: A Software Flow Control Interrupt (IIR[5:0] = 010000b) is generated if Software Flow Control is enabled and XOFFI (IER[5]) becomes set, indicating that an XOFF character has been received. The interrupt is cleared by reading the Interrupt Identification Register.

Hardware Flow Control Interrupt: A Hardware Flow Control Interrupt (IER[5:0] = 100000b) is generated if Hardware Flow Control is enabled and either RTSI (IER[6]) or CTSI (IER[7]) becomes set indicating that a rising edge has been detected on either the RTS/CTS Modem Control line. The interrupt is cleared by reading the Interrupt Identification Register.

UARTn+0008h FIFO Control Register UARTn_FCR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RFTL1	RFTL0	TFTL1	TFTL0	DMA1	CLRT	CLRR	FIFOE
Type									WO							

FCR FCR is used to control the trigger levels of the FIFOs, or flush the FIFOs.

FCR[7:6] is modified when LCR != BFh

FCR[5:4] is modified when LCR != BFh & EFR[4] = 1

FCR[4:0] is modified when LCR != BFh

FCR[7:6] RX FIFO trigger threshold

0 1

1 6

2 12

3 RXTRIG

FCR[5:4] TX FIFO trigger threshold

0 1

4

8

14 (FIFOSIZE - 2)

DMA1 This bit determines the DMA mode, which the TXRDY and RXRDY pins support. TXRDY and RXRDY act to support single-byte transfers between the UART and memory (DMA mode 0) or multiple byte transfers (DMA mode1). Note that this bit has no effect unless the FIFOE bit is set as well

0 The device operates in DMA Mode 0.

The device operates in DMA Mode 1.

TXRDY – mode0: Goes active (low) when the TX FIFO or the TX Holding Register is empty. Becomes inactive when a byte is written to the Transmit channel.

TXRDY – mode1: Goes active (low) when there are no characters in the TX FIFO. Becomes inactive when the TX FIFO is full.

RXRDY – mode0: Becomes active (low) when at least one character is in the RX FIFO or the RX Buffer Register is full. Becomes inactive when there are no more characters in the RX FIFO or RX Buffer register.

RXRDY – mode1: Becomes active (low) when the RX FIFO Trigger Level is reached or an RX FIFO Character Timeout occurs. Goes inactive when the RX FIFO is empty.

CLRT Clear Transmit FIFO. This bit is self-clearing.

0 Leave TX FIFO intact.

1 Clear all the bytes in the TX FIFO.

CLRR Clear Receive FIFO. This bit is self-clearing.

0 Leave RX FIFO intact.

1 Clear all the bytes in the RX FIFO.

FIFOE FIFO Enabled. This bit must be set to 1 for any of the other bits in the registers to have any effect.

0 Disable both the RX and TX FIFOs.

1 Enable both the RX and TX FIFOs.

UARTn+000Ch Line Control Register UARTn_LCR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLAB	SB	SP	EPS	PEN	STB	WLS1	WLS0
Type									R/W							
Reset									0	0	0	0	0	0	0	0

LCR Line Control Register. Determines characteristics of serial communication signals.

Modified when LCR[7] = 0.

DLAB Divisor Latch Access Bit.

0 The RX and TX Registers are read/written at Address 0 and the IER register is read/written at Address 4.

1 The Divisor Latch LS is read/written at Address 0 and the Divisor Latch MS is read/written at Address 4.

SB Set Break

0 No effect

1 SOUT signal is forced into the “0” state.

SP Stick Parity

0 No effect.

The Parity bit is forced into a defined state, depending on the states of EPS and PEN:

If EPS=1 & PEN=1, the Parity bit is set and checked = 0.

If EPS=0 & PEN=1, the Parity bit is set and checked = 1.

EPS Even Parity Select

0 When EPS=0, an odd number of ones is sent and checked.

1 When EPS=1, an even number of ones is sent and checked.

PEN Parity Enable

0 The Parity is neither transmitted nor checked.

1 The Parity is transmitted and checked.

STB Number of STOP bits

0 One STOP bit is always added.

1 Two STOP bits are added after each character is sent; unless the character length is 5 when 1 STOP bit is added.

WLS1, 0 Word Length Select.

0 5 bits

6 bits

7 bits

8 bits

UARTn+0010h Modem Control Register UARTn_MCR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF STATUS	IR ENABLE	X	LOOP	OUT2	OUT1	RTS	DTR
Type									R/W							
Reset									0	0	0	0	0	0	0	0

MCR Modem Control Register. Control interface signals of the UART.

MCR[4:0] are modified when LCR[7] = 0,

MCR[7:6] are modified when LCR[7] = 0 & EFR[4] = 1.

XOFF Status This is a read-only bit.

0 When an XON character is received.

1 When an XOFF character is received.LOOP Loop-back control bit.

0 No loop-back is enabled.

1 Loop-back mode is enabled.

OUT2 Controls the state of the output NOUT2, even in loop mode.

0 NOUT2=1.

1 NOUT2=0.

OUT1 Controls the state of the output NOUT1, even in loop mode.

0 NOUT1=1.

1 NOUT1=0.

RTS Controls the state of the output NRTS, even in loop mode.

0 NRTS=1.

1 NRTS=0.

DTR Control the state of the output NDTR, even in loop mode.

0 NDTR=1.

1 NDTR=0.

UARTn+0014h Line Status Register UARTn_LSR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFOERR	TEMT	THRE	BI	FE	PE	OE	DR
Type									R/W							
Reset									0	1	1	0	0	0	0	0

LSR Line Status Register.

Modified when LCR[7] = 0.

FIFOERR RX FIFO Error Indicator.

0 No PE, FE, BI set in the RX FIFO.

1 Set to 1 when there is at least one PE, FE or BI in the RX FIFO.

TEMT TX Holding Register (or TX FIFO) and the TX Shift Register are empty.

0 Empty conditions below are not met.

1 If FIFOs are enabled, the bit is set whenever the TX FIFO and the TX Shift Register are empty. If FIFOs are disabled, the bit is set whenever TX Holding Register and TX Shift Register are empty.

THRE Indicates if there is room for TX Holding Register or TX FIFO is reduced to its Trigger Level.

0 Reset whenever the contents of the TX FIFO are more than its Trigger Level (FIFOs are enabled), or whenever TX Holding Register is not empty(FIFOs are disabled).

1 Set whenever the contents of the TX FIFO are reduced to its Trigger Level (FIFOs are enabled), or whenever TX Holding Register is empty and ready to accept new data (FIFOs are disabled).

BI Break Interrupt.

0 Reset by the CPU reading this register

1 If the FIFOs are disabled, this bit is set whenever the SIN is held in the 0 state for more than one transmission time (START bit + DATA bits + PARITY + STOP bits).

If the FIFOs are enabled, this error is associated with a corresponding character in the FIFO and is flagged when this byte is at the top of the FIFO. When a break occurs, only one zero character is loaded into the FIFO: the next character transfer is enabled when SIN goes into the marking state and receives the next valid start bit.

FE Framing Error.

0 Reset by the CPU reading this register

1 If the FIFOs are disabled, this bit is set if the received data did not have a valid STOP bit. If the FIFOs are enabled, the state of this bit is revealed when the byte it refers to is the next to be read.

PE Parity Error

0 Reset by the CPU reading this register

1 If the FIFOs are disabled, this bit is set if the received data did not have a valid parity bit. If the FIFOs are enabled, the state of this bit is revealed when the referred byte is the next to be read.

OE Overrun Error.

0 Reset by the CPU reading this register.

1 If the FIFOs are disabled, this bit is set if the RX Buffer was not read by the CPU before new data from the RX Shift Register overwrote the previous contents.

If the FIFOs are enabled, an overrun error occurs when the RX FIFO is full and the RX Shift Register becomes full. OE is set as soon as this happens. The character in the Shift Register is then overwritten, but not transferred to the FIFO.

DR Data Ready.

0 Cleared by the CPU reading the RX Buffer or by reading all the FIFO bytes.

1 Set by the RX Buffer becoming full or by a byte being transferred into the FIFO.

UARTn+0018h Modem Status Register UARTn_MSR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS
Type									R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset									Input	Input	Input	Input	0	0	0	0

Note: After a reset, D4-D7 are inputs. A modem status interrupt can be cleared by writing ‘0’ or set by writing ‘1’ to this register. D0-D3 can be written to.

Modified when LCR[7] = 0.

MSR Modem Status Register

DCD Data Carry Detect.

When Loop = "0", this value is the complement of the NDCD input signal.

When Loop = "1", this value is equal to the OUT2 bit in the Modem Control Register.

RI Ring Indicator.

When Loop = "0", this value is the complement of the NRI input signal.

When Loop = "1", this value is equal to the OUT1 bit in the Modem Control Register.

DSR Data Set Ready

When Loop = "0", this value is the complement of the NDSR input signal.

When Loop = "1", this value is equal to the DTR bit in the Modem Control Register.

CTS Clear To Send.

When Loop = "0", this value is the complement of the NCTS input signal.

When Loop = "1", this value is equal to the RTS bit in the Modem Control Register.

DDCD Delta Data Carry Detect.

0 The state of DCD has not changed since the Modem Status Register was last read

1 Set if the state of DCD has changed since the Modem Status Register was last read.

TERI Trailing Edge Ring Indicator

0 The NRI input does not change since this register was last read.

1 Set if the NRI input changes from “0” to “1” since this register was last read.

DDSR Delta Data Set Ready

0 Cleared if the state of DSR has not changed since this register was last read.

1 Set if the state of DSR has changed since this register was last read.

DCTS Delta Clear To Send

0 Cleared if the state of CTS has not changed since this register was last read.

1 Set if the state of CTS has changed since this register was last read.

UARTn+001Ch Scratch Register UARTn_SCR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SCR[7:0]							
Type									R/W							

A general purpose read/write register. After reset, its value is un-defined.

Modified when LCR[7] = 0.

UARTn+0000h Divisor Latch (LS) UARTn_DLL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLL[7:0]							
Type									R/W							
Reset									1							

UARTn+0004h Divisor Latch (MS) UARTn_DLM

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLL[7:0]							
Type									R/W							
Reset									0							

Note: DLL & DLM can only be updated if DLAB is set (“1”).. Note too that division by 1 generates a BAUD signal that is constantly high.

Modified when LCR[7] = 1.

The table below shows the divisor needed to generate a given baud rate from CLK inputs of 13, 26 MHz and 52 MHz. The effective clock enable generated is 16 x the required baud rate.

BAUD	13MHz	26MHz	52MHz
110	7386	14773	29545
300	2708	5417	10833

1200	677	1354	2708
2400	338	677	1354
4800	169	339	677
9600	85	169	339
19200	42	85	169
38400	21	42	85
57600	14	28	56
115200	6	14	28

Table 21 Divisor needed to generate a given baud rate

UARTn+0008h Enhanced Feature Register UARTn_EFR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AUTO CTS	AUTO RTS	D5	ENABLE -E	SW FLOW CONT[3:0]			
Type									R/W	R/W	R/W	R/W	R/W			
Reset									0	0	0	0	0			

*NOTE: Only when LCR=BF'h

Auto CTS Enables hardware transmission flow control

0 Disabled.

1 Enabled.

Auto RTS Enables hardware reception flow control

0 Disabled.

1 Enabled.

Enable-E Enable enhancement features.

0 Disabled.

1 Enabled.

CONT[3:0] Software flow control bits.

00xx No TX Flow Control

10xx Transmit XON1/XOFF1 as flow control bytes

01xx Transmit XON2/XOFF2 as flow control bytes

11xx Transmit XON1 & XON2 and XOFF1 & XOFF2 as flow control words

xx00 No RX Flow Control

xx10 Receive XON1/XOFF1 as flow control bytes

xx01 Receive XON2/XOFF2 as flow control bytes

xx11 Receive XON1 & XON2 and XOFF1 & XOFF2 as flow control words

UARTn+0010h XON1 UARTn_XON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON1[7:0]							
Type									R/W							
Reset									0							

UARTn+0014h XON2 UARTn_XON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON2[7:0]							
Type									R/W							
Reset									0							

UARTn+0018h XOFF1 UARTn_XOFF1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF1[7:0]							
Type									R/W							
Reset									0							

UARTn+001Ch XOFF2 UARTn_XOFF2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF2[7:0]							
Type									R/W							
Reset									0							

*Note: XON1, XON2, XOFF1, XOFF2 are valid only when LCR=BFh.

UARTn+0020h AUTOBAUD_EN UARTn_AUTOBAUD_EN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																AUTO_EN
Type																R/W
Reset																0

AUTOBAUD_EN Auto-baud enable signal

0 Auto-baud function disable

1 Auto-baud function enable

UARTn+0024h HIGH SPEED UART UARTn_HIGHSPEED

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SPEED [1:0]	
Type															R/W	
Reset															0	

SPEED UART sample counter base

0 based on 16*baud_pulse, baud_rate = system clock frequency/16/{DLH, DLL}

based on 8*baud_pulse, baud_rate = system clock frequency/8/{DLH, DLL}

based on 4*baud_pulse, baud_rate = system clock frequency/4/{DLH, DLL}

based on sampe_count * baud_pulse, baud_rate = system clock frequency / sampe_count

The table below shows the divisor needed to generate a given baud rate from CLK inputs of 13M Hz based on different HIGHSPEED value.

BAUD	HIGHSPEED = 0	HIGHSPEED = 1	HIGHSPEED = 2
110	7386	14773	29545
300	2708	7386	14773
1200	677	2708	7386
2400	338	677	2708
4800	169	338	677
9600	85	169	338
19200	42	85	169
38400	21	42	85
57600	14	21	42
115200	7	14	21
230400	*	7	14
460800	*	*	7
921600	*	*	*

Table 22 Divisor needed to generate a given baud rate from 13MHz based on different HIGHSPEED value

The table below shows the divisor needed to generate a given baud rate from CLK inputs of 26 MHz based on different HIGHSPEED value.

BAUD	HIGHSPEED = 0	HIGHSPEED = 1	HIGHSPEED = 2
110	14773	29545	59091
300	5417	14773	29545
1200	1354	5417	14773

2400	677	1354	5417
4800	339	677	1354
9600	169	339	667
19200	85	169	339
38400	42	85	169
57600	28	42	85
115200	14	28	42
230400	7	14	28
460800	*	7	14
921600	*	*	7

Table 23 Divisor needed to generate a given baud rate from 26 MHz based on different HIGHSPEED value

The table below shows the divisor needed to generate a given baud rate from CLK inputs of 52MHz based on different HIGHSPEED value.

BAUD	HIGHSPEED = 0	HIGHSPEED = 1	HIGHSPEED = 2
110	29545	59091	118182
300	10833	29545	59091
1200	2708	10833	29545
2400	1354	2708	10833
4800	677	1354	2708
9600	339	677	1354
19200	169	339	677
38400	85	169	339
57600	56	85	169
115200	28	56	85
230400	14	28	56
460800	7	14	28
921600	*	7	14

Table 24 Divisor needed to generate a given baud rate from 52 MHz based on different HIGHSPEED value

UARTn+0028h SAMPLE_COUNT UARTn_SAMPLE_COUNT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SAMPLECOUNT [7:0]							
Type									R/W							
Reset									0							

When HIGHSPEED=3, the sample_count is the threshold value for UART sample counter (sample_num).

Count from 0 to sample_count.

For example, this register shall be set to 13 when you want to diveded by 14.

UARTn+002Ch SAMPLE_POINT UARTn_SAMPLE_POINT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SAMPLEPOINT [7:0]							
Type									R/W							
Reset									Ffh							

When HIGHSPEED=3, UART gets the input data when sample_count=sample_num.

e.g. system clock = 13MHz, 921600 = 13000000 / 14

sample_count = 14 and sample point = 7 (sample the central point to decrease the inaccuracy)

The SAMPLE_POINT is usually (SAMPLE_COUNT/2).

UARTn+0030h AUTOBAUD_REG UARTn_AUTOBAUD_REG

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BAUD_STAT[3:0]				BAUDRATE[3:0]			
Type									RO				RO			
Reset									0				0			

BAUD_RATE Autobaud baud rate

0 115200

57600

38400

19200

9600

4800

2400

1200

300

110

BAUDSTAT Autobaud format

0 Autobaud is detecting

AT_7N1

AT_7O1

AT_7E1

AT_8N1

AT_8O1

AT_8E1

at_7N1

at_7E1

at_7O1

at_8N1

at_8E1

at_8O1

Autobaud detection fails

UARTn+0034h Rate Fix Address UARTn_RATEFIX_AD

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RESTRICT	FREQ_SEL	AUTOBAUD_RATE_FIX	RXTE_FIX
Type													R/W	R/W	R/W	R/W
Reset													0	0	0	0

RATE_FIX When you set "rate_fix"(34H[0]), you can transmit and receive data only if 1) the f13m_en is enable and the freq_sel (34H[2]) is set to 1, or

2) the f26m_en is enable and the freq_sel (34H[2]) is set to 0.

AUTOBAUD_RATE_FIX When you set "autobaud_rate_fix"(34H[1]), you can tx/rx the autobaud packet only if

1) the f13m_en is enable and the freq_sel (34H[2]) is set to 1, or

2) the f26m_en is enable and the freq_sel (34H[2]) is set to 0.

FREQ_SEL

0 Select f26m_en for rate_fix and autobaud_rate_fix

1 Select f13m_en for rate_fix and autobaud_rate_fix

RESTRICT The "restrict" (34H[3]) is used to set a more condition for the autobaud fsm starting point

UARTn+0038h AUTOBAUDSAMPLE UARTn_AUTOBAUDSAMPLE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										AUTOBAUDSAMPLE						

Type										R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset										dh						

Since the system clock may change, autobaud sample duration should change as system clock changes.

When system clock = 13MHz, autobaudsample = 6; when system clock = 26MHz, autobaudsample = 13.

UARTn+003Ch Guard time added register UARTn_GUARD

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												GUARD_EN	GUARD_CNT[3:0]			
Type												R/W	R/W	R/W	R/W	R/W
Reset												0	0	0	0	0

GUARD_CNT Guard interval count value. Guard interval = (1/(system clock / **div_step** / div)) * GUARD_CNT.

GUARD_EN Guard interval add enable signal.

0 No guard interval added.

1 Add guard interval after stop bit.

UARTn+0040h Escape character register UARTn_ESCAPE_DAT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ESCAPE_DAT[7:0]							
Type									R/W							
Reset									FFh							

ESCAPE_DAT Escape character added before software flow control data and escape character, i.e. if tx data is xon (31h), with esc_en =1, uart transmits data as esc + CEh (~xon).

UARTn+0044h Escape enable register UARTn_ESCAPE_EN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ESC_EN
Type																R/W
Reset																0

ESC_EN Add escape character in transmitter and remove escape character in receiver by UART.

0 Do not deal with the escape character.

1 Add escape character in transmitter and remove escape character in receiver.

UARTn+0048h Sleep enable register UARTn_SLEEP_EN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SELLP_EN
Type																R/W
Reset																0

SLEEP_EN For sleep mode issue

0 Do not deal with sleep mode indicate signal

1 To activate hardware flow control or software control according to software initial setting when chip enters sleep mode. Releasing hardware flow when chip wakes up; but for software control, uart sends xon when awaken and when FIFO does not reach threshold level.

UARTn+004Ch Virtual FIFO enable register UARTn_VFIFO_EN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																VFIFO_EN
Type																R/W
Reset																0

VFIFO_EN Virtual FIFO mechanism enable signal.

0 Disable VFIFO mode.

1 Enable VFIFO mode. When virtual mode is enabled, the flow control is based on the DMA threshold, and generates a timeout interrupt for DMA.

UARTn+0050h Rx Trigger Address UARTn_RXTRI_AD

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RXTRIG[3:0]			
Type													R/W			
Reset													0			

RXTRIG When {rtm,rtl}=2'b11, The Rx FIFO threshold will be Rxtrig.

3.13 Auxiliary ADC Unit

The auxiliary ADC unit is used to monitor the status of the battery and charger, to identify the plugged peripheral, and to perform temperature measurement. Seven input channels allow diverse applications in this unit.

Each channel can operate in one of two modes: immediate mode and timer-triggered mode. The mode of each channel can be individually selected through register AUXADC_CON0. For example, if the flag SYN0 in the register

AUXADC_CON0 is set, the channel 0 is set in timer-triggered mode. Otherwise, the channel operates in immediate mode.

In immediate mode, the A/D converter samples the value once only when the flag in the AUXADC_CON1 register has been set. For example, if the flag IMM0 in AUXADC_CON1 is set, the A/D converter samples the data for channel 0. The IMM flags must be cleared and set again to initialize another sampling.

The value sampled for channel 0 is stored in register AUXADC_DAT0, the value for channel 1 is stored in register AUXADC_DAT1, etc.

If the AUTOSET flag in the register AUXADC_CON3 is set, the auto-sample function is enabled. The A/D converter samples the data for the channel in which the corresponding data register has been read. For example, in the case where the SYN1 flag is not set, the AUTOSET flag is set, when the data register AUXADC_DAT0 has been read, the A/D converter samples the next value for channel 1 immediately.

If multiple channels are selected at the same time, the task is performed sequentially on every selected channel. For example, if AUXADC_CON1 is set to 0x7f, that is, all 7 channels are selected, the state machine in the unit starts sampling from channel 6 to channel 0, and saves the values of each input channel in the respective registers. The same process also applies in timer-triggered mode.

In timer-triggered mode, the A/D converter samples the value for the channels in which the corresponding SYN flags are set when the TDMA timer counts to the value specified in the register TDMA_AUXEV1, which is placed in the TDMA timer. For example, if AUXADC_CON0 is set to 0x7f, all 7 channels are selected to be in timer-triggered mode. The state machine samples all 7 channels sequentially and save the values in registers from AUXADC_DAT0 to AUXADC_DAT6, as it does in immediate mode.

There is a dedicated timer-triggered scheme for channel 0. This scheme is enabled by setting the SYN7 flag in the register AUXADC_CON2. The timing offset for this event is stored in the register TDMA_AUXEV0 in the TDMA timer. The sampled data triggered by this specific event is stored in the register AUXADC_DAT7. It is used to separate the results of two individual software routines that perform actions on the auxiliary ADC unit.

The AUTOCLR*n* in the register AUXADC_CON3 is set when it is intended to sample only once after setting timer-triggered mode. If AUTOCLR1 flag has been set, after the data for the channels in timer-triggered mode has been stored, the SYN*n* flags in the register AUXADC_CON0 are cleared. If AUTOCLR0 flag has been set, after the data for the channel 0 has been stored in the register AUXADC_DAT7, the SYN7 flag in the register AUXADC_CON2 is cleared.

The usage of the immediate mode and timer-triggered mode are mutually exclusive in terms of individual channels.

The PUWAIT_EN bit in the registers AUXADC_CON3 is used to power up the analog port in advance. This ensures that the power has ramped up to the stable state before A/D converter starts the conversion. The analog part is automatically powered down after the conversion is completed.

In MT6223, there are only three external pins (channel 0~2) for voltage detection. The other channels (3~6) are for charger, battery voltage, battery current and internal voltage detection.

3.13.1 Register Definitions

AUXADC+0000h Auxiliary ADC control register 0 AUXADC_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SYN6	SYN5	SYN4	SYN3	SYN2	SYN1	SYN0
Type										R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset										0	0	0	0	0	0	0

SYN*n* These 7 bits define whether the corresponding channel is sampled or not in timer-triggered mode. It is associated with timing offset register TDMA_AUXEV1. It supports multiple flags. The flags can be automatically cleared after those channel have been sampled if AUTOCLR1 in the register AUXADC_CON3 is set. To monitor ISENSE and BATSNS, the register INT_NODE_MUX[2] must be set to 1 in advanced.

0 The channel is not selected.

1 The channel is selected.

AUXADC+0004h Auxiliary ADC control register 1 AUXADC_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										IMM6	IMM5	IMM4	IMM3	IMM2	IMM1	IMM0
Type										R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset										0	0	0	0	0	0	0

IMM*n* These 7 bits are set individually to sample the data for the corresponding channel. It supports multiple flags.

0 The channel is not selected.

1 The channel is selected.

AUXADC+0008h Auxiliary ADC control register 2 AUXADC_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SYN7
Type																R/W
Reset																0

SYN7 This bit is used only for channel 0 and is to be associated with timing offset register TDMA_AUXEV0 in the TDMA timer in timer-triggered mode. The flag can be automatically cleared after channel 0 has been sampled if AUTOCLR0 in the register AUXADC_CON3 is set.

0 The channel is not selected.

1 The channel is selected.

AUXADC+000Ch Auxiliary ADC control register 3 AUXADC_CON3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOSET				PUWAIT_EN		AUTOCLR1	AUTOCLR0								STA
Type	R/W				R/W		R/W	R/W								RO
Reset	0				0		0	0								0

AUTOSET This field defines the auto-sample mode of the module. In auto-sample mode, each channel with its sample register being read can start sampling immediately without configuring the control register AUXADC_CON1 again.

PUWAIT_EN Thus field enables the power warm-up period to ensure power stability before the SAR process takes place. It is recommended to activate this field.

0 The mode is not enabled.

1 The mode is enabled.

AUTOCLR1 The field defines the auto-clear mode of the module for event 1. In auto-clear mode, each timer-triggered channel gets samples of the specified channels once the SYN*n* bit in the register AUXADC_CON0 has been set. The SYN*n* bits are automatically cleared and the channel is not enabled again by the timer event except when the SYN*n* flags are set again.

0 The automatic clear mode is not enabled.

1 The automatic clear mode is enabled.

AUTOCLR0 The field defines the auto-clear mode of the module for event 0. In auto-clear mode, the timer-triggered channel 0 gets the sample once the SYN7 bit in the register AUXADC_CON2 has been set. The SYN7 bit is automatically cleared and the channel is not enabled again by the timer event 0 except when the SYN7 flag is set again.

0 The automatic clear mode is not enabled.

1 The automatic clear mode is enabled.

STA The field defines the state of the module.

0 This module is idle.

1 This module is busy.

AUXADC+0010h Auxiliary ADC channel 0 register AUXADC_DAT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							DAT									
Type							RO									
Reset							0									

The register stores the sampled data for the channel 0. There are 8 registers of the same type for the corresponding channel . The overall register definition is listed in **Table 25**.

Register Address	Register Function	Acronym
AUXADC+0010h	Auxiliary ADC channel 0 data register	AUXADC_DAT0
AUXADC+0014h	Auxiliary ADC channel 1 data register	AUXADC_DAT1
AUXADC+0018h	Auxiliary ADC channel 2 data register	AUXADC_DAT2
AUXADC+001Ch	Auxiliary ADC channel 3 data register	AUXADC_DAT3
AUXADC+0020h	Auxiliary ADC channel 4 data register	AUXADC_DAT4
AUXADC+0024h	Auxiliary ADC channel 5 data register	AUXADC_DAT5
AUXADC+0028h	Auxiliary ADC channel 6 data register	AUXADC_DAT6
AUXADC+002Ch	Auxiliary ADC channel 0 data register for TDMA event 0	AUXADC_DAT7

Table 25 Auxiliary ADC data register list

3.14 General Purpose Inputs/Outputs

MT6223 offers 52 general-purpose I/O pins. By setting the control registers, MCU software can control the direction, the output value, and read the input values on these pins. These GPIOs and GPOs are multiplexed with other functionalities to reduce the pin count. To further reduce pin count, the GPIO setting is split into two scenarios, auxiliary function mode and debug mode. Depending on the GPIO_BANK(0x01C0) bit, overall GPIO setting can alternate between two modes (default is aux. Functional mode). However, leave some GPIO to be in auxiliary function mode while others are in debug mode is prohibited. In addition, all GPO pins are removed. To facilitate application use, software can configure which clock to send outside the chip. There are 6 clock-out ports embedded in 52 GPIO pins, and each clock-out can be programmed to output appropriate clock source.

For MT6223C, BPI_BUS2 and BPI_BUS3 can be used to provide MSDC clock output to memory card interface, these two I/O pin MUX is selected by ACIF_CON0[14] and ACIF_CON0[15], respectively.

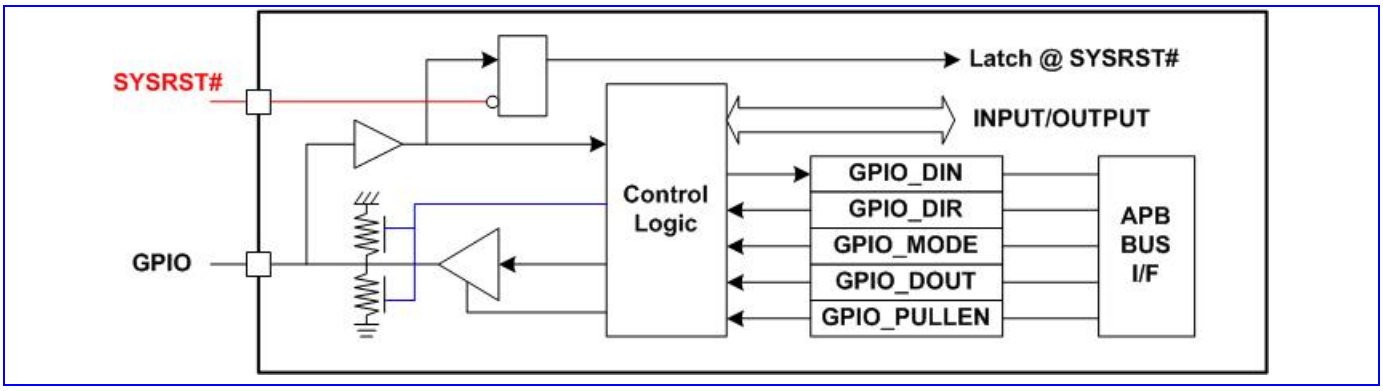


Figure 30 GPIO Block Diagram

GPIOs at RESET

Upon hardware reset (SYSRST#), GPIOs are all configured as inputs and the following alternative usages of GPIO pins are enabled:

These GPIOs are used to latch the inputs upon reset to memorize the desired configuration to make sure that the system restarts or boots in the right mode.

Multiplexing of Signals on GPIO

The GPIO pins can be multiplexed with other signals.

- DAICLK, DAIPCMIN, DAIPCMOUT, DAIRST: digital audio interface for FTA
- BPI_BUS6, BPI_BUS7, BPI_BUS8, BPI_BUS9: radio hard-wire control
- BSI_CS1: additional chip select signal for radio 3-wire interface
- LSCK, LSA0, LSDA, LSCE0#, LSCE1#: serial display interface
- LPCE1#: parallel display interface chip select signal
- PWM: pulse width modulation signal
- ALERTER: pulse width modulation signal for buzzer
- URXD1, UTXD1, URTS1, UCTS1: data and flow control signals for UART1
- URXD2, UTXD2, URTS2, UCTS2: data and flow control signals for UART2

- URXD3, UTXD3: data signals for UART3
- SRCLKENAI: external power on signal of the external VCXO LDO
- EA25, EA0: external memory interface address bit 25 and bit 0
- 32KHz, 6.5MHz, 13MHz, 26MHz clocks

3.14.1 Register Definitions

GPIO+0000h GPIO direction control register 1 GPIO_DIR1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GPIO +0010h GPIO direction control register 2 GPIO_DIR2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	PGIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIO+0020h GPIO direction control register 3 GPIO_DIR3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIO+0030h GPIO direction control register 4 GPIO_DIR4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												GPIO52	GPIO51	GPIO50	GPIO49	GPIO48
Type												R	R/W	R/W	R/W	R/W
Reset												0	0	0	0	0

GPIO*n* GPIO direction control

0 GPIOs are configured as input

1 GPIOs are configured as output

GPIO +0040h GPIO pull-up/pull-down enable register 1 GPIO_PULLEN1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GPIO +0050h GPIO pull-up/pull-down enable register 2 GPIO_PULLEN2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	PGIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1

GPIO+0060h GPIO pull-up/pull-down enable register 3 GPIO_PULLEN3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GPIO+0070h GPIO pull-up/pull-down enable register 4 GPIO_PULLEN4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												GPIO52	GPIO51	GPIO50	GPIO49	GPIO48
Type												R/W	R/W	R/W	R/W	R/W
Reset												1	1	1	1	1

GPIO*n* GPIO pull up/down enable

0 GPIOs pull up/down is not enabled

1 GPIOs pull up/down is enabled

GPIO +0080h GPIO data inversion control register 1 GPIO_DINV1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INV15	INV14	INV13	INV12	INV11	INV10	INV9	INV8	INV7	INV6	INV5	INV4	INV3	INV2	INV1	INV0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIO +0090h GPIO data inversion control register 2 GPIO_DINV2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INV31	INV30	INV29	INV28	INV27	INV26	INV25	INV24	INV23	INV22	INV21	INV20	INV19	IVN18	INV17	INV16

Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIO +00A0h GPIO data inversion control register 3 GPIO_DINV3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INV47	INV46	INV45	INV44	INV43	INV42	INV41	INV40	INV39	INV38	INV37	INV36	INV35	INV34	INV33	INV32
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIO+00B0h GPIO data inversion control register 4 GPIO_DINV4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												INV52	INV51	INV50	INV49	INV48
Type												R/W	R/W	R/W	R/W	R/W
Reset												0	0	0	0	0

INVn GPIO inversion control

0 GPIOs data inversion disable

1 GPIOs data inversion enable

GPIO +00C0h GPIO data output register 1 GPIO_DOUT1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIO +00D0h GPIO data output register 2 GPIO_DOUT2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	PGIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIO +00E0h GPIO data output register 3 GPIO_DOUT3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32

Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIO+00F0h GPIO data output register 4 GPIO_DOUT4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												~~GPIO52~~	GPIO51	GPIO50	GPIO49	GPIO48
Type												~~R/W~~	R/W	R/W	R/W	R/W
Reset												~~0~~	0	0	0	0

GPIOn GPIO data output control

0 GPIOs data output 1

1 GPIOs data output 0

GPIO +0100h GPIO data Input register 1 GPIO_DIN1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

GPIO +0110h GPIO data Input register 2 GPIO_DIN2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	PGIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

GPIO +0120h GPIO data Input register 3 GPIO_DIN3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

GPIO+0130h GPIO data input register 4 GPIO_DIN4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												GPIO52	GPIO51	GPIO50	GPIO49	GPIO48
Type												RO	RO	RO	RO	RO

Reset												X	X	X	X	X

GPIOn GPIOs data input

GPIO+01C0h GPIO bank GPIO_BANK

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BANK
Type																R/W
Reset																1

FIELD Configure the GPIO sets to auxiliary function mode or to debug mode

- 0 debug mode
- 1 auxiliary function mode

GPIO+0200h CLK_OUT0 setting CLKO_MODE1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CLKOUT			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

CLKOUT select the clock output source

- 1 f26m_ck
- 2 f13m_ck
- 3 f65m_ck, 6.5MHz
- 4 f32k_ck
- 5 dsp1_ck
- 6 dsp2_ck
- 7 mcu_ck
- 8 ahb_ck
- 9 slow_ck
- A fmcu_ck, PLL output divided by two, 52MHz
- B fdsp_ck, PLL output, 104MHz

GPIO+0210h CLK_OUT1 setting CLKO_MODE2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CLKOUT			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

GPIO+0220h CLK_OUT2 setting CLKO_MODE3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CLKOUT			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

GPIO+0230h CLK_OUT3 setting CLKO_MODE4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CLKOUT			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

GPIO+0240h CLK_OUT4 setting CLKO_MODE5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CLKOUT			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

GPIO+0250h CLK_OUT5 setting CLKO_MODE6

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CLKOUT			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

GPIO +0150h GPIO mode control register 1 GPIO_MODE1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO7_M		GPIO6_M		GPIO5_M		GPIO4_M		GPIO3_M		GPIO2_M		GPIO1_M		GPIO0_M	
Type	R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
Reset	01		01		01		01		01		01		01		01	

GPIO0_M GPIO mode selection

- 00 Configured as GPIO function
- 01 parallel LCD data bit 8
- 10 Reserved
- 11 Backup-SIMDATA for both modes

GPIO1_M GPIO mode selection

- 00 Configured as GPIO function
- 01 parallel LCD data bit 7
- 10 Reserved
- 11 Backup-SIMVCC if GPIO_BANK is 1

GPIO2_M GPIO mode selection

- 00 Configured as GPIO function
- 01 parallel LCD data bit 6
- 10 Reserved
- 11 Backup-SIMSEL if GPIO_BANK is 1

GPIO3_M GPIO mode selection

- 00 Configured as GPIO function
- 01 parallel LCD data bit 5
- 10 Reserved
- 11 Backup-SIMCLK if GPIO_BANK is 1

GPIO4_M GPIO mode selection

- 00 Configured as GPIO function
- 01 parallel LCD data bit 4
- 10 Reserved
- 11 Backup-SIMRST if GPIO_BANK is 1

GPIO5_M GPIO mode selection

- 00 Configured as GPIO function

01 parallel LCD data bit 3

10 Reserved

11 Reserved

GPIO6_M GPIO mode selection

00 Configured as GPIO function

01 parallel LCD data bit 2

10 Reserved

11 Reserved

GPIO7_M GPIO mode selection

00 Configured as GPIO function

01 parallel LCD data bit 1

10 Reserved

11 Reserved

GPIO +0160h GPIO mode control register 2 GPIO_MODE2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15_M		GPIO14_M		GPIO13_M		GPIO12_M		GPIO11_M		GPIO10_M		GPIO9_M		GPIO8_M	
Type	R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
Reset	00		01		01		01		01		01		01		01	

GPIO8_M GPIO mode selection

00 Configured as GPIO function

01 LCD reset

10 Reserved

11 Reserved

GPIO9_M GPIO mode selection

00 Configured as GPIO function

01 parallel LCD write strobe

10 Reserved

11 Reserved

GPIO10_M GPIO mode selection

00 Configured as GPIO function

01 parallel LCD read strobe

~~10 LCD serial clock~~

11 Reserved

GPIO11_M GPIO mode selection

00 Configured as GPIO function

01 parallel LCD data bit 0

~~10 serial LCD data bit~~

11 Reserved

GPIO12_M GPIO mode selection

00 Configured as GPIO function

01 parallel LCD_A0

~~10 serial LCD_SA0~~

11 Reserved

GPIO13_M GPIO mode selection

00 Configured as GPIO function

01 parallel LCD chip-select 0

~~10 serial LCD chip-select 0~~

11 Reserved

GPIO14_M GPIO mode selection

00 Configured as GPIO function

01 parallel LCD chip-select 1

~~10 serial LCD chip-select 1~~

11 Internal interrupt 30

GPIO15_M GPIO mode selection

00 Configured as GPIO function

01 DAI clock output

10 EDI clock if GPIO_BANK is 1, SWDBG clock if GPIO_BANK is 0

11 Reserved if GPIO_BANK is 1, slave DSP task ID 2 if GPIO_BANK is 0

GPIO +0170h GPIO mode control register 3 GPIO_MODE3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO23_M		GPIO22_M		GPIO21_M		GPIO20_M		GPIO19_M		GPIO18_M		GPIO17_M		GPIO16_M	
Type	R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
Reset	0		00		00		10		00		00		00		00	

GPIO16_M GPIO mode selection

00 Configured as GPIO function

01 DAI PCM output

10 EDI data if GPIO_BANK is 1, SWDBG ADDR[1] if GPIO_BANK is 0

11 Reserved if GPIO_BANK is 1, slave DSP task ID 3 if GPIO_BANK is 0

GPIO17_M GPIO mode selection

00 Configured as GPIO function

01 DAI PCM input

10 Reserved if GPIO_BANK is 1, SWDBG ADDR[0] if GPIO_BANK is 0

11 Reserved if GPIO_BANK is 1, slave DSP task ID 4 if GPIO_BANK is 0

GPIO18_M GPIO mode selection

00 Configured as GPIO function

01 DAI reset

10 Reserved if GPIO_BANK is 1, SWDBG write strobe if GPIO_BANK is 0

11 Reserved if GPIO_BANK is 1, slave DSP task ID 5 if GPIO_BANK is 0

GPIO19_M GPIO mode selection

00 Configured as GPIO function

01 DAI sync.

10 EDI word-select if GPIO_BANK is 1, SWDBG packet-end if GPIO_BANK is 0

11 Reserved if GPIO_BANK is 1, slave DSP task ID 6 if GPIO_BANK is 0

GPIO20_M GPIO mode selection

00 Configured as GPIO function

01 BPI bus bit 6

10 xadmux. Only used when being boot-up. After system reset, xadmux is of no use, and software can configure the GPIO20_M to any other function

11 Reserved

GPIO21_M GPIO mode selection

00 Configured as GPIO function

01 BPI bus bit 7

10 BSI read-back, BSI_RFIN

11 clock-out 0

GPIO22_M GPIO mode selection

00 Configured as GPIO function

01 BPI bus bit 8

10 Key-pad column 5

11 clock-out 1 if GPIO_BANK is 1, master DSP task ID 1 if GPIO_BANK is 0

GPIO23_M GPIO mode selection

00 Configured as GPIO function

01 BPI bus bit 9

10 BSI chip-select 1

11 clock-out 2

GPIO +0180h GPIO mode control register 4 GPIO_MODE4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO31_M		GPIO30_M		~~GPIO29_M~~		GPIO28_M		GPIO27_M		GPIO26_M		GPIO25_M		GPIO24_M	
Type	R/W		R/W		~~R/W~~		R/W		R/W		R/W		R/W		R/W	
Reset	01		01		~~00~~		01		01		01		00		00	

GPIO24_M GPIO mode selection

00 Configured as GPIO function

01 alerter

10 Reserved if GPIO_BANK is 1, SWDBG data bit 0 if GPIO_BANK is 0

11 Reserved if GPIO_BANK is 1, slave DSP SICE clock if GPIO_BANK is 0

GPIO25_M GPIO mode selection

00 Configured as GPIO function

01 PWM

10 Reserved if GPIO_BANK is 1, SWDBG data bit 1 if GPIO_BANK is 0

11 Reserved if GPIO_BANK is 1, slave DSP SICE mode-select if GPIO_BANK is 0

GPIO26_M GPIO mode selection

00 Configured as GPIO function

01 JTRST_B

10 External interrupt 4

11 Reserved

GPIO27_M GPIO mode selection

00 Configured as GPIO function

01 JTDI

10 External interrupt 5

11 Reserved

GPIO28_M GPIO mode selection

00 Configured as GPIO function

01 JTMS

10 External interrupt 6

11 Reserved

~~GPIO29_M GPIO mode selection~~

~~00 Configured as GPIO function~~

~~01 WATCHDOG~~

~~10 Reserved~~

~~11 Reserved~~

GPIO30_M GPIO mode selection

00 Configured as GPIO function

01 EA0

10 EA25

11 Reserved

GPIO31_M GPIO mode selection

00 Configured as GPIO function

01 SRCLKENAI

10 Power Key (for backup)

11 Reserved if GPIO_BANK is 1, master DSP task ID0 if GPIO_BANK is 0

GPIO +0190h GPIO mode control register 5 GPIO_MODE5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO39_M		GPIO38_M		GPIO37_M		GPIO36_M		GPIO35_M		GPIO34_M		GPIO33_M		GPIO32_M	
Type	R/W		R/W		R/W		R/W		R/W		R/W		R/W		R/W	
Reset	01		01		01		01		01		01		01		01	

GPIO32_M GPIO mode selection

00 Configured as GPIO function

01 Key-pad column 4

10 Reserved if GPIO_BANK is 1, SWDBG data bit 2 if GPIO_BANK is 0

11 Reserved

GPIO33_M GPIO mode selection

00 Configured as GPIO function

01 Key-pad column 3

10 Reserved if GPIO_BANK is 1, SWDBG data bit 3 if GPIO_BANK is 0

11 Reserved

GPIO34_M GPIO mode selection

00 Configured as GPIO function

01 Key-pad column 2

10 Reserved if GPIO_BANK is 1, SWDBG data bit 4 if GPIO_BANK is 0

11 Reserved

GPIO35_M GPIO mode selection

00 Configured as GPIO function

01 Key-pad column 1

10 Reserved if GPIO_BANK is 1, SWDBG data bit 5 if GPIO_BANK is 0

11 Reserved

GPIO36_M GPIO mode selection

00 Configured as GPIO function

01 Key-pad column 0

10 Reserved if GPIO_BANK is 1, SWDBG data bit 6 if GPIO_BANK is 0

11 Reserved

GPIO37_M GPIO mode selection

00 Configured as GPIO function

01 Key-pad row 4

10 Reserved if GPIO_BANK is 1, SWDBG data bit 7 if GPIO_BANK is 0

11 Reserved

GPIO38_M GPIO mode selection

00 Configured as GPIO function

01 Key-pad row 3

10 Reserved if GPIO_BANK is 1, SWDBG read-strobe if GPIO_BANK is 0

11 Reserved

GPIO39_M GPIO mode selection

00 Configured as GPIO function

01 Key-pad row 2

10 Reserved if GPIO_BANK is 1, SWDBG read-output-enable if GPIO_BANK is 0

11 Reserved

GPIO +01A0h GPIO mode control register 6 GPIO_MODE6

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47_M		GPIO46_M		GPIO45_M		GPIO44_M		GPIO43_M		GPIO42_M		GPIO41_M		GPIO40_M	

Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	00	00	00	01	00	00	01	01

GPIO40_M GPIO mode selection

00 Configured as GPIO function

01 Key-pad row 1

10 Reserved if GPIO_BANK is 1, SWDBG Full-flag if GPIO_BANK is 0

11 Reserved

GPIO41_M GPIO mode selection

00 Configured as GPIO function

01 Key-pad row 0

10 Reserved if GPIO_BANK is 1, SWDBG Empty-flag if GPIO_BANK is 0

11 Reserved

GPIO42_M GPIO mode selection

00 Configured as GPIO function

01 External interrupt 2

10 MIRQ

11 Reserved if GPIO_BANK is 1, tdma_sdat[0] if GPIO_BANK is 0

GPIO43_M GPIO mode selection

00 Configured as GPIO function

01 External interrupt 3

10 Reserved

11 Reserved if GPIO_BANK is 1, tdma_sdat[1] if GPIO_BANK is 0

GPIO44_M GPIO mode selection, the mode setting LSB is inverted in read-back, the following setting table means what value software should write when in coding. Note that the function of SET and CLR is reversed for this GPIO

01 Configured as GPIO function

00 UART1 TXD signal

11 Reserved if GPIO_BANK is 1, tdma_evtval if GPIO_BANK is 0

10 Reserved if GPIO_BANK is 1, AHB clock if GPIO_BANK is 0

GPIO45_M GPIO mode selection

00 Configured as GPIO function if GPIO_BANK is 1, tdma_fs if GPIO_BANK is 0

01 UART1 flow control CTS_B

10 Reserved if GPIO_BANK is 1, CTIRQ2 if GPIO_BANK is 0

11 SCL if GPIO_BANK is 1, slave DSP ID0 if GPIO_BANK is 0

GPIO46_M GPIO mode selection

00 Configured as GPIO function if GPIO_BANK is 1, TDMA_BTXEN if GPIO_BANK is 0

01 UART1 flow control RTS_B

10 Reserved if GPIO_BANK is 1, CTIRQ1 if GPIO_BANK is 0

11 SDA if GPIO_BANK is 1, slave DSP ID1 if GPIO_BANK is 0

GPIO47_M GPIO mode selection

00 Configured as GPIO function if GPIO_BANK is 1, TDMA_BTXFS if GPIO_BANK is 0

01 UART3 TXD signal

10 UART2 CTS_B signal if GPIO_BANK is 1, DTIRQ if GPIO_BANK is 0

11 clock-out 3 if GPIO_BANK is 1, slave DSP SICE data if GPIO_BANK is 0

GPIO +01B0h GPIO mode control register 7 GPIO_MODE7

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							GPIO52		GPIO51		GPIO50		GPIO49		GPIO48	
Type							R/W		R/W		R/W		R/W		R/W	
Reset							1		0		01		0		0	

GPIO48_M GPIO mode selection

00 Configured as GPIO function if GPIO_BANK is 1, TDMA_BRXEN if GPIO_BANK is 0

01 UART3 RXD Signal

10 UART2 RTS_B Signal if GPIO_BANK is 1, DSP2_CK if GPIO_BANK is 0

11 clock-out 4 if GPIO_BANK is 1, master DSP SICE mode-select if GPIO_BANK is 0

GPIO49_M GPIO mode selection

00 Configured as GPIO function if GPIO_BANK is 1, TDMA_BRXFS if GPIO_BANK is 0

01 UART2 RXD Signal

10 clock-out 5

11 Reserved if GPIO_BANK is 1, master DSP SICE clock if GPIO_BANK is 0

GPIO50_M GPIO mode selection, the mode setting LSB is inverted in read-back, the following setting table means what value software should write when in coding. Note that the function of SET and CLR is reversed for this GPIO

01 Configured as GPIO function

00 UART1 RXD Signal

10 Reserved if GPIO_BANK is 1, slow clock if GPIO_BANK is 0

11 Reserved

GPIO51_M GPIO mode selection

00 Configured as GPIO function

01 UART2 TXD Signal

10 Reserved if GPIO_BANK is 1, MCU clock if GPIO_BANK is 0

11 VIBRATOREN (software mimic PWM) if GPIO_BANK is 1, master DSP SICE data if GPIO_BANK is 0

GPIO52_M GPIO mode selection

00 Configured as GPI function, GPIO52 allows input mode only

01 MFIQ

10 ECS3_B

11 Reserved

GPIO +0300h OE read-back selection GPIO_TM

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TM_DIR
Type																R/W
Reset																0

TM_DIR Select to read GPIO_DIRx as the real pad output-enable or the MCU-configured GPIO_DIR

0 MCU-configured

1 Real pad OE

GPIO+xxx4h GPIO xxx register SET GPIO_XXX_SET

For all registers addresses listed above, writing to the +4h addresse offset will perform a bit-wise **OR** function between the 16bit written value and the 16bit register value already existing in the corresponding GPIO_xxx registers.

Eg.

If GPIO_DIR1 (GPIO+0000h) = 16'h0F0F,

writing GPIO_DIR1_SET (GPIO+0004h) = 16'F0F0 will result in GPIO_DIR1 = 16'hFFFF.

GPIO+xxx8h GPIO xxx register CLR GPIO_XXX_CLR

For all registers addresses listed above, writing to the +8h addresse offset will perform a bit-wise **AND-NOT** function between the 16bit written value and the 16bit register value already existing in the corresponding GPIO_xxx registers.

Eg.

If GPIO_DIR1 (GPIO+0000h) = 16'h0F0F,

writing GPIO_DIR1_CLR (GPIO+0008h) = 16'0F0F will result in GPIO_DIR1 = 16'h0000.

CONFG +0700h SIM interface Power-saving ACIF_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPI3_MSDC_MODE	BPI2_MSDC_MODE	WT_SD_DIS	LCD_PD_SEL	CIF_SMT_EN	MFIQ_SEL	MIRQ_SEL	WT_SDCNT								SIM_PWRSAVE_EN
Type	R/W	R/W	R/W	R/W	RW/	R/W	R/W	R/W								R/W
Reset	0	0	0	0	0	0	0	0								0

SIM_PWRSAVE_EN Pull high CORE_SIMDATA_OUT when VSIM is not enabled

0 Disable

1 Enable

LCD_PD_SEL Select the pull-down enable for LCD_D[8:0]

0 PD of LCD_D[8:0] is decided by LCD controller chip-selects

1 PD of LCD_D[8:0] is disable

WT_SD_DIS Slow-down disable for wavetable. The slow-down is to suppress the AHB request capability of wavetable

0 Slow-down enable

1 Slow-down disable

WT_SDCNT Slow-down counter for wavetable. The larger WT_SDCNT, the more AHB request is suppressed.

MIRQ_SEL Selection for source of ARM MIRQ

0 Source from GPIO42 (EINT2)

1 Source from internal signal “GPIO42 AND GPIO14”

MFIQ_SEL Selection for source of ARM MFIQ

0 Source from GPIO52 (ECS3_B)

1 Source from internal signal “GPIO52 AND GPIO14”

BPI2_MSDC_MODE Select pin BPI_BUS2 between original BPI_BUS2 function and MSDC clock output, it is for MT6223C only

0 BPI_BUS2

1 memory card clock output

BPI3_MSDC_MODE Select pin BPI_BUS3 between original BPI_BUS3 function and MSDC clock output, it is for MT6223C only

0 BPI_BUS3

1 memory card clock output

CONFG +0704h LCD/CAM I/O driving strength control ACIF_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIF_PCLK_SEL	CIF_LCD_TRIG	CIF_DMA_DREQ_SEL	CIF_DMA_TRIG	CIF_PCLK_INV	PLCD_SR	PLCD_E2	PLCD_E4	PLCD_E8	CIF_INT30_INV			CLKO345_DRV	CLKO012_DRV	BPI3_E2	BP3I_E4
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0			0	0	0	0

PLCD _E8 The driving strength control of the parallel LCM control interface

PLCD _E4 The driving strength control of the parallel LCM control interface

PLCD _E2 The driving strength control of the parallel LCM control interface

PLCD_SR The slew rate control of the parallel LCM control interface

BPI3_E2 The driving strength control of the BPI3

BPI3_E4 The driving strength control of the BPI3

CLKO012_DRV The driving strength control of CLK_OUT0 ~ CLK_OUT3

0 2mA

1 14mA

CLKO345_DRV The driving strength control of CLK_OUT3 ~ CLK_OUT5

0 2mA

1 14mA

CIF_INT30_INV Select inversion of LCD_CS1_B (GPIO14 mode 2) as INT30 of CIRQ

0 Inversion disabled

1 Inversion enabled

CIF_PCLK_INV Select the polarity of PIXEL_CLOCK input (LCD_CS1_B or ECS3_B, depending on CIF_PCLK_SEL)

0 Non-inversions

1 Select the inverted pixel clock

CIF_DMA_TRIG Enable the hardware DMA DREQ for CIF

0 Disabled

1 Enabled

CIF_DMA_DREQ_SEL Select the source of DMA DREQ for CIF

0 DREQ comes from "ECS3_B(HSYNC) & LCD_CS1_B(PCLK)"

1 DREQ comes from "EINT2(HSYNC) & LCD_CS1_B(PCLK)" or from "EINT2(HSYNC) & ECS_B(PCLK), "depending on CIF_PCLK_SEL

CIF_LCD_TRIG Enable the hardware LCD DREQ for CIF

0 Disabled

1 Enabled

CIF_PCLK_SEL Select the source of PIXEL clock

0 ECS3_B(GPIO52)

1 LCD_CS1_B(GPIO14)

	PCLK	HSYNC	ACIF_CON[31, 29]	ACIF_CON[27]	ACIF_CON[22]	Interrupt source
GPIO set 1	ECS3_B(GPIO52 @ mode 1)	LCD_CS1_B(GPIO14 @ mode3)	0 0	Invert of PCLK	Invert of INT30	INT30
GPIO set 2	ECS3_B(GPIO52 @ mode 1)	EINT2(GPIO14 @ mode2)	0 1	Invert of PCLK	X	MIRQ
GPIO set 3	LCD_CS1_B(GPIO14 @ mode3)	EINT2(GPIO14 @ mode2)	1 1	Invert of PCLK	X	MIRQ
GPIO set 4	EINT2(GPIO14 @ mode2)	LCD_CS1_B(GPIO14 @ mode3)	1 1	X	Invert of INT30	INT30

3.15 General Purpose Timer

3.15.1 General Description

Three general-purpose timers are provided. The timers are 16 bits long and run independently of each other, although they share the same clock source. Two timers can operate in one of two modes: one-shot mode and auto-repeat mode; the other is a free running timer. In one-shot mode, when the timer counts down and reaches zero, it is halted. In auto-repeat mode, when the timer reaches zero, it simply resets to countdown initial value and repeats the countdown to zero; this loop repeats

until the disable signal is set to 1. Regardless of the timer's mode, if the countdown initial value (i.e. GPTIMER1_DAT for GPT1 or GPTIMER_DAT2 for GPT2) is written when the timer is running, the new initial value does not take effect until the next time the timer is restarted. In auto-repeat mode, the new countdown start value is used on the next countdown iteration. Therefore, before enabling the gptimer, the desired values for GPTIMER_DAT and the GPTIMER_PRESCALER registers must first be set.

3.15.2 Register Definitions

GPT +0000h GPT1 Control register GPTIMER1_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN	MODE														
Type	R/W	R/W														
Reset	0	0														

MODE This register controls GPT1 to count repeatedly (in a loop) or just one-shot.

0 One-shot mode is selected.

Auto-repeat mode is selected.

EN This register controls GPT1 to start counting or to stop.

0 GPT1 is disabled.

1 GPT1 is enabled.

GPT +0004h GPT1 Time-Out Interval register GPTIMER1_DAT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNT [15:0]															
Type	R/W															
Reset	FFFFh															

CNT [15:0] Initial counting value. GPT1 counts down from GPTIMER1_DAT. When GPT1 counts down to zero, a GPT1 interrupt is generated.

GPT +0008h GPT2 Control register GPTIMER2_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN	MODE														
Type	R/W	R/W														
Reset	0	0														

MODE This register controls GPT2 to count repeatedly (in a loop) or just one-shot.

0 One-shot mode is selected

1 Auto-repeat mode is selected

EN This register controls GPT2 to start counting or to stop.

0 GPT2 is disabled.

1 GPT2 is enabled.

GPT +000Ch GPT2 Time-Out Interval register GPTIMER2_DAT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNT [15:0]															
Type	R/W															
Reset	FFFFh															

CNT [15:0] Initial counting value. GPT2 counts down from GPTIMER2_DAT. When GPT2 counts down to zero, a GPT2 interrupt is generated.

GPT +0010h GPT Status register GPTIMER_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															GPT2	GPT1
Type															RC	RC
Reset															0	0

This register illustrates the gptimer timeout status. Each flag is set when the corresponding timer countdown completes, and can be cleared when the CPU reads the status register.

GPT +0014h GPT1 Prescaler register GPTIMER1_PRESCALER

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PRESCALER [2:0]		
Type														R/W		
Reset														100b		

PRESCALER This register controls the counting clock for gptimer1.

000 16 KHz

001 8 KHz

010 4 KHz

011 2 KHz

1 KHz

500 Hz

110 250 Hz

125 Hz

GPT +0018h GPT2 Prescaler register GPTIMER2_PRESCALER

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PRESCALER [2:0]		
Type														R/W		
Reset														100b		

PRESCALER This register controls the counting clock for gptimer2.

000 16 KHz

001 8 KHz

010 4 KHz

011 2 KHz

100 1 KHz

101 500 Hz

110 250 Hz

125 Hz

GPT+001Ch GPT3 Control register GPTIMER3_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																R/W
Reset																0

EN This register controls GPT3 to start counting or to stop.

0 GPT3 is disabled.

1 GPT3 is enabled.

GPT+0020h GPT3 Time-Out Interval register GPTIMER3_DAT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNT[15:0]															
Type	RO															
Reset	0															

CNT [15:0] If EN=1, GPT3 is a free running timer . Software reads this register for the countdown start value for GPT3.

GPT+0024h GPT3 Prescaler register GPTIMER3_PRESCALER

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PRESCALER [2:0]		
Type														R/W		
Reset														100b		

PRESCALER This register controls the counting clock for gptimer3.

000 16 KHz

001 8 KHz

010 4 KHz

011 2 KHz

100 1 KHz

101 500 Hz

110 250 Hz

111 125 Hz

3.16 GPRS Cipher Unit

3.16.1 General Description

The unit implements the GPRS encryption/decryption scheme that accelerates the computation of encryption and decryption GPRS pattern. The block accelerates the computation of the key stream. However the bit-wise encryption/decryption of the data is still done by the MCU.

Both GEA and GEA2 are supported.

Register Address	Register Function	Acronym
GCU+0000h	GPRS Encryption Algorithm Control Register	GCU_CON
GCU+0004h	GPRS Encryption Algorithm Status Register	GCU_SAT
GCU+0008h	GPRS Secret Key Kc 0 Register	GCU_SKEY0
GCU+000Ch	GPRS Secret Key Kc 1 Register	GCU_SKEY1
GCU+0010h	GPRS Message Key Register	GCU_MKEY
GCU+0014h	GPRS Ciphered Data Register	GCU_CDATA

Table 26 GCU Registers

3.16.2 Register Definitions

GCU+0000h GPRS Encryption Algorithm Control Register GCU_CON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RBO	KS		SINIT	DIR	ALG	
Type										R/W	R/W		WO	R/W	R/W	
Reset										0	10		0	0	0	

This register controls the key generation function of the GPRS Encryption Algorithm.

ALG Choose the encryption/decryption algorithm.

00 = GEA

01 = GEA2

10 = GEA3

11 = Reserved

DIR The DIRECTION input of the GPRS Encryption Algorithm.

SINIT Start initialization. The MCU writes 1 to start initialization. The bit is always read at 0.

KS Control the read access. 00 = byte access, 01 = half word (16 bits) access, 10 = word access, 11 reserved. Default value is 10.

RBO Reversal Byte Order bit. If the bit was set to 1, the byte order of GCU_SKEY0, GCU_SKEY1, GCU_MKEY in write operation and GCU_SKEY0, GCU_SKEY1, GCU_MKEY, GCU_CKEY in read operation would be the reverse of baseband processor, and if the bit was 0, the behavior would be the same as baseband processor. Byte-order of GCU_CON and GCU_SAT is not affected. The default value is 0 which is different from that in MT6218B.

GCU+0004h GPRS Encryption Algorithm Status Register GCU_SAT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STAT													KEY_COM	INIT	
Type	RO													RO	RO	

Reset	110											0	0	

This register shows the status of the GPRS Encryption unit.

INIT Initialization flag. 1 = the GCU is currently performing the initialization phase.

KEY_COM Key-stream computation. 1 = the GCU is computing new key stream, while 0 = a new key is available or the GCU is in initialization phase.

STAT The state of GCU core. For debug purpose.

GCU+0008h GPRS Secret Key Kc 0 Register GCU_SKEY0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	KC[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KC[15:0]															
Type	R/W															
Reset	0															

GCU+000Ch GPRS Secret Key Kc 1 Register GCU_SKEY1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	KC[63:48]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KC[47:32]															
Type	R/W															
Reset	0															

This set of registers shall be programmed with the GPRS Encryption Algorithm secret key.

GCU+0010h GPRS Message Key Register GCU_MKEY

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MKEY[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	MKEY[15:0]
Type	R/W
Reset	0

This register shall be programmed with the “message key” for the GPRS Encryption Algorithm.

GCU+0014h GPRS Ciphered DATA Register GCU_CDATA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDATA[31:16]															
Type	RO															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDATA[15:0]															
Type	RO															

The register contains the key stream. GCU will continue to generate next word of key while current word of key is removed.

3.16.3 Design

3.16.3.1 Block architecture

The architecture is depicted as **Figure 31**.

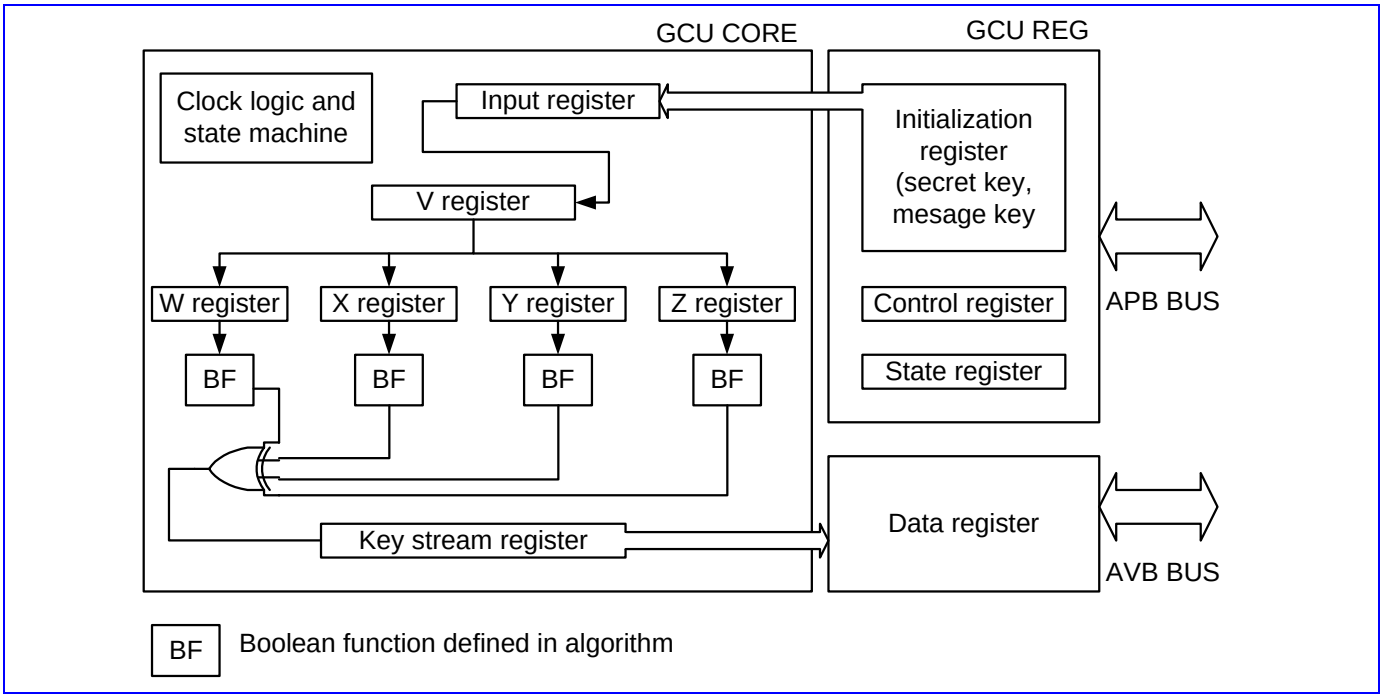


Figure 31 The block diagram of the GCU

In the core circuit, 7 shift registers are defined. The input register is a 97-bit register. It converts the parallel initialization data into serial concatenation of the secret key, the direction flag, and the message key. The key-stream register is a 32-bit register. It converts the serial key-stream into parallel output. The output bit-width could be byte, half-word, and word depending on

the value of KS. The V register is a 97-bit shift register. The W, X, Y, and Z registers are 29, 31, 32, and 33 bit shift registers, respectively.

3.16.3.2 Block state machine

A state machine is used to control the operation of registers. The state diagram is depicted as Figure 32.

Seven states are specified. RSET, INIT, STIR, INIT4, CHECKZ, KEYGEN, WAIT. The state transition is triggered by the clock logic. The operation in each state is briefly described as below.

In INIT state, V register is clocked with input from the input register. It takes 97 cycles for both GEA and GEA2.

In STIR state, V register is clocked without input for 128 cycles for GEA (194 cycles for GEA2).

In INIT4 state, V register is clocked without input and is shifted to provide the input to W (GEA2), X, Y, and Z registers. W (GEA2), X, Y, and Z registers are clocked with input. It takes 64 cycles for GEA (97 cycles for GEA2).

In CHECKZ state, Check all zeros condition of W (GEA2), X, Y, and Z registers. It takes 1 cycle. It is to keep all registers not in all zeros state.

In KEYGEN state, W (GEA2), X, Y and Z registers are clocked without input. The Boolean function result generates the key stream continuously. After one word is generated, it enters WAIT state. For KS equal to 00, it takes 8 cycles. For KS equal to 01, it takes 16 cycles. For KS equal to 10, it takes 32 cycles.

In WAIT state, the key stream generation is paused waiting the MCU to read the previous data. The MCU read access triggers next key stream generation and enter the KEYGEN state.

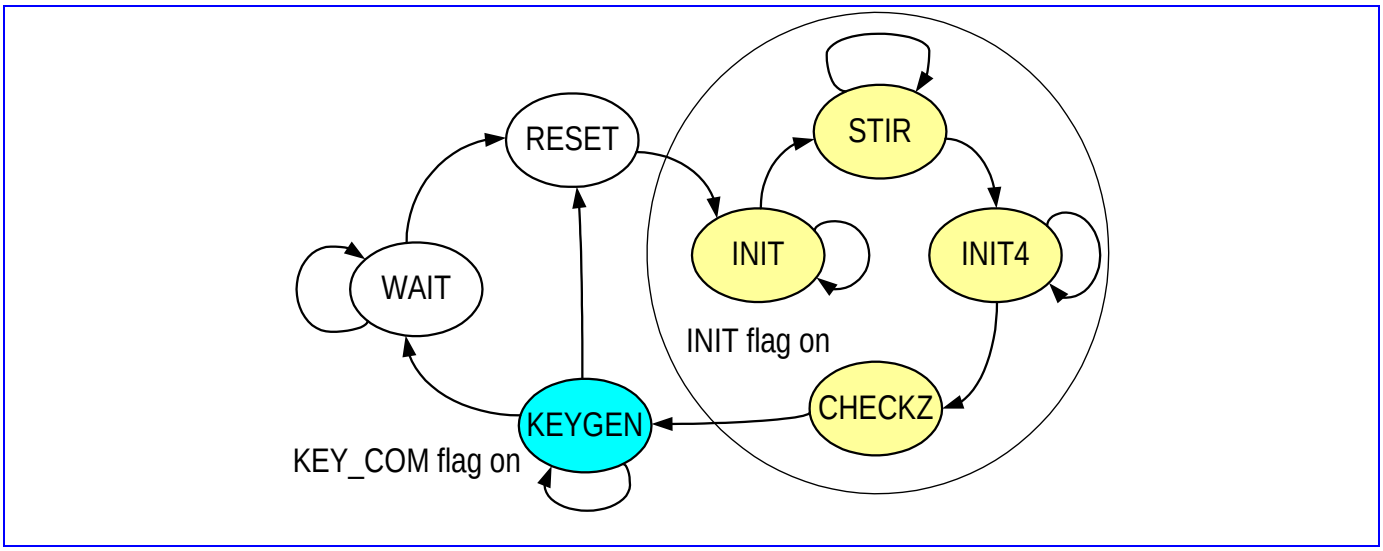


Figure 32 The state diagram of the GCU

Note:

The initialization phase including RSET, INIT, STIR, INIT4, CHECKZ, and the first KEYGEN states. Totally 320 cycles for GEA (421 cycles for GEA2) are necessary. In initialization phase, the INIT flag is asserted.

The MCU should poll the status of the GCU, and read the key-stream continuously until enough key-stream is retrieved. The GCU doesn't need to know how long the key-stream is. Every time the MCU reads the GCU_READ register, KEYGEN_START is asserted to trigger the key computation. In the phase of key computation, KEY_COM is asserted.

The MCU takes one cycle to read a word through the AVB bus. Due to the length of the LLC packet, the key-stream ranges from 3 to 1600 bytes. Ideally, for GEA2, it takes at least 389 + 1600 * 8 = 13189 cycles to generate 1600 bytes key-stream. It is about 253us in the case of 52MHz system clock.

The timing diagram is depicted as **Figure 33**.

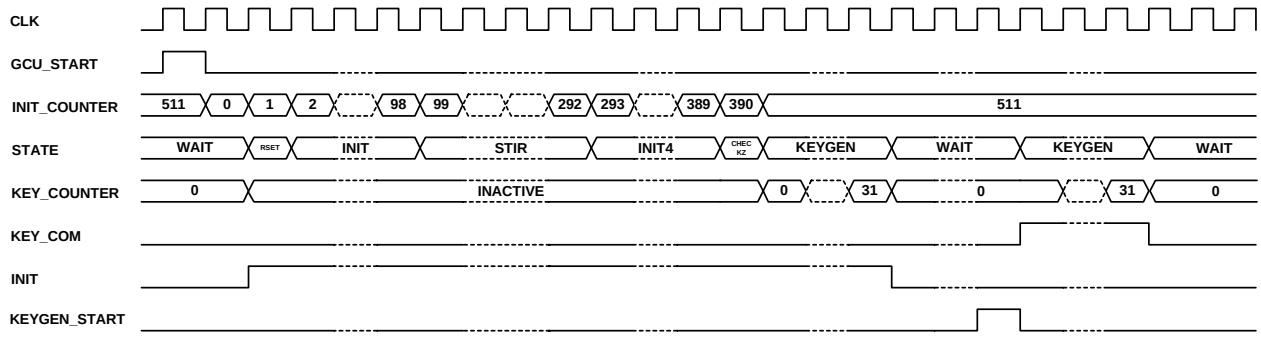


Figure 33 The timing diagram of the GCU (in case of GEA2)

3.17 Security Engine

3.17.1 General Description

SE realizes an efficient scheme to protect the program in non-volatile memory. Applying the flows in the IC with Chip-ID can: a) encrypted codes to protect the codes to be cracked (Confidentiality); b) guarantee the integrity; c) Copyright protection.

To protect the program in the novo memory, SE references 1: Chip UID; 2: custom seed; 3: Internal reproducible noise to enlarge the entropy space of ciphering. After proper configuration in BCON and BSEED, users can encrypt program plaintext into cipher-texts and store them onto NoVo memory. Due to the program are stored in ciphered mode, it's not easy to be disassembled. Further, the encryption process has referred to Chip UID, which may be different between two different chips, the cipher-text encrypted referred to Chip UIDA is very likely decrypted to wrong one referred to other IDs.

3.17.2 Register Definitions

Figure 34: SE Registers

Register Address	Register Function	Acronym
SE + 00c0h	SE Secure Booting control	SE_BCON
SE + 00c4h	SE Secure Booting source data	SE_BSRC
SE + 00c8h	SE Secure Booting seed data	SE_BSEED
SE + 00cch	SE Secure Booting encrypted data	SE_BENC
SE + 00d0h	SE Secure Booting decrypted data	SE_BDEC

SE+00c0h SE Secure Booting control SE_BCON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**PAR3**	**PAR2**	**PAR1**	**DIS**

Type													R/W	R/W	R/W	R/W
Reset													0	0	0	0

DIS Disable Secure Booting function. When DIS is asserted, the data read from SE_BENC and SE_BDEC is the same as SE_BSRC.

PAR1 Use inner information parameter 1 (SK) to strengthen security.

PAR2 Use inner information parameter 2 (RS) to strengthen security.

PAR3 Use inner information parameter 3 (MR) to strengthen security.

SE+00c4h SE Secure Booting source data SE_BSRC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BSRC[31:16]**															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BSRC[15:0]**															
Type	WO															
Reset	0															

BSRC Source data for Secure Booting to be encrypted (obtained from SE_BENC) or decrypted (obtained from SE_BDEC).

SE+00c8h SE Secure Booting seed value SE_BSEED

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BSEED[31:16]**															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BSEED[15:0]**															
Type	WO															
Reset	0															

BSEED Seed data needed to increase security of the Boot Secure function. Set the seed value before performing Boot Secure the first time.

SE+00cch SE Secure Booting encrypted data SE_BENC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BENC[31:16]**															
Type	RO															

Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BENC[15:0]**															
Type	RO															
Reset	0															

BENC Encrypted data from SE_BSRC.

SE+00d0h SE Secure Booting decrypted data SE_BDEC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BDEC[31:16]**															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BDEC[15:0]**															
Type	RO															
Reset	0															

BDEC Decrypted data from SE_BSRC.

3.17.3 Secure Booting Procedure

Secure Booting is the major feature of SE that protects the program contents on flash memory from modification, skip or hard copy. With a secure process and a unique chip ID (UID), SE can encrypt or decrypt a segment of instruction data in order.

Encryption procedure:

Activate the eFuse module.

Write the seed value into BSEED. The seed value can be any 32-bit value. The same seed value is necessary in the decryption procedure.

Write the control value into BCON.

Write source data (instruction) into BSRC and read the cipher text from BENC.

Repeat step 4 until all instructions are encrypted.

Decryption procedure:

Activate the eFuse module.

Write the seed value into BSEED. The seed value must be the same one used in the encryption procedure.

Write the control value into BCON. The control value must be the same one used in the encryption procedure.

Write the source data (instruction) into BSRC and read the plain text from BDEC.

Repeat step 4 until all instructions are decrypted.

Notes:

A bit length equal or less than 32 bits is acceptable for Secure Boot. E.g.: a 16-bit data 0x1234 is treated as 0x12340000 32-bit data and decrypted in the same manner.

For security reasons, access times to be encrypted or decrypted should not be the multiples of 4.

The internal states of Secure Booting function change under the following conditions, such that redundant register access is forbidden.

Write data into BSRC

Write data into BSEED

Read data from BENC or BDEC

As an example of the encryption and decryption of 16-bit data, consider the value 0xabcd:

Encryption:

The data is padded with zeros to obtain a 32-bit value: 0xabcd0000.

The encryption operation produces a value 0x12345678.

Decryption:

Only the most significant 16 bits 0x1234000 are considered and decrypted as 0xabcd7893.

The first 16 bits 0xabcd are retained, and 0x00007893 is ignored.

3.18 Real Time Clock

3.18.1 General Description

The Real Time Clock (RTC) module provides time and data information. The clock is based on a 32.768KHz oscillator with an independent power supply. When the mobile handset is powered off, a dedicated regulator supplies the RTC block. If the main battery is not present, a backup supply such as a small mercury cell battery or a large capacitor is used. In addition to providing timing data, an alarm interrupt is generated and can be used to power up the baseband core via the BBWAKEUP pin. Regulator interrupts corresponding to seconds, minutes, hours and days can be generated whenever the time counter value reaches a maximum value (e.g., 59 for seconds and minutes, 23 for hours, etc.). The year span is supported up to 2127. The maximum day-of-month values, which depend on the leap year condition, are stored in the RTC block.

3.18.2 Register Definitions

RTC+0000h Baseband power up RTC_BBPU

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY_BBPU												AUTO	BBPU	WRITE_EN	PWREN

Type	W					R/W	R/W	R/W	R/W

KEY_BBPU A bus write is acceptable only when KEY_BBPU=0x43.

AUTO Controls if BBWAKEUP is automatically in the low state when SYSRST# transitions from high to low.

0 BBWAKEUP is not automatically in the low state when SYSRST# transitions from high to low.

1 BBWAKEUP is automatically in the low state when SYSRST# transitions from high to low.

BBPU Controls the power of PMIC. If powerkey1=A357h and powerkey2=67D2h, PMIC takes on the value programmed by software; otherwise PMIC is low.

0 Power down

1 Power on

WRITE_EN When WRITE_EN is set to 0 by the software program, the RTC write interface is disabled until another system power on. This is equivalent to *RTC_debounce_counter_clear_b* signal. In most cases, you should write this bit same as BBPU.

PWREN

0 RTC alarm has no action on power switch.

When an RTC alarm occurs, BBPU is set to 1, and the system powers on by RTC alarm wakeup.

RTC+0004h RTC IRQ status RTC_IRQ_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															TCSTA	ALSTA
Type															R/C	R/C

ALSTA This register indicates the IRQ status and whether or not the alarm condition has been met.

0 No IRQ occurred; the alarm condition has not been met.

1 IRQ occurred; the alarm condition has been met.

TCSTA This register indicates the IRQ status and whether or not the tick condition has been met.

0 No IRQ occurred; the tick condition has not been met.

1 IRQ occurred; the tick condition has been met.

RTC+0008h RTC IRQ enable RTC_IRQ_EN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WING													ONESHOT	TC_EN	AL_EN
Type	R/O													R/W	R/W	R/W

ONESHOT Controls automatic reset of AL_EN and TC_EN.

AL_EN This register enables the control bit for IRQ generation if the alarm condition has been met.

0 Disable IRQ generation.

1 Enable the alarm time match interrupt. Clear the interrupt when ONESHOT is high upon generation of the corresponding IRQ.

TC_EN This register enables the control bit for IRQ generation if the tick condition has been met.

0 Disable IRQ generation.

Enable the tick time match interrupt. Clear the interrupt when ONESHOT is high upon generation of the corresponding IRQ.

WING This bit indicates that RTC is still writing to this register.

RTC+000Ch Counter increment IRQ enable RTC_CII_EN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WING						1/8SECCII	1/4SECCII	1/2SECCII	YEACII	MTHCII	DOWCII	DOMCII	HOUCII	MINCII	SECCII
Type	R/O						R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This register activates or de-activates the IRQ generation when the TC counter reaches its maximum value.

SECCII Set this bit to 1 to activate the IRQ at each second update.

MINCII Set the bit to 1 to activate the IRQ at each minute update.

HOUCII Set the bit to 1 to activate the IRQ at each hour update.

DOMCII Set the bit to 1 to activate the IRQ at each day-of-month update.

DOWCII Set the bit to 1 to activate the IRQ at each day-of-week update.

MTHCII Set the bit to 1 to activate the IRQ at each month update.

YEACII Set the bit to 1 to activate the IRQ at each year update.

1/2SECCII Set the bit to 1 to activate the IRQ at each one-half of a second update.

1/4SECCII Set the bit to 1 to activate the IRQ at each one-fourth of a second update.

1/8SECCII Set the bit to 1 to activate the IRQ at each one-eighth of a second update.

WING This bit indicates RTC is still writing to this register.

RTC+0010h RTC alarm mask RTC_AL_MASK

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WING									YEA_MSK	MTH_MSK	DOW_MSK	DOM_MSK	HOU_MSK	MIN_MSK	SEC_MSK
Type	R/O									R/W	R/W	R/W	R/W	R/W	R/W	R/W

The alarm condition for alarm IRQ generation depends on whether or not the corresponding bit in this register is masked. Warning: If you set all bits 1 in RTC_AL_MASK (i.e. RTC_AL_MASK=0x7f) and PWREN=1 in RTC_BBPU, it means alarm comes EVERY SECOND, not disabled.

SEC_MSK

0 Condition (RTC_TC_SEC = RTC_AL_SEC) is checked to generate the alarm signal.

1 Condition (RTC_TC_SEC = RTC_AL_SEC) is masked, i.e. the value of RTC_TC_SEC does not affect the alarm IRQ generation.

MIN_MSK

0 Condition (RTC_TC_MIN = RTC_AL_MIN) is checked to generate the alarm signal.

1 Condition (RTC_TC_MIN = RTC_AL_MIN) is masked, i.e. the value of RTC_TC_MIN does not affect the alarm IRQ generation.

HOU_MSK

0 Condition (RTC_TC_HOU = RTC_AL_HOU) is checked to generate the alarm signal.

1 Condition (RTC_TC_HOU = RTC_AL_HOU) is masked, i.e. the value of RTC_TC_HOU does not affect the alarm IRQ generation.

DOM_MSK

0 Condition (RTC_TC_DOM = RTC_AL_DOM) is checked to generate the alarm signal.

1 Condition (RTC_TC_DOM = RTC_AL_DOM) is masked, i.e. the value of RTC_TC_DOM does not affect the alarm IRQ generation.

DOW_MSK

0 Condition (RTC_TC_DOW = RTC_AL_DOW) is checked to generate the alarm signal.

1 Condition (RTC_TC_DOW = RTC_AL_DOW) is masked, i.e. the value of RTC_TC_DOW does not affect the alarm IRQ generation.

MTH_MSK

0 Condition (RTC_TC_MTH = RTC_AL_MTH) is checked to generate the alarm signal.

1 Condition (RTC_TC_MTH = RTC_AL_MTH) is masked, i.e. the value of RTC_TC_MTH does not affect the alarm IRQ generation.

YEA_MSK

0 Condition (RTC_TC_YEA = RTC_AL_YEA) is checked to generate the alarm signal.

Condition (RTC_TC_YEA = RTC_AL_YEA) is masked, i.e. the value of RTC_TC_YEA does not affect the alarm IRQ generation.

WING This bit indicates RTC is still writing to this register.

RTC+0014h RTC seconds time counter register RTC_TC_SEC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WING										TC_SECOND					
Type	R/O										R/W					

TC_SECOND The second initial value for the time counter. The range of its value is: 0-59.

WING This bit indicates RTC is still writing to this register.

RTC+0018h RTC minutes time counter register RTC_TC_MIN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WING										TC_MINUTE					
Type	R/O										R/W					

TC_MINUTE The minute initial value for the time counter. The range of its value is: 0-59.

WING This bit indicates RTC is still writing to this register.

RTC+001Ch RTC hours time counter register RTC_TC_HOU

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WING											TC_HOUR				
Type	R/O											R/W				

TC_HOUR The hour initial value for the time counter. The range of its value is: 0-23.

WING This bit indicates RTC is still writing to this register.

RTC+0x0020 RTC day-of-month time counter register RTC_TC_DOM

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WING											TC_DOM				
Type	R/O											R/W				

TC_DOM The day-of-month initial value for the time counter. The day-of-month maximum value depends on the leap year condition, i.e. 2 LSB of year time counter are zeros.

WING This bit indicates RTC is still writing to this register.

RTC+0x0024 RTC day-of-week time counter register RTC_TC_DOW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WING													TC_DOW		
Type	R/O													R/W		

TC_DOW The day-of-week initial value for the time counter. The range of its value is: 1-7.

WING This bit indicates RTC is still writing to this register.

RTC+0x0028 RTC month time counter register RTC_TC_MTH

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WING												TC_MONTH			
Type	R/O												R/W			

TC_MONTH The month initial value for the time counter. The range of its value is: 1-12.

WING This bit indicates RTC is still writing to this register.

RTC+0x002C RTC year time counter register RTC_TC_YEA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WING									AL_SECOND						
Type	R/O									R/W						

TC_YEAR The year initial value for the time counter. The range of its value is: 0-127. (2000-2127)

WING This bit indicates RTC is still writing to this register.

RTC+0x0030 RTC second alarm setting register RTC_AL_SEC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WING										AL_SECOND					
Type	R/O										R/W					

AL_SECOND The second value of the alarm counter setting. The range of its value is: 0-59.

WING This bit indicates RTC is still writing to this register.

RTC+0x0034 RTC minute alarm setting register RTC_AL_MIN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WING										AL_MINUTE					
Type	R/O										R/W					

AL_MINUTE The minute value of the alarm counter setting. The range of its value is: 0-59.

WING This bit indicates RTC is still writing to this register.

RTC+0x0038 RTC hour alarm setting register RTC_AL_HOU

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WING											AL_HOUR				
Type	R/O											R/W				

AL_HOUR The hour value of the alarm counter setting. The range of its value is: 0-23.

WING This bit indicates RTC is still writing to this register.

RTC+0x003C RTC day-of-month alarm setting register RTC_AL_DOM

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WING											AL_DOM				
Type	R/O											R/W				

AL_DOM The day-of-month value of the alarm counter setting. The day-of-month maximum value depends on the leap year condition, i.e. 2 LSB of year time counter are zeros.

WING This bit indicates RTC is still writing to this register.

RTC+0x0040 RTC day-of-week alarm setting register RTC_AL_DOW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WING													AL_DOW		
Type	R/O													R/W		

AL_DOW The day-of-week value of the alarm counter setting. The range of its value is: 1-7.

WING This bit indicates RTC is still writing to this register.

RTC+0x0044 RTC month alarm setting register RTC_AL_MTH

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WING												AL_MONTH			
Type	R/O												R/W			

AL_MONTH The month value of the alarm counter setting. The range of its value is: 1-12.

WING This bit indicates RTC is still writing to this register.

RTC+0x0048 RTC year alarm setting register RTC_AL_YEA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WING									AL_YEAR						
Type	R/O									R/W						

AL_YEAR The year value of the alarm counter setting. The range of its value is: 0-127. (2000-2127)

WING This bit indicates RTC is still writing to this register.

RTC+0050h RTC_POWERKEY1 register RTC_POWERKEY1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_POWERKEY1															
Type	R/W															

RTC+0054h RTC_POWERKEY2 register RTC_POWERKEY2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_POWERKEY2															
Type	R/W															

These register sets are used to determine if the real time clock has been programmed by software; i.e. the time value in real time clock is correct. When the real time clock is first powered on, the register contents are all undefined, therefore the time values shown are incorrect. Software needs to know if the real time clock has been programmed. Hence, these two registers are defined to solve this power-on issue. After software programs the correct value, these two register sets do not need to be updated. In addition to programming the correct time value, when the contents of these register sets are wrong, the interrupt is not generated. Therefore, the real time clock does not generate the interrupts before the software programs the registers; unwanted interrupt due to wrong time value do not occur. The correct values of these two register sets are:

RTC_POWERKEY1 A357h

RTC_POWERKEY2 67D2h

RTC+0058h PDN1 RTC_PDN1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WING	DBING							RTC_PDN1[7:0]							
Type	R/O	R/O							R/W							

RTC_PDN1[3:1] is for reset de-bounce mechanism.

0 2ms

1 8ms

2 32ms

3 128ms

4 256ms

5 512ms

6 1024ms

7 2048ms

RTC_PDN1[7:4] & RTC_PDN1[0] is the spare register for software to keep power on and power off state information.

DBING This bit indicates RTC is still de-bouncing.

WING This bit indicates RTC is still writing to this register.

RTC+005Ch PDN2 RTC_PDN2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WING								RTC_PDN2[7:0]							
Type	R/O								R/W							

RTC_PDN2 The spare register for software to keep power on and power off state information.

WING This bit indicates RTC is still writing to this register.

RTC+0060h RTC writing completed flag RTC_WOK

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name														WING3	WING2	WING1
Type														R/O	R/O	R/O

WING1 This bit indicates RTC is still writing POWERKEY1.

WING2 This bit indicates RTC is still writing POWERKEY2.

WING3 This bit indicates RTC is still writing BBPU.

RTC+0064h Spare register for specific purpose RTC_SPAR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RTC_SPAR															
Type	R/W															

RTC_SPAR These registers are reserved for specific purpose.

3.19 Divider

To ease the processing load of MCU, a divider is employed here. The divider can operate signed and unsigned 32bit/32bit division, as well as modulus. The processing time of the divider is from 1 clock cycle to 33 clock cycles, which depends upon the magnitude of the value of the dividend. The detailed processing time is listed below in Table 21. From the table we can see that there are two kind of processing time (except for when the dividend is zero) in an item. Which kind depends on whether there is the need for restoration at the last step of the division operation.

After the divider is started by setting START to "1" in Divider Control Register, DIV_RDY will go low, and it will be asserted after the division process is finished. MCU could detect this status bit by polling it to know the correct access timing. In order to simplify polling, only the value of register DIV_RDY will appear while Divider Control Register is read. Hence, MCU does not need to mask other bits to extract the value of DIV_RDY.

In GSM/GPRS system, many divisions are executed with some constant divisors. Therefore, some often-used constants are stored in the divider to speed up the process. By controlling control bits IS_CNST and CNST_IDX in Divider Control register, one can start a division without giving a divisor. This could save the time for writing divisor in and the instruction fetch time, and thus make the process more efficient.

Signed Division		Unsigned Division	
Dividend	Clock Cycles	Dividend	Clock Cycles
0000_0000h	1	0000_0000h	1
0000_00ffh – (-0000_0100h), excluding 0x0000_0000	8 or 9	0000_0001h - 0000_00ffh	8 or 9
0000_ffffh – (-0001_0000h)	16 or 17	0000_0100h - 0000_ffffh	16 or 17
00ff_ffffh – (-0100_0000h)	24 or 25	0001_0000h - 00ff_ffffh	24 or 25
7fff_ffffh – (-8000_0000h)	32 or 33	0100_0000h - ffff_ffffh	32 or 33

Table 27 Processing time in different value of dividend.

3.19.1 Register Definitions

DIVIDER+0000h Divider Control Register DIV_CON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														CNST_IDX		
Type														WO		
Reset														0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											IN_CNST	SIGN			DIV_RDY	START
Type											WO	WO			RO	WO
Reset											0	1			1	0

START To start division. It will return to 0 after division has started.

DIV_RDY Current status of divider. Note that when DIV_CON register is read, only the value of DIV_RDY will appear. That means program does not need to mask other part of the register to extract the information of DIV_RDY.

0 division is in progress.

division is finished.

SIGN To indicate signed or unsigned division.

0 Unsigned division.

1 Signed division.

IS_CNST To indicate if internal constant value should be used as a divisor. If IS_CNST is enabled, User does not need to write the value of the divisor, and divider will automatically use the internal constant value instead. What value divider will use depends on the value of CNST_IDX.

0 Normal division. Divisor is written in via APB

1 Using internal constant divisor instead.

CNST_IDX Index of constant divisor.

0 divisor = 13

divisor = 26

divisor = 51

divisor = 52

divisor = 102

divisor = 104

DIVIDER +0004h Divider Dividend register DIV_DIVIDEND

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	DIVIDEND[31:16]															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIVIDEND[15:0]															
Type	WO															
Reset	0															

Dividend.

DIVIDER +0008h Divider Divisor register DIV_DIVISOR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DIVISOR[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIVISOR[15:0]															
Type	R/W															
Reset	0															

Divisor.

DIVIDER +000Ch Divider Quotient register DIV_QUOTIENT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QUOTIENT[31:16]															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QUOTIENT[15:0]															
Type	RO															
Reset	0															

Quotient.

DIVIDER +0010h Divider Remainder register DIV_REMAINDER

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	REMAINDER[31:16]															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REMAINDER[15:0]															
Type	RO															
Reset	0															

Remainder.

3.19.2 Design

3.19.2.1 Implementation

To avoid largely increasing area cost, radix-2 non-restoring divider architecture is adopted here, which can provide signed and unsigned 2's complement division and modulus with 32-bit dividend and 32-bit divisor. After processing, 32-bit quotient and 32-bit remainder will be generated, and the calculation latency is from 1 clock cycle, if dividend is zero, to 33 clock cycles in the worst case.

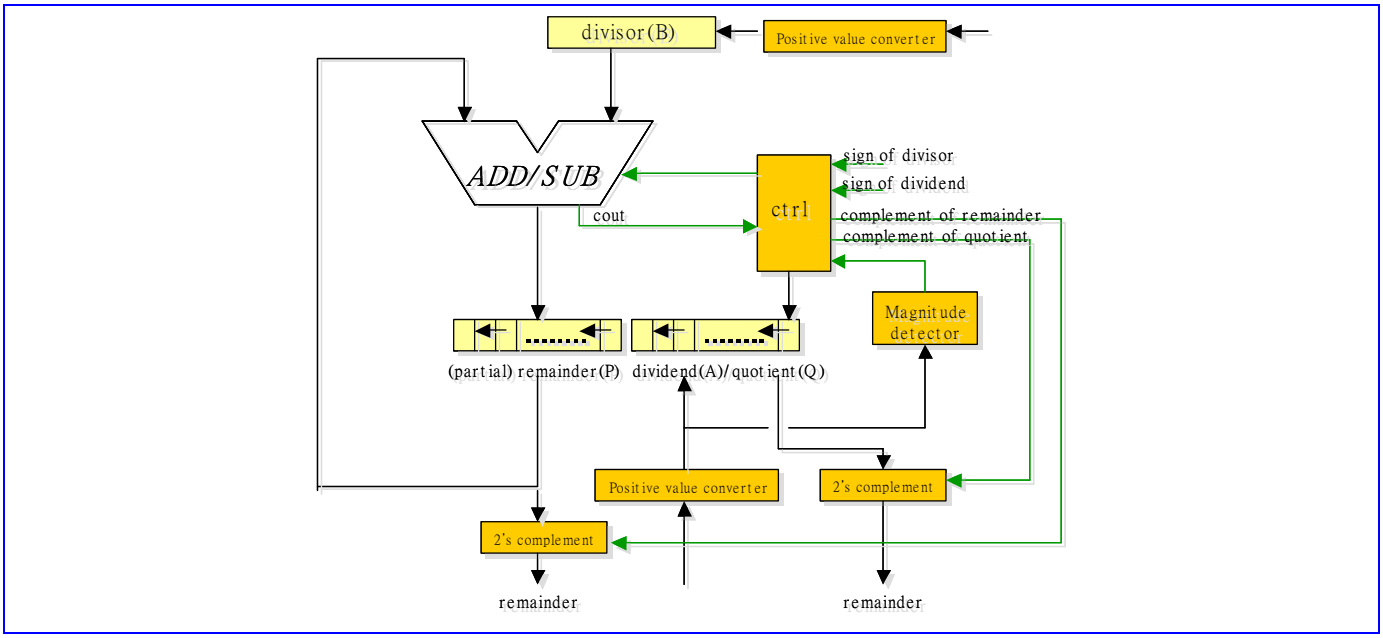


Figure 35 Architecture of radic-2 non-restoring divider for MCU system

Non-restoring divider has an advantage that it does not need to determine if a restoring operation is needed in each step of division. The only determination is executed at the end of division, which is used to correct the value of remainder. This advantage can reduce the complexity and ease the calculation in each step.

The adder/subtractor and the partial remainder register are 34 bits width. The additional 2 MSB are guard bits to contain the possible largest/smallest value in division. Dividend and quotient share the same register, and it is 32 bits wide.

The operation of non-restoring unsigned divider is very easy to understand. It is just like calculating division by hand. Generally we can divide each step into three actions. That is

- (i) Shift the register pair (P,A) one bit left

- (ii-a) If P is negative, add B to P
- (ii-b) If P is positive, subtract B from P
- (iii) If P is negative, set the low-order bit of A to 0, otherwise set it to 1

After n cycles, the quotient will be in dividend register (A). If partial remainder is positive at this moment, it is the final remainder. Otherwise it has to be restored, adding B to it, to generate the final remainder. There is an example below to illustrate how a non-restoring division operates.

P	A	Operation
00000	1110	Divide 14 = 1110 by 3 = 11. B register always contains 0011
00001	110	step 1(i): shift
+11101		step 1(ii-b): subtract b (add two's complement)

11110	1100	step 1(iii): P is negative, so set quotient bit to 0
11101	100	step 2(i): shift
+00011		step 2(ii-a): add b

00000	1001	step 2(iii): P is positive, so set quotient bit to 1
00001	001	step 3(i): shift
+11101		step 3(ii-b): subtract b

11110	0010	step 3(iii): P is negative, so set quotient bit to 0
11100	010	step 4(i): shift
+00011		step 4(ii-a): add b

11111	0100	step 4(iii): P is negative, set quotient bit to 0
+00011		Remainder is negative, so do final restore step

00010		

For a signed division, what we need to do is to just change dividend and divisor to positive, and adjust the sign of quotient and remainder upon the sign of dividend and divisor. Namely, if the sign of dividend and divisor is different, then the sign of quotient is a minus. In the same manner, if dividend is positive, the sign of remainder will be a plus too.

For many applications, the dividend is not so large, and it would be inefficient for MCU waiting for the divider to spend 33 cycles to finish the operation. Therefore, a dividend magnitude detector is designed here to detect how many bits the dividend need to express its value, and skip un-used bit upon the detection result to speed up the processing. There are four kinds of dividend length that are supported in this detector: 8-bit, 16-bit, 24-bit, and 32-bit. For example, if magnitude detector detects only 8 bits are needed to express the dividend, the dividend will left shift 24 bits at the beginning of the division to skip the

calculation of the 24 MSB. This will reduce the total process time to 8 or 9 clock cycles. In real implementation, it is not necessary to really shift 24 bits at the beginning. In our design, it was implemented just by directing bit 7 to the LSB of partial remainder register. This can also be applied to other cases. All of the processing time corresponding to the bit number needed to express a dividend are listed in Table 21.

3.19.2.2 Inputs/Outputs

Group	Signal	I/O	Description
RESET	preset_rstb	I	APB reset
CLOCK	bclk_ck	I	Core clock of modules connected to APB bus only with power down control
APB	penable	I	APB penable signal
APB	psel	I	APB psel signal
APB	pwrite	I	APB pwrite signal
APB	paddr[15:0]	I	APB address
APB	pwdata[31:0]	I	APB write data
APB	prdata[31:0]	O	APB read data

3.20 CSD Accelerator

3.20.1 General Description

This unit performs the data format conversion of RA0, RA1, and FAX in CSD service. CSD service consists of two major functions: data flow throttling and data format conversion. The data format conversion is a bit-wise operation and takes a number of instructions to complete a conversion. Therefore, it is not efficient to do by MCU itself. A coprocessor, CSD accelerator, is designed here to reduce the computing power needed to perform this function.

CSD accelerator only helps in converting data format; the data flow throttling function is still implemented by the MCU. CSD accelerator performs three types of data format conversion, RA0, RA1, and FAX.

For RA0 conversion, only uplink RA0 data format conversion is provided here. This is because there are too many judgments on the downlink path conversion, which will greatly increase area cost. Uplink RA0 conversion is to insert one start bit and one stop bit before and after a byte, respectively, during 16 bytes. **Figure 36** illustrates the detailed conversion table.

RA0 converter can only process RA0 data state by state. Before filling in new data, software must make sure the converted data of certain state is withdrawn, or the converted data will be replaced by the new data. For example, if 32-bit data is written, and the state pointer goes from state 0 to state 1, and word ready of state 0 is asserted; then, before writing the next 32-bit data, the word of state 0 should be withdrawn first, or the data will be lost.

RA0 records the number of written bytes, state pointer, and ready state word. The information can help software to perform flow control. See Register Definition for more detail.

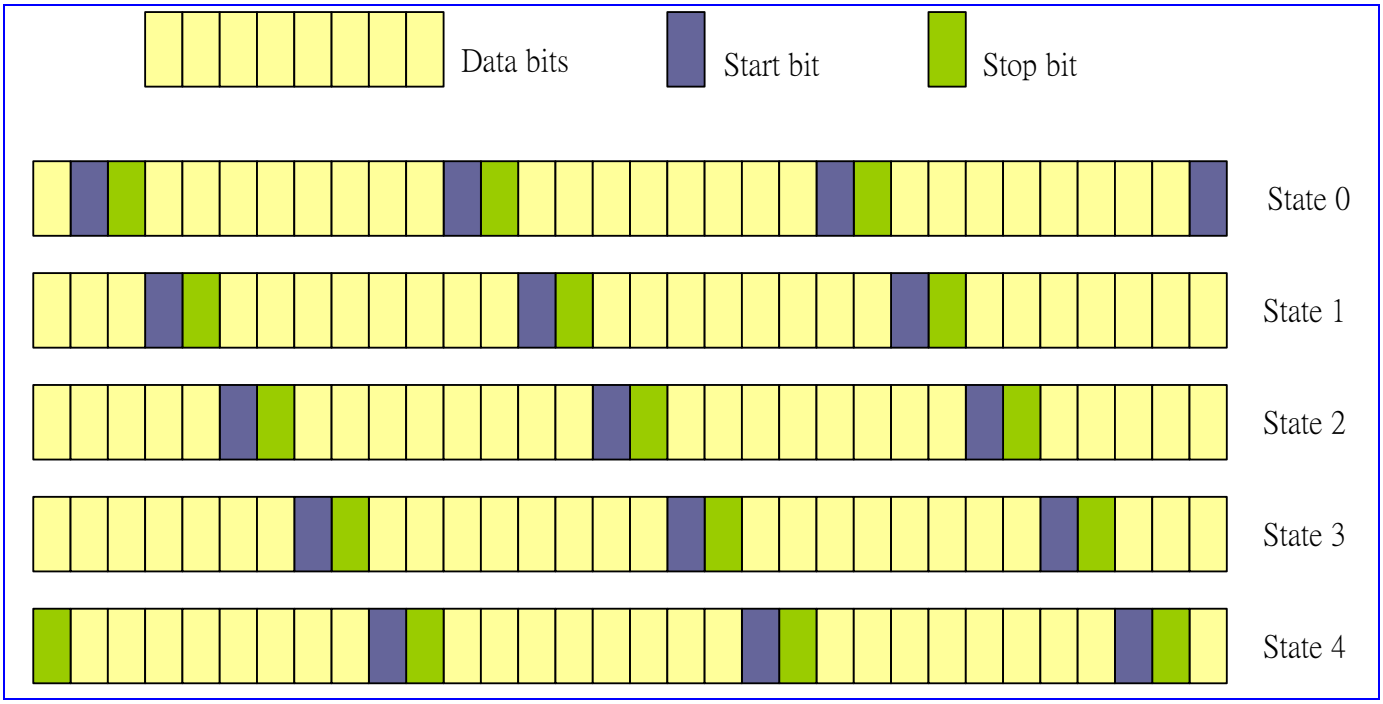


Figure 36 data format conversion of RA0

For RA1 conversion, both directions, downlink and uplink, are supported. The data formats vary in different data rate. The detailed conversion table is shown in **Figure 37** and **Figure 38**. The yellow part is the payload data, and the blue part is the status bit.

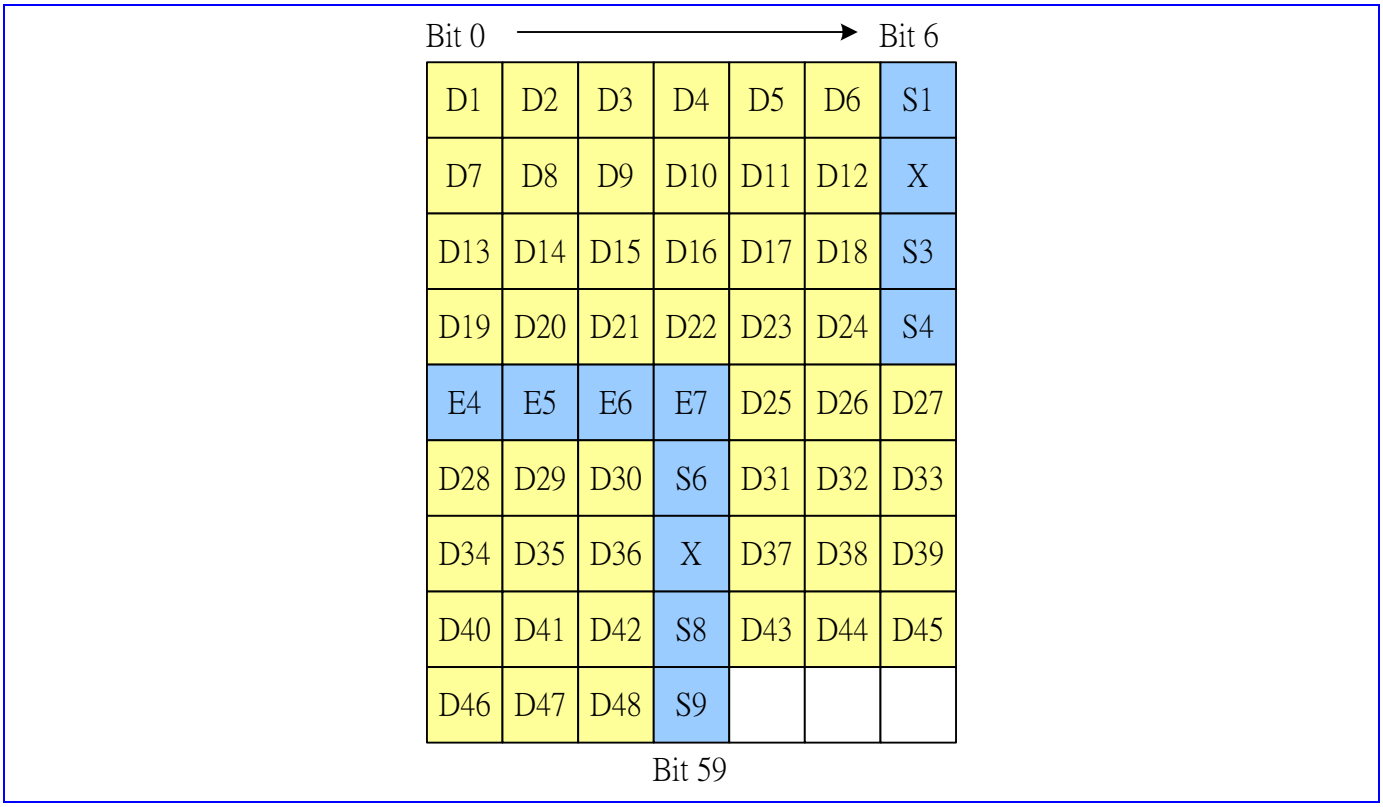


Figure 37 data format conversion for 6k/12k RA1

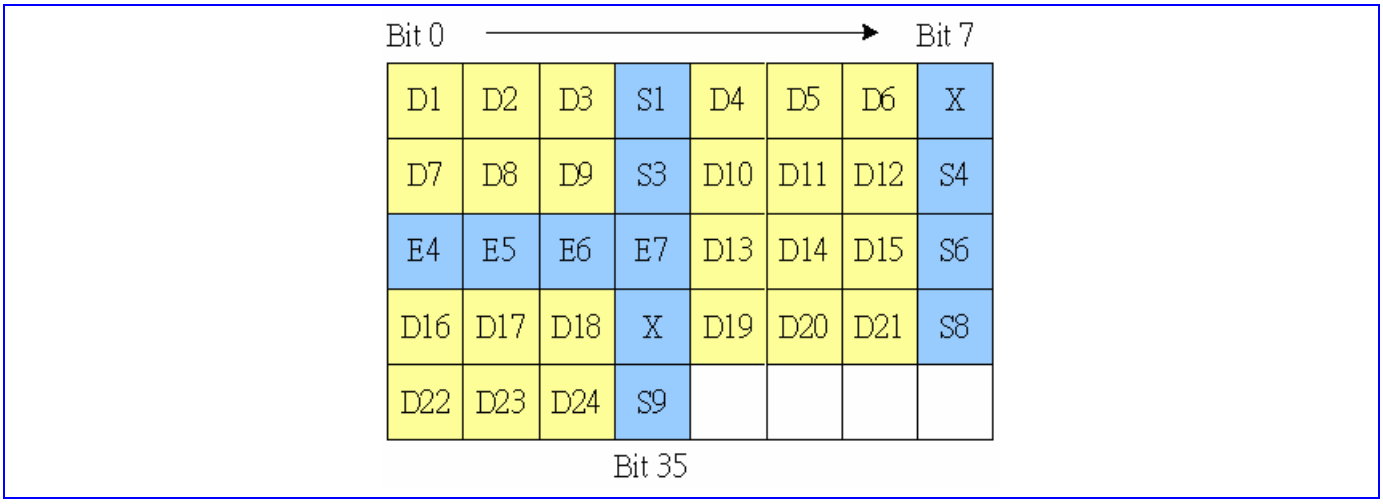


Figure 38 data format conversion for 3.6k RA1

For FAX, two types of bit-reversal functions are provided. One is bit-wise reversal, and the other is byte-wise reversal, which are illustrated in **Figure 39** and **Figure 40**, respectively.

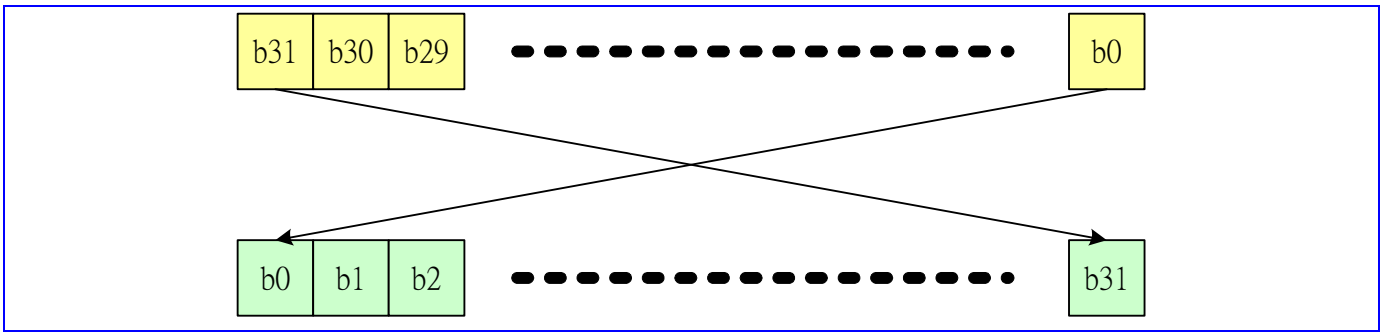


Figure 39 Type 1 bit reverse

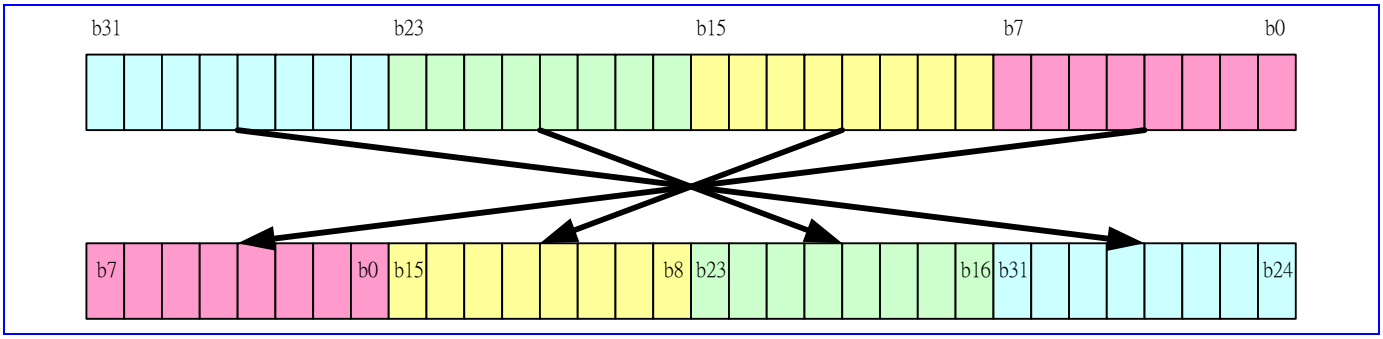


Figure 40 Type 2 bit reverse

Register Address	Register Function	Acronym
CSD + 0000h	CSD RA0 Control Register	CSD_RA0_CON
CSD + 0004h	CSD RA0 Status Register	CSD_RA0_STA
CSD + 0008h	CSD RA0 Input Data Register	CSD_RA0_DI
CSD + 000Ch	CSD RA0 Output Data Register	CSD_RA0_DO
CSD + 0100h	CSD RA1 6K/12K Uplink Input Data Register 0	CSD_RA1_6K_12K_ULDI0

CSD + 0104h	CSD RA1 6K/12K Uplink Input Data Register 1	CSD_RA1_6K_12K_ULDI1
CSD + 0108h	CSD RA1 6K/12K Uplink Status Data Register	CSD_RA1_6K_12K_ULSTUS
CSD + 010Ch	CSD RA1 6K/12K Uplink Output Data Register 0	CSD_RA1_6K_12K_ULDO0
CSD + 0110h	CSD RA1 6K/12K Uplink Output Data Register 1	CSD_RA1_6K_12K_ULDO1
CSD + 0200h	CSD RA1 6K/12K Downlink Input Data Register 0	CSD_RA1_6K_12K_DLDI0
CSD + 0204h	CSD RA1 6K/12K Downlink Input Data Register 1	CSD_RA1_6K_12K_DLDI1
CSD + 0208h	CSD RA1 6K/12K Downlink Output Data Register 0	CSD_RA1_6K_12K_DLDO0
CSD + 020Ch	CSD RA1 6K/12K Downlink Output Data Register 1	CSD_RA1_6K_12K_DLDO1
CSD + 0210h	CSD RA1 6K/12K Downlink Status Data Register	CSD_RA1_6K_12K_DLSTUS
CSD + 0300h	CSD RA13.6K Uplink Input Data Register 0	CSD_RA1_3P6K_ULDI0
CSD + 0304h	CSD RA13.6K Uplink Status Data Register	CSD_RA1_3P6K_ULSTUS
CSD + 0308h	CSD RA13.6K Uplink Output Data Register 0	CSD_RA1_3P6K_ULDO0
CSD + 030Ch	CSD RA13.6K Uplink Output Data Register 1	CSD_RA1_3P6K_ULDO1
CSD + 0400h	CSD RA1 3.6K Downlink Input Data Register 0	CSD_RA1_3P6K_DLDI0
CSD + 0404h	CSD RA1 3.6K Downlink Input Data Register 1	CSD_RA1_3P6K_DLDI1
CSD + 0408h	CSD RA1 3.6K Downlink Output Data Register 0	CSD_RA1_3P6K_DLDO0
CSD + 040Ch	CSD RA1 3.6K Downlink Status Data Register	CSD_RA1_3P6K_DLSTUS
CSD + 0500h	CSD FAX Bit Reverse Type 1 Input Data Register	CSD_FAX_BR1_DI
CSD + 0504h	CSD FAX Bit Reverse Type 1 Output Data Register	CSD_FAX_BR1_DO
CSD + 0510h	CSD FAX Bit Reverse Type 2 Input Data Register	CSD_FAX_BR2_DI
CSD + 0514h	CSD FAX Bit Reverse Type 2 Output Data Register	CSD_FAX_BR2_DO

Table 28 CSD Accelerater Registers

3.20.2 Register Definitions

CSD+0000h CSD RA0 Control Register CSD_RA0_CON

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RST	BTS0		VLD_BYTE		
Type											WO	WO		WO		
Reset											0	0		100		

VLD_BYTE Specify how many valid bytes in the current input data. It must be specified before filling data in.

BTS0 Back to state 0. Force RA0 converter go back to state 0. Incomplete word will be padded by STOP bit. For instance, back-to-state0 command is issued after 8 byte data are filled in. Then these bit after the 8th byte will be padded with stop bits, and RDYWD2 is asserted. After removing state word 2, the state pointer goes back to state 0. Note that new data filling should take place after removing state word 2, or the state pointer may be out of order.

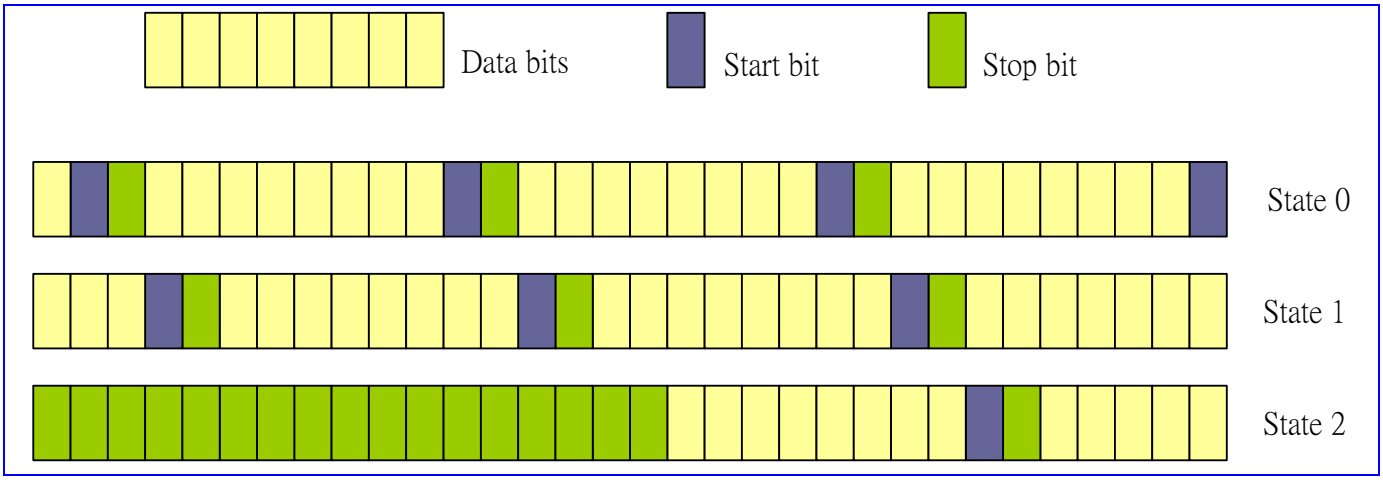


Figure 41 Example of Back to state 0

RST Reset RA0 converter. In case, erroneously operation makes data disordered. This bit can restore all state to original state.

CSD+0004h CSD RA0 Status Register CSD_RA0_STA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					BYTECNT				CRTSTA		RDYWD					
Type					RO				RO		RC					
Reset					0				0		0					

RDYWD0~4 Ready word. To indicate which state word is ready for withdrawal. Data should be withdrawn before next data fills into CSD_RA0_DI, if there are any bits asserted.

0 Not ready

1 Ready

CRTSTA current state. State0 ~ state4. To indicate which state word software is filling in.

BYTECNT The total number of bytes software is filling in.

CSD+0008h CSD RA0 Input Data Register CSD_RA0_DI

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DIN															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	WO															
Reset	0															

DIN The RA0 convert input data. Ready word indicator shall be check before filling in data. If any words are ready, withdraw them first; otherwise the ready data in RA0 converter will be replaced.

CSD+000Ch CSD RA0 Output Data Register CSD_RA0_DO

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOUT															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															
Type	RO															
Reset	0															

DOUT RA0 converted data. The return data corresponds to the ready word indicator defined in CSD_RA0_STA register. The five bit of RDYWD map to state0 ~ state 4 accordingly. When CSD_RA0_DO is read, the asserted state word will be returned. If there are two state words asserted at the same time, the lower one will be returned.

CSD+0100h CSD RA1 6K/12K Uplink Input Data Register 0 CSD_RA1_6K_12K_ULDI0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DIN															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															

Type	WO
Reset	0

DIN The D1 to D32 of RA1 uplink data.

CSD+0104h CSD RA1 6K/12K Uplink Input Data Register 1 CSD_RA1_6K_12K_ULDI1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	WO															
Reset	0															

DIN The D33 to D48 of RA1 uplink data.

CSD+0108h CSD RA1 6K/12K Uplink Status Data Register CSD_RA1_6K_12K_ULSTUS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										E7	E6	E5	E4	X	SB	SA
Type										WO	WO	WO	WO	WO	WO	WO
Reset										0	0	0	0	0	0	0

SA Represents S1, S3, S6, and S8 of status bits.

SB Represents S4 and S9 of status bits.

X Represents X of status bits.

E4 Represents E4 of status bits.

E5 Represents E5 of status bits.

E6 Represents E6 of status bits.

E7 Represents E7 of status bits.

CSD+010Ch CSD RA1 6K/12K Uplink Output Data Register 0 CSD_RA1_6K_12K_ULDO0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOUT															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOU															
Type	RO															
Reset	0															

DOUT The bit 0 to bit 31 of RA1 6K/12K uplink frame.

CSD+0110h CSD RA1 6K/12K Uplink Output Data Register 1 CSD_RA1_6K_12K_ULDO1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DOUT											
Type					RO											
Reset					0											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															
Type	RO															
Reset	0															

DOUT The bit32 to bit 59 of RA1 6K/12K uplink frame.

CSD+0200h CSD RA1 6K/12K Downlink Input Data Register 0 CSD_RA1_6K_12K_DLDI0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DIN															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	WO															
Reset	0															

DIN The bit 0 to bit 31 of RA1 6K/12K downlink frame.

CSD+0204h CSD RA1 6K/12K Downlink Input Data Register 1 CSD_RA1_6K_12K_DLDI1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DIN											
Type					WO											
Reset					0											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	WO															
Reset	0															

DIN The bit32 to bit 59 of RA1 6K/12K downlink frame.

CSD+0208h CSD RA1 6K/12K Downlink Output Data Register 0 CSD_RA1_6K_12K_DLDO0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOUT															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															
Type	RO															
Reset	0															

DOUT The D1 to D32 of RA1 downlink data.

CSD+020Ch CSD RA1 6K/12K Downlink Output Data Register 1 CSD_RA1_6K_12K_DLDO1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															
Type	RO															

Reset	0

DOUT The D33 to D48 of RA1 downlink data.

CSD+0210h CSD RA1 6K/12K Downlink Status Data Register CSD_RA1_6K_12K_DLSTUS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										E7	E6	E5	E4	X	SB	SA
Type										RO	RO	RO	RO	RO	RO	RO
Reset										0	0	0	0	0	0	0

SA The result of majority votes of S1, S3, S6 and S8. SA is “0” if equal vote.

SB The result of majority votes of S4 and S9. SB is “0” if equal vote.

X The result of majority votes of two X bits in downlink frame. X is “0” if equal vote.

E4 Represents E4 of status bits.

E5 Represents E5 of status bits.

E6 Represents E6 of status bits.

E7 Represents E7 of status bits.

CSD+0300h CSD RA1 3.6K Uplink Input Data Register 0 CSD_RA1_3P6K_ULDI0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									DIN							
Type									WO							
Reset									0							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	WO															
Reset	0															

DIN The D1 to D24 of RA1 3.6K uplink data.

CSD+0304h CSD RA1 3.6K Uplink Status Data Register

CSD_RA1_3P6K_ULSTUS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										E7	E6	E5	E4	X	SB	SA
Type										WO	WO	WO	WO	WO	WO	WO
Reset										0	0	0	0	0	0	0

SA Represents S1, S3, S6, and S8 of status bits.

SB Represents S4 and S9 of status bits.

X Represents X of status bits.

E4 Represents E4 of status bits.

E5 Represents E5 of status bits.

E6 Represents E6 of status bits.

E7 Represents E7 of status bits.

CSD+0308h CSD RA1 3.6K Uplink Output Data Register 0

CSD_RA1_3P6K_ULDO0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOUT															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															
Type	RO															
Reset	0															

DOUT The bit 0 to bit 31 of RA1 3.6K uplink frame

CSD+030Ch CSD RA1 3.6K Uplink Output Data Register 1

CSD_RA1_3P6K_ULDO1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DOUT			
Type													RO			
Reset													0			

DOUT The bit 32 to bit 35 of RA1 3.6K uplink frame

CSD+0400h CSD RA1 3.6K Downlink Input Data Register 0 CSD_RA1_3P6K_DLDI0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DIN															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	WO															
Reset	0															

DIN The bit 0 to bit 31 of RA1 3.6K downlink frame

CSD+0404h CSD RA1 3.6K Downlink Input Data Register 1 CSD_RA1_3P6K_DLDI1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DIN			
Type													WO			
Reset													0			

DIN The bit 32 to bit 35 of RA1 3.6K downlink frame

CSD+0408h CSD RA1 3.6K Downlink Output Data Register 0 CSD_RA1_3P6K_DLDO0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name									DOUT							
Type									RO							
Reset									0							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															
Type	RO															
Reset	0															

DIN The D1 to D24 of RA1 3.6K downlink data.

CSD+040Ch CSD RA1 3.6K Downlink Status Data Register CSD_RA1_3P6K_DL STUS

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										E7	E6	E5	E4	X	SB	SA
Type										RO	RO	RO	RO	RO	RO	RO
Reset										0	0	0	0	0	0	0

SA The result of majority votes of S1, S3, S6 and S8. SA is “0” if equal vote.

SB The result of majority votes of S4 and S9. SB is “0” if equal vote.

X The result of majority votes of two X bits in downlink frame. X is “0” if equal vote.

E4 Represents E4 of status bits.

E5 Represents E5 of status bits.

E6 Represents E6 of status bits.

E7 Represents E7 of status bits.

CSD+0500h CSD FAX Bit Reverse Type 1 Input Data Register CSD_FAX_BR1_DI

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DIN															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															

Type	WO
Reset	0

DIN 32-bit input data for type 1 bit reverse of FAX data. The action of Type 1 bit reverse is to reverse this word by word.

CSD+0504h CSD FAX Bit Reverse Type 1 Output Data Register CSD_FAX_BR1_DO

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOUT															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															
Type	RO															
Reset	0															

DOUT 32-bit result data for type 1 bit reverse of FAX data.

CSD+0510h CSD FAX Bit Reverse Type 2 Input Data Register CSD_FAX_BR2_DI

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DIN															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIN															
Type	WO															
Reset	0															

DIN 32-bit input data for type 2 bit reverse of FAX data. The action of Type 1 bit reverse is to reverse this word by byte.

CSD+0514h CSD FAX Bit Reverse Type 2 Output Data Register CSD_FAX_BR2_DO

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOUT															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOUT															
Type	RO															

Reset	0

DOUT 32-bit result data for type 2 bit reverse of FAX data.

3.20.3 Design

3.20.3.1 Inputs/Outputs

Group	Signal	I/O	Description
RESET	preset_rstb	I	APB reset
CLOCK	pclk_ck	I	APB bus clock, gated
APB	penable	I	APB penable signal
APB	psel	I	APB psel signal
APB	pwrite	I	APB pwrite signal
APB	paddr[15:0]	I	APB address
APB	pwdata[31:0]	I	APB write data
APB	prdata[31:0]	O	APB read data

3.21 FCS Codec

3.21.1 General Description

FCS (Frame Check Sequence) is used to detect errors in the following information bits:

- RLP-frame of CSD services in GSM. The frame length is fixed as 240 or 576 bits including the 24-bit FCS field.
- LLC-frame of GPRS service. The frame length is determined by the information field, and length of the FCS field is 24-bit.

Generation of the frame check sequence is very similar to the CRC coding in baseband signal processing. ETSI GSM specifications 04.22 and 04.64 both define the coding rule. The coding rules are:

1. 1. The CRC shall be ones complement of the modulo-2 sum of:

- the remainder of $x^k \cdot (x^{23}+x^{22}+x^{21}+...+x^2+x+1)$ modulo-2 divided by the generator polynomial, where k is the number of bits of the dividend. (i.e. fill the shift registers with all ones initially before feeding data)
- the remainder of the modulo-2 division by the generator polynomial of the product of x^{24} by the dividend, which are the information bits.

2. 2. The CRC-24 generator polynomial is:

$G(x)=x^{24}+x^{23}+x^{21}+x^{20}+x^{19}+x^{17}+x^{16}+x^{15}+x^{13}+x^8+x^7+x^5+x^4+x^2+1$

3. 3. The 24-bit CRC are appended to the data bits in the MSB-first manner.
4. 4. Decoding is identical to encoding except that data fed into the syndrome circuit is 24-bit longer than the information bits at encoding. The dividend is also multiplied by x^{24}. If no error occurs, the remainder should satisfy

$R(x)=x^{22}+x^{21}+x^{19}+x^{18}+x^{16}+x^{15}+x^{11}+x^{8}+x^{5}+x^{4}$ (0x6d8930)

And the parity output word will be 0x9276cf.

In contrast to conventional CRC, this special coding scheme makes the encoder fully identical to the decoder and simplifies the hardware design.

3.21.2 Register Definitions

FCS+0000h FCS input data register FCS_DATA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

THE data bits input. First write of this register is the starting point of the encode or decode process.

DX X=0…15. The input format is $D15\cdot x^{n}+ D14\cdot x^{n-1}+ D13\cdot x^{n-2}+ \ldots + Dk\cdot x^{k}+ \ldots$, thus D15 is the first bit being pushed into the shift register. If the last data word is less than 16 bits, the rest bits are neglected.

FCS+0004h Input data length indication register FCS_DLEN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LEN															
Type	WO															

THE MCU specifies the total data length in bits to be encoded or decoded.

LEN The data length. A number of multiple-of-8 is required (Number_of_Bytes x 8)

FCS+0x0008h FCS parity output register 1, MSB part FCS_PAR1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
Type	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FCS+000Ch FCS parity output register 2, LSB part FCS_PAR2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									P23	P22	P21	P20	P19	P18	P17	P16
Type									RC	RC	RC	RC	RC	RC	RC	RC
Reset									0	0	0	0	0	0	0	0

PARITY bits output. For FCS_PAR2, bit 8 to bit15 will be filled by zeros when reading.

PX X=0…23. The output format is $P23 \cdot D^{23} + P22 \cdot D^{22} + P21 \cdot D^{21} + \ldots + Pk \cdot D^{k} + \ldots + P1 \cdot D^{1} + P0$, thus P23 is the earliest bit being popped out from the shift register and first appended to the information bits. In other words, {FCS_PAR2[7:0], FCS_PAR1[15:8], FCS_PAR1[7:0] } is the order of appending parity to data.

FCS+0010h FCS codec status register FCS_STAT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														BUSY	FER	RDY
Type														RC	RC	RC
Reset														0	1	0

BUSY Since the codec works in serial manner and the data word is input in parallel manner, BUSY = 1 indicates that current data word is being processed and write to FCS_DATA is invalid. BUSY = 0 allows write of FCS_DATA during encode or decode process.

FER Frame error indication, only for decode mode. FER = 0 means no error occurs and FER = 1 means the parity check has failed. Write of FCS_RST.RST or first write of FCS_DATA will reset this bit to 0.

RDY When RDY = 1, the encode or decode process has been finished. For encode, the parity data in FCS_PAR1 and FCS_PAR2 are correctly available. For decode, FCS_STAT.FER indication is valid. Write of FCS_RST.RST or first write of FCS_DATA will reset this bit to 0.

FCS+0014h FCS codec reset register FCS_RST

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													EN_DE	PAR	BIT	RST
Type													WO	WO	WO	WO

RST RST = 0 resets the CRC coprocessor. Before setup of FCS codec, the MCU needs to set RST = 0 to flush the shift register content before encode or decode.

BIT BIT = 0 means not to invert the bit order in a byte of data words when the codec is running. BIT = 1 means the bit order in a byte written in FCS_DATA should be reversed.

PAR PAR = 0 means not to invert the bit order in a byte of parity words when the codec is running, include reading of FCS_PAR1 and FCS_PAR2. PAR = 1 means bit order of parity words should be reversed, in decoding or encoding.

EN_DE EN_DE = 0 means encode; EN_DE = 1 means decode

3.21.3 Design

3.21.3.1 Architecture

Generation of the frame check sequence is very similar to the CRC coding in baseband signal processing. ETSI GSM specifications 04.22 and 04.64 both define the coding rule. The coding rules are:

5. 1. The CRC shall be ones complement of the modulo-2 sum of:

- the remainder of $x^{k} \cdot (x^{23}+x^{22}+x^{21}+\ldots+x^{2}+x+1)$ modulo-2 divided by the generator polynomial, where k is the number of bits of the dividend. (i.e. fill the shift registers with all ones initially before feeding data)
- the remainder of the modulo-2 division by the generator polynomial of the product of x^{24} by the dividend, which are the information bits.

6. 2. The CRC-24 generator polynomial is:

$G(x)=x^{24}+x^{23}+x^{21}+x^{20}+x^{19}+x^{17}+x^{16}+x^{15}+x^{13}+x^{8}+x^{7}+x^{5}+x^{4}+x^{2}+1$

7. 3. The 24-bit CRC are appended to the data bits in the MSB-first manner.

8. 4. Decoding is identical to encoding except that data fed into the syndrome circuit is 24-bit longer than the information bits at encoding. The dividend is also multiplied by x^{24}. If no error occurs, the remainder should satisfy

$R(x)=x^{22}+x^{21}+x^{19}+x^{18}+x^{16}+x^{15}+x^{11}+x^{8}+x^{5}+x^{4}$ (0x6d8930)

And the parity output word will be 0x9276cf.

Figure 42 is the architecture of the FCS codec. The codec is connected to APB and is very similar to the CRC coprocessor in the DSP subsystem. The input is 16-bit in parallel and a busy flag is used for the MCU to check if the next data word can be written into the FCS_DATA register. The total data length is specified in the FCS_DLEN register. There is no data buffer inside the codec, thus we need FCS_STAT.RDY to indicate that the encoding or decoding is done and the result can be read by the MCU. For encode, the parity bits are present in the FCS_PAR1 and FCS_PAR2 registers. For decode, the parity check result is present in FCS_STAT.FER.

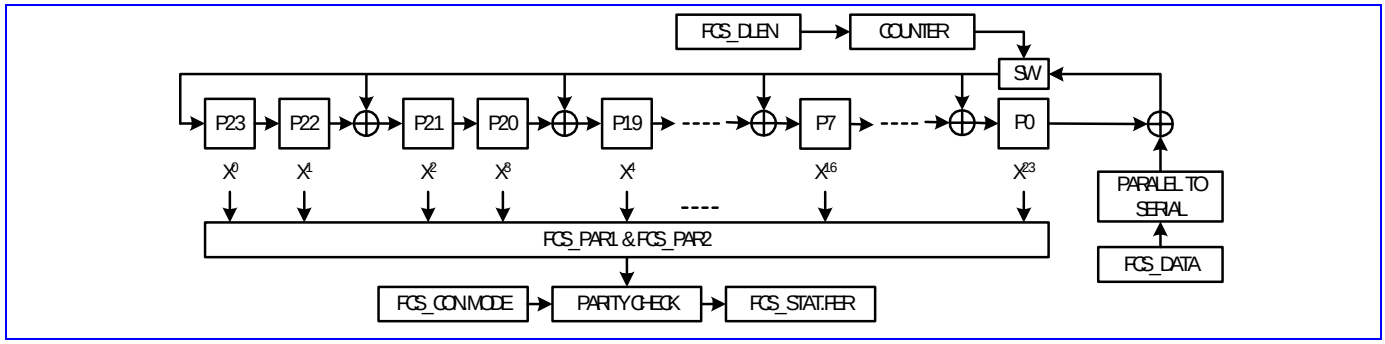


Figure 42 FCS codec circuit.

The codec is setup in the following sequence:

9. Reset FCS codec by set FCS_RST.RST = 0.

10. Write total data length of the block into FCS_DLEN.

11. Write FCS_DATA. The MCU then polls the FCS_STAT.BUSY flag. If BUSY = 0, the next data word can be written. This step is repeated until the last data word is sent.

12. When the process is finished, FCS_STAT.RDY is raised. For encode, the MCU reads FCS_PAR2 and FCS_PAR1 in order and further processing can go on. For decode, the MCU checks FCS_STAT.ERR to see if the data passed the parity check.

3.21.3.2 Interface

Group	Signal	I/O	Description
fcs	mclk_ck	I	Free running clock. Frequency same as AHB and APB bus clock
	bclk_ck	I	Core clock of modules connected to APB bus only with power down control
	paddr[15:0]	I	APB accessing address. For FCS codec, only paddr[4:0] are used.
	psel	I	PSEL signal on the APB bus.

	penable	I	PENABLE signal on the APB bus.
	prdata[15:0]	O	PRDATA of the APB bus.
	pwdata[15:0]	I	PWDATA of the APB bus.
	pwrite	I	APB write signal
RESET	preset_rstb	I	APB bus reset

3.22 EFUSE Controller (efusec)

3.22.1 General Description

There is 64-bit EFUSE macro in MT6223. EFUSE macro is a one-time-programming non-volatile memory. We usually use it as storage of sensitive and important data. Efuse controller delivers efuse status and re-initializes efuse macro.

3.22.2 Register Definitions

CONFG+F000h EFUSE control EFUSEC_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RD										SPD				BUSY	VLD
Type	WO										R/W				RO	RO
Reset	0										0				0	0

VLD Indicate if EFUSE data are valid or not. EFUSEC will initialize all EFUSE macros automatically. After finishing the initialization, this bit will change to 1 from 0. In other case, if you initialize EFUSE macros by write RD=1 manually, the VLD will go to low. After RD process done, VLD will go to high again.

BUSY EFUSE controller is busy. You can write EFUSEC control registers only when BUSY is low.

SPD System bus speed selection. Change this field depends on the reality.

00 System bus frequency is 13MHz

01 System bus frequency is 26MHz

10 System bus frequency is 39MHz

11 System bus frequency is 52MHz

RD Initialize EFUSE macros manually. The BUSY is 1 and VLD is 0 while EFUSEC re-initialize all EFUSE macros. After finishing the initialization, BUSY changes to 0 and VLD changes to 1.

4 Radio Interface Control

This chapter details the MT6223 interface control with the radio part of a GSM/GPRS terminal. Providing a comprehensive control scheme, the MT6223 radio interface consists of Baseband Serial Interface (BSI), Baseband Parallel Interface (BPI), Automatic Power Control (APC) and Automatic Frequency Control (AFC) together with APC-DAC and AFC-DAC.

4.1 Baseband Serial Interface

The Baseband Serial Interface controls external radio components. A 3-wire serial bus transfers data to RF circuitry for PLL frequency change, reception gain setting, and other radio control purposes. In this unit, BSI data registers are double-buffered in the same way as the TDMA event registers. The user writes data into the write buffer and the data is transferred from the write buffer to the active buffer when a TDMA_EVTVAL signal (from the TDMA timer) is pulsed.

Each data register BSI_D*n*_DAT is associated with one data control register BSI_D*n*_CON, where *n* denotes the index. Each data control register identifies which events (signaled by TDMA_BSISTR*n*, generated by the TDMA timer) trigger the download process of the word in register BSI_D*n*_DAT. The word and its length (in bits) is downloaded via the serial bus. A special event is triggered when the IMOD flag is set to 1: it provides immediate download process without software programming the TDMA timer.

If more than one data word is to be downloaded on the same BSI event, the word with the lowest address among them is downloaded first, followed by the next lowest and so on.

The total download time depends on the word length, the number of words to download, and the clock rates. The programmer must space the successive event to provide enough time. If the download process of the previous event is not complete before a new event arrives, the latter is suppressed.

The unit has four output pins: BSI_CLK is the output clock, BSI_DATA is the serial data port, and BSI_CS0 and BSI_CS1 are the select pins for 2 external components. BSI_CS1 is multiplexed with another function. Please refer to GPIO table for more detail.

In order to support bi-directional read and write operations of the RF chip, software can directly write values to BSI_CLK, BSI_DATA and BSI_CS by programming the BSI_DOUT register. Data from the RF chip can be read by software via the register BSI_DIN. If the RF chip interface is a 3-wire interface, then BSI_DATA is bi-directional. Before software can program the 3-wire behavior, the BSI_IO_CON register must be set. An additional signal path from GPIO accommodates RF chips with a 4-wire interface.

The block diagram of the BSI unit is as depicted in **Figure 43.**

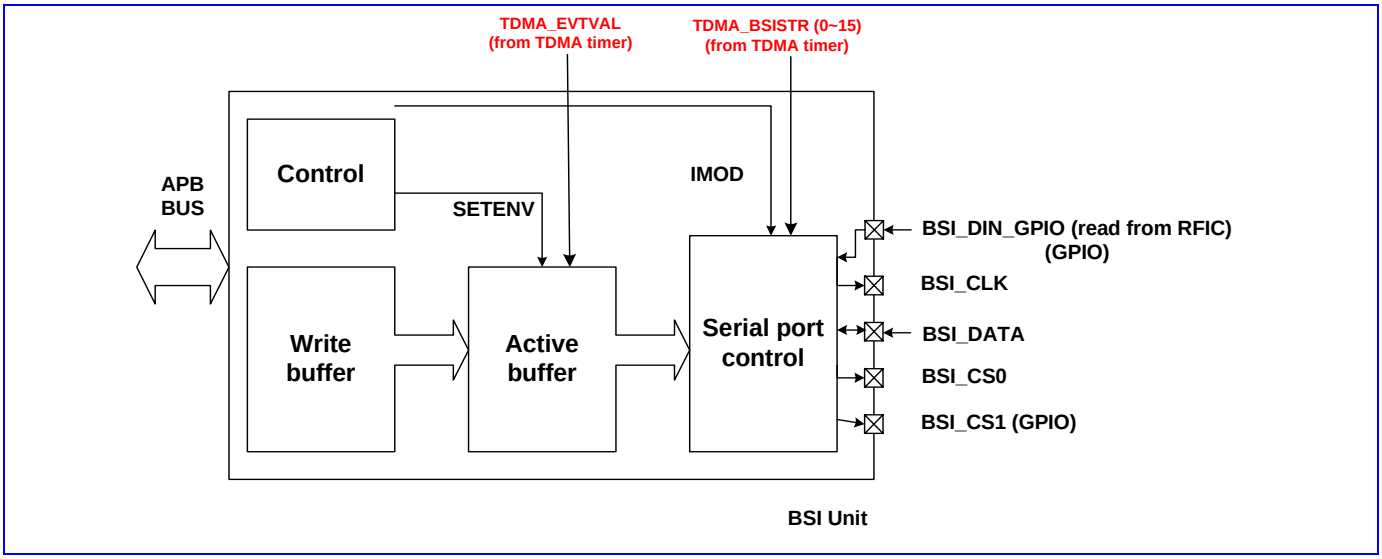


Figure 43 **Block diagram of BSI unit.**

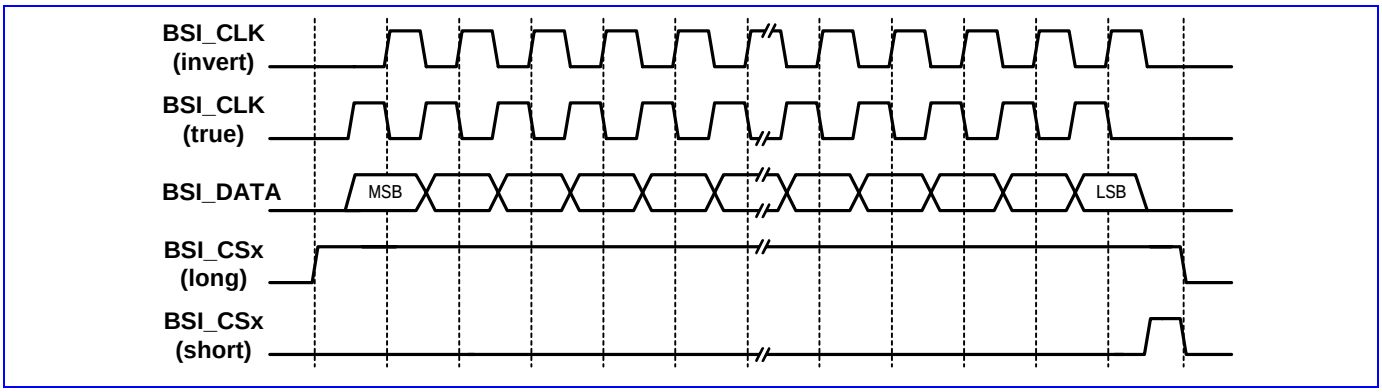


Figure 44 Timing characteristic of BSI interface.

4.1.1 Register Definitions

BSI+0000h BSI control register BSI_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								SETENV	EN1_POL	EN1_LEN	EN0_POL	EN0_LEN	IMOD	CLK_SPD		CLK_POL
Type								R/W	R/W	R/W	R/W	R/W	WO	R/W		R/W
Reset								0	0	0	0	0	N/A	0		0

This register is the control register for the BSI unit. The register controls the signal type of the 3-wire interface.

CLK_POL Controls the polarity of BSI_CLK. Refer to Figure 44.

0 True clock polarity

Inverted clock polarity

CLK_SPD Defines the clock rate of BSI_CLK. The 3-wire interface provides 4 choices of data bit rate. The default is 52/2 MHz.

00 52/2 MHz

01 52/4 MHz

10 52/6 MHz

11 52/8 MHz

IMOD Enables immediate mode. If the user writes 1 to the flag, the download is triggered immediately without waiting for the timer events. The words for which the register event ID equals 1Fh are downloaded following this signal. This flag is write-only. The immediate write is exercised only once: the programmer must write the flag again to invoke another immediate download. Setting the flag does not disable the other events from the timer; the programmer can disable all events by setting BSI_ENA to all zeros.

ENX_LEN Controls the type of signals BSI_CS0 and BSI_CS1. Refer to **Figure 43.**

0 Long enable pulse

Short enable pulse

ENX_POL Controls the polarity of signals BSI_CS0 and BSI_CS1.

0 True enable pulse polarity

1 Inverted enable pulse polarity

SETENV Enables the write operation of the active buffer.

0 The user writes to the write buffer. The data is then latched in the active buffer after TDMA_EVTVAL is pulsed.

1 The user writes data directly to the active buffer.

BSI+0004h Control part of data register 0 BSI_D0_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISB	LEN										EVT_ID				
Type	R/W	R/W										R/W				

This register is the control part of the data register 0. The register determines the required length of the download data word, the event to trigger the download process of the word, and the targeted device.

Table 30 lists the 44 data registers of this type. The max length of the first 40 data registers is 32 bits, and that of the last 4 data registers is 78 bits. Multiple data control registers may contain the same event ID. The data words of all registers with the same event ID are downloaded when the event occurs.

EVT_ID Stores the event ID for which the data word awaits to be downloaded.

00000~10011 Synchronous download of the word with the selected EVT_ID event. The relationship between this field and the event is listed as **Table 29.**

Event ID (in binary) – EVT_ID	Event name
00000	TDMA_BSISTR0

00001	TDMA_BSISTR1
00010	TDMA_BSISTR2
00011	TDMA_BSISTR3
00100	TDMA_BSISTR4
00101	TDMA_BSISTR5
00110	TDMA_BSISTR6
00111	TDMA_BSISTR7
01000	TDMA_BSISTR8
01001	TDMA_BSISTR9
01010	TDMA_BSISTR10
01011	TDMA_BSISTR11
01100	TDMA_BSISTR12
01101	TDMA_BSISTR13
01110	TDMA_BSISTR14
01111	TDMA_BSISTR15
10000	TDMA_BSISTR16
10001	TDMA_BSISTR17
10010	TDMA_BSISTR18
10011	TDMA_BSISTR19

Table 29 The relationship between the value of EVT_ID field in the BSI control registers and the TDMA_BSISTR events.

10100~11110 Reserved

11111 Immediate download

LEN The field stores the length of the data word. The actual length is defined as LEN + 1 in units of bits. For data registers 0~39, the value ranges from 0 to 31, corresponding to 1 to 32 bits in length. For data registers 40~43, the value ranges from 0 to 77, corresponding to 1 to 78 bits in length.

ISB The flag selects the target device.

0 Device 0 is selected.

Device 1 is selected.

BSI +0008h Data part of data register 0 BSI_D0_DAT

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DAT [31:16]															

Type	R/W															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAT [15:0]															
Type	R/W															

This register is the data part of the data register 0. The legal length of the data is up to 32 bits. The actual number of bits to be transmitted is specified in LEN field in the BSI_D0_CON register.

DAT The field signifies the data part of the data register.

Table 30 lists the address mapping and function of the 44 pairs of data registers.

Register Address	Register Function	Acronym
BSI +0004h	Control part of data register 0	BSI_D0_CON
BSI +0008h	Data part of data register 0	BSI_D0_DAT
BSI +000Ch	Control part of data register 1	BSI_D1_CON
BSI +0010h	Data part of data register 1	BSI_D1_ DAT
BSI +0014h	Control part of data register 2	BSI_D2_CON
BSI +0018h	Data part of data register 2	BSI_D2_ DAT
BSI +001Ch	Control part of data register 3	BSI_D3_CON
BSI +0020h	Data part of data register 3	BSI_D3_ DAT
BSI +0024h	Control part of data register 4	BSI_D4_CON
BSI +0028h	Data part of data register 4	BSI_D4_ DAT
BSI +002Ch	Control part of data register 5	BSI_D5_CON
BSI +0030h	Data part of data register 5	BSI_D5_ DAT
BSI +0034h	Control part of data register 6	BSI_D6_CON
BSI +0038h	Data part of data register 6	BSI_D6_ DAT
BSI +003Ch	Control part of data register 7	BSI_D7_CON
BSI +0040h	Data part of data register 7	BSI_D7_ DAT
BSI +0044h	Control part of data register 8	BSI_D8_CON
BSI +0048h	Data part of data register 8	BSI_D8_ DAT
BSI +004Ch	Control part of data register 9	BSI_D9_CON
BSI +0050h	Data part of data register 9	BSI_D9_ DAT
BSI +0054h	Control part of data register 10	BSI_D10_CON

BSI +0058h	Data part of data register 10	BSI_D10_ DATA
BSI +005Ch	Control part of data register 11	BSI_D11_CON
BSI +0060h	Data part of data register 11	BSI_D11_ DAT
BSI +0064h	Control part of data register 12	BSI_D12_CON
BSI +0068h	Data part of data register 12	BSI_D12_ DAT
BSI +006Ch	Control part of data register 13	BSI_D13_CON
BSI +0070h	Data part of data register 13	BSI_D13_ DAT
BSI +0074h	Control part of data register 14	BSI_D14_CON
BSI +0078h	Data part of data register 14	BSI_D14_ DAT
BSI +007Ch	Control part of data register 15	BSI_D15_CON
BSI +0080h	Data part of data register 15	BSI_D15_ DAT
BSI +0084h	Control part of data register 16	BSI_D16_CON
BSI +0088h	Data part of data register 16	BSI_D16_ DAT
BSI +008Ch	Control part of data register 17	BSI_D17_CON
BSI +0090h	Data part of data register 17	BSI_D17_ DAT
BSI +0094h	Control part of data register 18	BSI_D18_CON
BSI +0098h	Data part of data register 18	BSI_D18_ DAT
BSI +009Ch	Control part of data register 19	BSI_D19_CON
BSI +00A0h	Data part of data register 19	BSI_D19_ DAT
BSI +00A4h	Control part of data register 20	BSI_D20_CON
BSI +00A8h	Data part of data register 20	BSI_D20_ DAT
BSI +00ACh	Control part of data register 21	BSI_D21_CON
BSI +00B0h	Data part of data register 21	BSI_D21_ DAT
BSI +00B4h	Control part of data register 22	BSI_D22_CON
BSI +00B8h	Data part of data register 22	BSI_D22_ DAT
BSI +00BCh	Control part of data register 23	BSI_D23_CON
BSI +00C0h	Data part of data register 23	BSI_D23_ DAT
BSI +00C4h	Control part of data register 24	BSI_D24_CON
BSI +00C8h	Data part of data register 24	BSI_D24_ DAT

BSI +00CCh	Control part of data register 25	BSI_D25_CON
BSI +00D0h	Data part of data register 25	BSI_D25_ DAT
BSI +00D4h	Control part of data register 26	BSI_D26_CON
BSI +00D8h	Data part of data register 26	BSI_D26_ DAT
BSI +00DCh	Control part of data register 27	BSI_D27_CON
BSI +00E0h	Data part of data register 27	BSI_D27_ DAT
BSI +00E4h	Control part of data register 28	BSI_D28_CON
BSI +00E8h	Data part of data register 28	BSI_D28_ DAT
BSI +00ECh	Control part of data register 29	BSI_D29_CON
BSI +00F0h	Data part of data register 29	BSI_D29_ DAT
BSI +00F4h	Control part of data register 30	BSI_D30_CON
BSI +00F8h	Data part of data register 30	BSI_D30_ DAT
BSI +00FCh	Control part of data register 31	BSI_D31_CON
BSI +0100h	Data part of data register 31	BSI_D31_ DAT
BSI +0104h	Control part of data register 32	BSI_D32_CON
BSI +0108h	Data part of data register 32	BSI_D32_ DAT
BSI +010Ch	Control part of data register 33	BSI_D33_CON
BSI +0110h	Data part of data register 33	BSI_D33_ DAT
BSI +0114h	Control part of data register 34	BSI_D34_CON
BSI +0118h	Data part of data register 34	BSI_D34_ DAT
BSI +011Ch	Control part of data register 35	BSI_D35_CON
BSI +0120h	Data part of data register 35	BSI_D35_ DAT
BSI +0124h	Control part of data register 36	BSI_D36_CON
BSI +0128h	Data part of data register 36	BSI_D36_ DAT
BSI +012Ch	Control part of data register 37	BSI_D37_CON
BSI +0130h	Data part of data register 37	BSI_D37_ DAT
BSI +0134h	Control part of data register 38	BSI_D38_CON
BSI +0138h	Data part of data register 38	BSI_D38_ DAT
BSI +013Ch	Control part of data register 39	BSI_D39_CON

BSI +0140h	Data part of data register 39	BSI_D39_ DAT
BSI +0144h	Control part of data register 40	BSI_D40_CON
BSI +0148h	Data part of data register 40 (MSB 14 bits)	BSI_D40_ DAT2
BSI +014Ch	Data part of data register 40	BSI_D40_ DAT1
BSI +0150h	Data part of data register 40 (LSB 32 bits)	BSI_D40_ DAT0
BSI +0154h	Control part of data register 41	BSI_D41_CON
BSI +0158h	Data part of data register 41 (MSB 14 bits)	BSI_D41_ DAT2
BSI +015Ch	Data part of data register 41	BSI_D41_ DAT1
BSI +0160h	Data part of data register 41 (LSB 32 bits)	BSI_D41_ DAT0
BSI +0164h	Control part of data register 42	BSI_D42_CON
BSI +0168h	Data part of data register 42 (MSB 14 bits)	BSI_D42_ DAT2
BSI +016Ch	Data part of data register 42	BSI_D42_ DAT1
BSI +0170h	Data part of data register 42 (LSB 32 bits)	BSI_D42_ DAT0
BSI +0174h	Control part of data register 43	BSI_D43_CON
BSI +0178h	Data part of data register 43 (MSB 14 bits)	BSI_D43_ DAT2
BSI +017Ch	Data part of data register 43	BSI_D43_ DAT1
BSI +0180h	Data part of data register 43 (LSB 32 bits)	BSI_D43_ DAT0

Table 30 **BSI data registers**

BSI +0190h BSI event enable register BSI_ENA_0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI15	BSI14	BSI13	BSI12	BSI11	BSI10	BSI9	BSI8	BSI7	BSI6	BSI5	BSI4	BSI3	BSI2	BSI1	BSI0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

This register enables an event by setting the corresponding bit. After a hardware reset, all bits are initialized to 1. These bits are also set to 1 after TDMA_EVTVAL pulse.

BSIx Enables downloading of the words corresponding to the events signaled by TMDA_BSI.

0 The event is not enabled.

The event is enabled.

BSI +0194h BSI event enable register – MSB 4 bits BSI_ENA_1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BSI19	BSI18	BSI17	BSI16
Type													R/W	R/W	R/W	R/W
Reset													1	1	1	1

The register could enable the event by setting the corresponding bit. After hardware reset, all bits are initialized as 1. Besides, those bits are set as 1 after TDMA_EVTVAL is pulsed.

BSIx The flag enables the downloading of the words that corresponds to the events signaled by TMDA_BSI.

The event is not enabled.

The event is enabled.

BSI +0198h BSI IO mode control register BSI_IO_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SEL_CS1	4_WIRE	DAT_DIR	MODE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

MODE Defines the source of BSI signal.

BSI signal is generated by the hardware.

BSI signal is generated by the software. In this mode, the BSI clock depends on the value of the field DOUT.CLK. BSI_CS depends on the value of the field DOUT.CS and BSI_DATA depends on the value of the field DOUT.DATA.

DAT_DIR Defines the direction of BSI_DATA.

BSI _DATA is configured as input. The 3-wire interface is used and BSI_DATA is bi-directional.

BSI_DATA is configured as output.

4_WIRE Defines the BSI_DIN source.

The 3-wire interface is used and BSI_DATA is bi-directional. BSI_DIN comes from the same pin as BSI_DATA.

The 4-wire interface is used. Another pin (GPIO) is used as BSI_DIN.

SEL_CS1 Defines which of the BSI_CSx (BSI_CS0 or BSI_CS1) is written by the software.

BSI_CS0 is selected.

BSI_CS1 is selected.

BSI +019Ch Software-programmed data out BSI_DOUT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														DATA	CS	CLK
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	W	W	W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CLK Signifies the BSI_CLK signal.

CS Signifies the BSI_CS signal.

DATA Signifies the BSI_DATA signal.

BSI +01A0h Input data from RF chip BSI_DIN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DIN
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DIN Registers the input value of BSI_DATA from the RF chip.

BSI +01A4h BSI data pair number BSI_PAIR_NUM

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											PAIR_NUM					
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R					
Reset	0	0	0	0	0	0	0	0	0	0	28					

PAIR_NUM The software can program how many pairs of data register to be used. The default value is 28 pairs. This value must be smaller or equal to 44. The first 40 pairs are 32-bit long, and the last four pairs are 78-bit long.

4.2 Baseband Parallel Interface

4.2.1 General Description

The Baseband Parallel Interface features 10 control pins, which are used for timing-critical external circuits. These pins typically control front-end components which must be turned on or off at specific times during GSM operation, such as transmit-enable, band switching, TR-switch, etc.

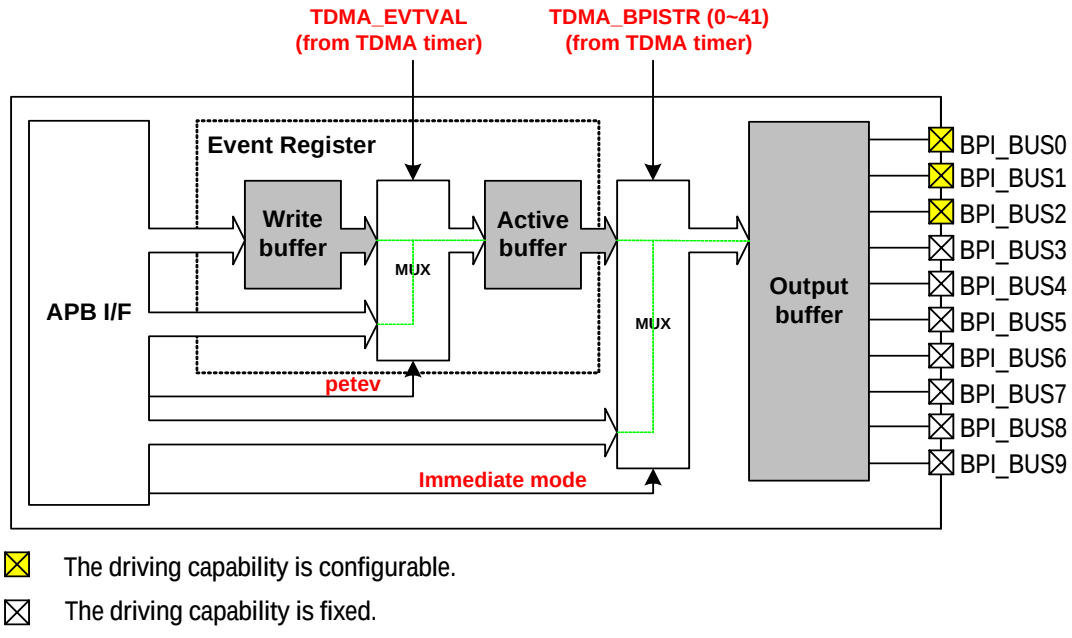


Figure 45 **Block diagram of BPI interface**

The user can program 42 sets of 10-bit registers to set the output value of BPI_BUS0~BPI_BUS9. The data is stored in the write buffers. The write buffers are then forwarded to the active buffers when the TDMA_EVTVAL signal is pulsed, usually once per frame. Each of the 42 write buffers corresponds to an active buffer, as well as to a TDMA event.

Each TDMA_BPISTR event triggers the transfer of data in the corresponding active buffer to the output buffer, thus changing the value of the BPI bus. The user can disable the events by programming the enable registers in the TDMA timer. If the TDMA_BPISTR event is disabled, the corresponding signal TDMA_BPISTR is not pulsed, and the value on the BPI bus remains unchanged.

For applications in which BPI signals serve as the switch, current-driving components are typically added to enhance driving capability. Three configurable output pins provide current up to 8 mA, and help reduce the number of external components. The output pins BPI_BUS6, BPI_BUS7, BPI_BUS8, and BPI_BUS9 are multiplexed with GPIO. Please refer to the GPIO table for more detailed information.

4.2.2 Register Definitions

BPI+0000h BPI control register BPI_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													PINM2	PINM1	PINM0	PETEV
Type													WO	WO	WO	R/W
Reset													0	0	0	0

This register is the control register of the BPI unit. The register controls the direct access mode of the active buffer and the current driving capability for the output pins.

The driving capabilities of BPI_BUS0, BPI_BUS1 and BPI_BUS2 can be 2 mA or 8 mA, determined by the value of PINM0, PINM1 and PINM2 respectively. These output pins provide a higher driving capability and save on external current-driving

components. In addition to the configurable pins, pins BPI_BUS3 to BPI_BUS9 provide a driving capability of 2 mA (fixed).

PETEV Enables direct access to the active buffer.

0 The user writes data to the write buffer. The data is latched in the active buffer after the TDMA_EVTVAL signal is pulsed.

The user directly writes data to the active buffer without waiting for the TDMA_EVTVAL signal.

PINM0 Controls the driving capability of BPI_BUS0.

0 The output driving capability is 2mA.

1 The output driving capability is 8mA.

PINM1 Controls the driving capability of BPI_BUS1.

0 The output driving capability is 2mA.

1 The output driving capability is 8mA.

PINM2 Controls the driving capability of BPI_BUS2.

0 The output driving capability is 2mA.

The output driving capability is 8mA.

BPI +0004h BPI data register 0 BPI_BUF0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							PO9	PO8	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This register defines the BPI signals that are associated with the event TDMA_BPI0.

Table 31 lists 42 registers of the same structure, each of which is associated with one specific event signal from the TDMA timer. The data registers are all double-buffered. When PETEV is set to 0, the data register links to the write buffer. When PETEV is set to 1, the data register links to the active buffer.

One register, BPI_BUFI, is dedicated for use in immediate mode. Writing a value to that register effects an immediate change in the corresponding BPI signal and bus.

POx This flag defines the corresponding signals for BPIx after the TDMA event 0 takes place.

The overall data register definition is listed in Table 31.

Register Address	Register Function	Acronym
BPI +0004h	BPI pin data for event TDMA_BPI 0	BPI_BUF0
BPI +0008h	BPI pin data for event TDMA_BPI 1	BPI_BUF1
BPI +000Ch	BPI pin data for event TDMA_BPI 2	BPI_BUF2
BPI +0010h	BPI pin data for event TDMA_BPI 3	BPI_BUF3

BPI +0014h	BPI pin data for event TDMA_BPI 4	BPI_BUF4
BPI +0018h	BPI pin data for event TDMA_BPI 5	BPI_BUF5
BPI +001Ch	BPI pin data for event TDMA_BPI 6	BPI_BUF6
BPI +0020h	BPI pin data for event TDMA_BPI 7	BPI_BUF7
BPI +0024h	BPI pin data for event TDMA_BPI 8	BPI_BUF8
BPI +0028h	BPI pin data for event TDMA_BPI 9	BPI_BUF9
BPI +002Ch	BPI pin data for event TDMA_BPI 10	BPI_BUF10
BPI +0030h	BPI pin data for event TDMA_BPI 11	BPI_BUF11
BPI +0034h	BPI pin data for event TDMA_BPI 12	BPI_BUF12
BPI +0038h	BPI pin data for event TDMA_BPI 13	BPI_BUF13
BPI +003Ch	BPI pin data for event TDMA_BPI 14	BPI_BUF14
BPI +0040h	BPI pin data for event TDMA_BPI 15	BPI_BUF15
BPI +0044h	BPI pin data for event TDMA_BPI 16	BPI_BUF16
BPI +0048h	BPI pin data for event TDMA_BPI 17	BPI_BUF17
BPI +004Ch	BPI pin data for event TDMA_BPI 18	BPI_BUF18
BPI +0050h	BPI pin data for event TDMA_BPI 19	BPI_BUF19
BPI +0054h	BPI pin data for event TDMA_BPI 20	BPI_BUF20
BPI +0058h	BPI pin data for event TDMA_BPI 21	BPI_BUF21
BPI +005Ch	BPI pin data for event TDMA_BPI 22	BPI_BUF22
BPI +0060h	BPI pin data for event TDMA_BPI 23	BPI_BUF23
BPI +0064h	BPI pin data for event TDMA_BPI 24	BPI_BUF24
BPI +0068h	BPI pin data for event TDMA_BPI 25	BPI_BUF25
BPI +006Ch	BPI pin data for event TDMA_BPI 26	BPI_BUF26
BPI +0070h	BPI pin data for event TDMA_BPI 27	BPI_BUF27
BPI +0074h	BPI pin data for event TDMA_BPI 28	BPI_BUF28
BPI +0078h	BPI pin data for event TDMA_BPI 29	BPI_BUF29
BPI +007Ch	BPI pin data for event TDMA_BPI 30	BPI_BUF30
BPI +0080h	BPI pin data for event TDMA_BPI 31	BPI_BUF31
BPI +0084h	BPI pin data for event TDMA_BPI 32	BPI_BUF32

BPI +0088h	BPI pin data for event TDMA_BPI 33	BPI_BUF33
BPI +008Ch	BPI pin data for event TDMA_BPI 34	BPI_BUF34
BPI +0090h	BPI pin data for event TDMA_BPI 35	BPI_BUF35
BPI +0094h	BPI pin data for event TDMA_BPI 36	BPI_BUF36
BPI +0098h	BPI pin data for event TDMA_BPI 37	BPI_BUF37
BPI +009Ch	BPI pin data for event TDMA_BPI 38	BPI_BUF38
BPI +00A0h	BPI pin data for event TDMA_BPI 39	BPI_BUF39
BPI +00A4h	BPI pin data for event TDMA_BPI 40	BPI_BUF40
BPI +00A8h	BPI pin data for event TDMA_BPI 41	BPI_BUF41
BPI +00ACh	BPI pin data for immediate mode	BPI_BUFI

Table 31 **BPI Data Registers.**

BPI +00B0h BPI event enable register 0 BPI_ENA0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BEN15	BEN14	BEN13	BEN12	BEN11	BEN10	BEN9	BEN8	BEN7	BEN6	BEN5	BEN4	BEN3	BEN2	BEN1	BEN0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

This register enables the events that are signaled by the TDMA timer: by clearing a register bit, the corresponding event signal is ignored. After a hardware reset, all the enable bits default to 1 (enabled). Upon receiving a TDMA_EVTVAL pulse, all register bits are also set to 1 (enabled).

BENn This flag indicates whether event n signals are heeded or ignored.

0 Event n is disabled (ignored).

1 Event n is enabled.

BPI+00B4h BPI event enable register 1 BPI_ENA1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BEN31	BEN30	BEN29	BEN28	BEN27	BEN26	BEN25	BEN24	BEN23	BEN22	BEN21	BEN20	BEN19	BEN18	BEN17	BEN16
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register enables the events that are signaled by the TDMA timing generator: by clearing a register bit, the corresponding event signal is ignored. After a hardware reset, all the enable bits default to 1 (enabled). Upon receiving the TDMA_EVTVAL pulse, all register bits are also set to 1 (enabled).

BENn This flag indicates whether event n signals are heeded or ignored.

0 Event n is disabled (ignored).

1 Event n is enabled.

BPI+00B8h BPI event enable register 2 BPI_ENA2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							BEN41	BEN40	BEN39	BEN38	BEN37	BEN36	BEN35	BEN34	BEN33	BEN32
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset							0	0	0	0	0	0	0	0	0	0

The register is used to enable the events that are signaled by the TDMA timing generator. After hardware reset, all the enable bits defaults to be 1 (enabled). Upon receiving the TDMA_EVTVAL pulse, those bits are also set to 1 (enabled).

BENn The flag controls the function of event n.

The event n is disabled.

The event n is enabled.

4.3 Automatic Power Control (APC) Unit

4.3.1 General Description

The Automatic Power Control (APC) unit controls the Power Amplifier (PA) module. Through APC unit, the proper transmit power level of the handset can be set to ensure that burst power ramping requirements are met. In one TDMA frame, up to 7 TDMA events can be enabled to support multi-slot transmission. In practice, 5 banks of ramp profiles are used in one frame to make up 4 consecutive transmission slots.

The shape and magnitude of the ramp profiles are configurable to fit ramp-up (ramp up from zero), intermediate ramp (ramp between transmission windows), and ramp-down (ramp down to zero) profiles. Each bank of the ramp profile consists of 16 8-bit unsigned values, which are adjustable for different conditions.

The entries from one bank of the ramp profile are partitioned into two parts, with 8 values in each half. In normal operation, the entries in the left half are multiplied by a 10-bit left scaling factor, and the entries in the right half are multiplied by a 10-bit right scaling factor. The values are then truncated to form 16 10-bit intermediate values. Finally the intermediate ramp profile are linearly interpolated into 32 10-bit values and sequentially used to update the D/A converter. The block diagram of the APC unit is shown in **Figure 46 .**

The APB bus interface is 32 bits wide. Four write accesses are required to program each bank of ramp profile. The detailed register allocations are listed in **Table 32.**

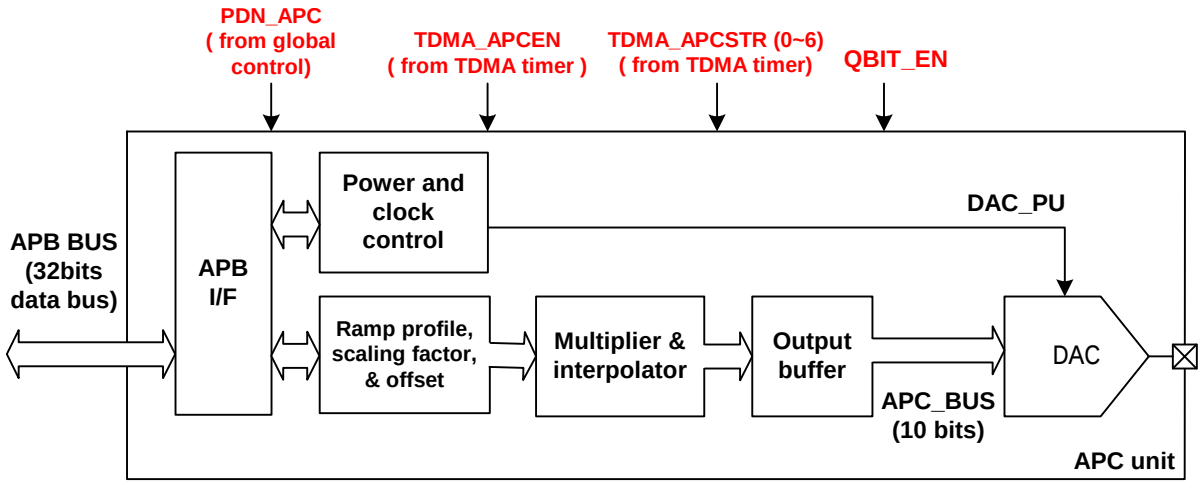


Figure 46 **Block diagram of APC unit.**

4.3.2 Register Definitions

APC+0000h APC 1st ramp profile #0 APC_PFA0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENT3								ENT2							
Type	R/W								R/W							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENT1								ENT0							
Type	R/W								R/W							

The register stores the first four entries of the first power ramp profile. The first entry resides in the least significant byte [7:0], the second entry in the second byte [15:8], the third entry in the third byte [23:16], and the fourth in the most significant byte [31:24]. Since this register provides no hardware reset, the programmer must configure it before any APC event takes place.

ENT3 The field signifies the 4th entry of the 1st ramp profile.

ENT2 The field signifies the 3rd entry of the 1st ramp profile.

ENT1 The field signifies the 2nd entry of the 1st ramp profile.

ENT0 The field signifies the 1st entry of the 1st ramp profile.

The overall ramp profile register definition is listed in **Table 32.**

Register Address	Register Function	Acronym
APC +0000h	APC 1st ramp profile #0	APC_PFA0
APC +0004h	APC 1st ramp profile #1	APC_PFA1
APC +0008h	APC 1st ramp profile #2	APC_PFA2
APC +000Ch	APC 1st ramp profile #3	APC_PFA3

APC +0020h	APC 2nd ramp profile #0	APC_PFB0
APC +0024h	APC 2nd ramp profile #1	APC_PFB1
APC +0028h	APC 2nd ramp profile #2	APC_PFB2
APC +002Ch	APC 2nd ramp profile #3	APC_PFB3
APC +0040h	APC 3rd ramp profile #0	APC_PFC0
APC +0044h	APC 3rd ramp profile #1	APC_PFC1
APC +0048h	APC 3rd ramp profile #2	APC_PFC2
APC +004Ch	APC 3rd ramp profile #3	APC_PFC3
APC +0060h	APC 4th ramp profile #0	APC_PFD0
APC +0064h	APC 4th ramp profile #1	APC_PFD1
APC +0068h	APC 4th ramp profile #2	APC_PFD2
APC +006Ch	APC 4th ramp profile #3	APC_PFD3
APC +0080h	APC 5th ramp profile #0	APC_PFE0
APC +0084h	APC 5th ramp profile #1	APC_PFE1
APC +0088h	APC 5th ramp profile #2	APC_PFE2
APC +008Ch	APC 5th ramp profile #3	APC_PFE3
APC +00A0h	APC 6th ramp profile #0	APC_PFF0
APC +00A4h	APC 6th ramp profile #1	APC_PFF1
APC +00A8h	APC 6th ramp profile #2	APC_PFF2
APC +00ACh	APC 6th ramp profile #3	APC_PFF3
APC +00C0h	APC 7th ramp profile #0	APC_PFG0
APC +00C4h	APC 7th ramp profile #1	APC_PFG1
APC +00C8h	APC 7th ramp profile #2	APC_PFG2
APC +00CCh	APC 7th ramp profile #3	APC_PFG3

Table 32 **APC ramp profile registers**

APC +0010h APC 1st ramp profile left scaling factor APC_SCAL0L

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SF									
Type							R/W									
Reset							1_0000_0000									

The register stores the left scaling factor of the 1st ramp profile. This factor multiplies the first 8 entries of the 1st ramp profile to provide the scaled profile, which is then interpolated to control the D/A converter.

After a hardware reset, the initial value of the register is 256. In this case, no scaling is done (each entry of the ramp profile is multiplied by 1), because the 8 least significant bits are truncated after multiplication.

The overall scaling factor register definition is listed in **Table 33 .**

SF Scaling factor. After a hardware reset, the value is 256.

APC +0014h APC 1st ramp profile right scaling factor APC_SCAL0R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SF									
Type							R/W									
Reset							1_0000_0000									

The register stores the right scaling factor of the 1st ramp profile. This factor multiplies the last 8 entries of the 1st ramp profile to provide the scaled profile, which is then interpolated to control the D/A converter.

After a hardware reset, the initial value of the register is 256. In this case, no scaling is done (each entry of the ramp profile is multiplied by 1), because the 8 least significant bits are truncated after multiplication.

The overall scaling factor register definition is listed in **Table 33 .**

SF Scaling factor. After a hardware reset, the value is 256.

APC+0018h APC 1st ramp profile offset value APC_OFFSET0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							OFFSET									
Type							R/W									
Reset							0									

There are 7 offset values for the corresponding ramp profile.

The 1st offset value also serves as the pedestal value. The value is used to power up the APC D/A converter before the RF signals start to transmit. The D/A converter is then biased on the value, to provide the initial control voltage for the external control loop. The exact value depends on the characteristics of the external components. The timing to output the pedestal value is configurable through the TDMA_BULCON2 register of the timing generator; its valid range is 0~127 quarter-bits of time after the baseband D/A converter is powered up.

OFFSET Offset value for the corresponding ramp profile. After a hardware reset, the default value is 0.

The overall offset register definition is listed in Table 33**.**

Register Address	Register Function	Acronym
APC +0010h	APC 1st ramp profile left scaling factor	APC_SCAL0L

APC +0014h	APC 1st ramp profile right scaling factor	APC_SCAL0R
APC +0018h	APC 1st ramp profile offset value	APC_OFFSET0
APC +0030h	APC 2nd ramp profile left scaling factor	APC_SCAL1L
APC +0034h	APC 2nd ramp profile right scaling factor	APC_SCAL1R
APC +0038h	APC 2nd ramp profile offset value	APC_OFFSET1
APC +0050h	APC 3rd ramp profile left scaling factor	APC_SCAL2L
APC +0054h	APC 3rd ramp profile right scaling factor	APC_SCAL2R
APC +0058h	APC 3rd ramp profile offset value	APC_OFFSET2
APC +0070h	APC 4th ramp profile left scaling factor	APC_SCAL3L
APC +0074h	APC 4th ramp profile right scaling factor	APC_SCAL3R
APC +0078h	APC 4th ramp profile offset value	APC_OFFSET3
APC +0090h	APC 5th ramp profile left scaling factor	APC_SCAL4L
APC +0094h	APC 5th ramp profile right scaling factor	APC_SCAL4R
APC +0098h	APC 5th ramp profile offset value	APC_OFFSET4
APC +00B0h	APC 6th ramp profile left scaling factor	APC_SCAL5L
APC +00B4h	APC 6th ramp profile right scaling factor	APC_SCAL5R
APC +00B8h	APC 6th ramp profile offset value	APC_OFFSET5
APC +00D0h	APC 7th ramp profile left scaling factor	APC_SCAL6L
APC +00D4h	APC 7th ramp profile right scaling factor	APC_SCAL6R
APC +00D8h	APC 7th ramp profile offset value	APC_OFFSET6

Table 33 APC scaling factor and offset value registers

APC+00E0h APC control register APC_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															GSM	FPU
Type															R/W	R/W
Reset															1	0

GSM Defines the operation mode of the APC module. In GSM mode, each frame has only one slot, thus only one scaling factor and one offset value must be configured. If the GSM bit is set, the programmer needs only to configure APC_SCAL0L and APC_OFFSET0. If the bit is not set, the APC module is operating in GPRS mode.

0 The APC module is operating in GPRS mode.

1 The APC module is operating in GSM mode. Default value.

FPU Forces the APC D/A converter to power up. Test only.

0 The APC D/A converter is not forced to power up. The converter is only powered on when the transmission window is opened. Default value.

1 The APC D/A converter is forced to power up.

4.3.3 Ramp Profile Programming

The first value of the first normalized ramp profile must be written in the least significant byte of the APC_PFA0 register. The second value must be written in the second least significant byte of the APC_PFA0, and so on.

Each ramp profile can be programmed to form an arbitrary shape.

The start of ramping is triggered by one of the TDMA_APCSTR signals. The timing relationship between TDMA_APCSTR and TDMA slots is depicted in **Figure 47** 錯誤! 找不到參照來源。 for 4 consecutive time slots case. The power ramping profile must comply with the timing mask defined in GSM SPEC 05.05. The timing offset values for 7 ramp profiles are stored in the TDMA timer register from TDMA_APC0 to TDMA_APC6.

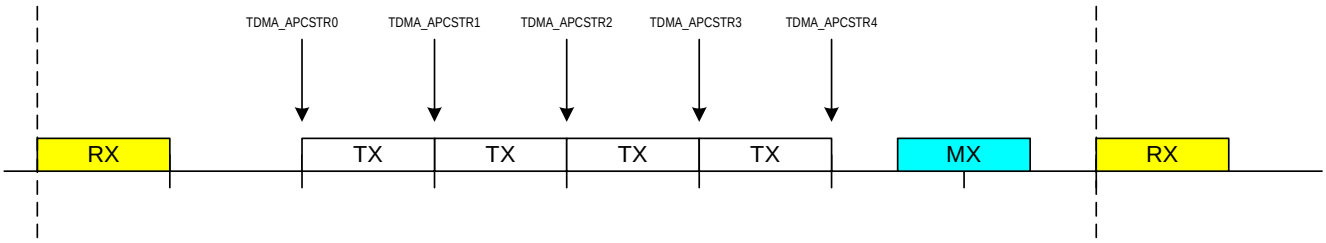


Figure 47 **Timing diagram of TDMA_APCSTR.**

Because the APC unit provides more than 5 ramp profiles, up to 4 consecutive transmission slots can accommodated. The 2 additional ramp profiles are useful particularly when the timing between the last 2 transmission time slots and CTIRQ is uncertain; software can begin writing the ramp profiles for the succeeding frame during the current frame, alleviating the risk of not writing the succeeding frame's profile data in time.

In GPRS mode, to fit the intermediate ramp profile between different power levels, a simple scaling scheme is used to synthesize the ramp profile. The equation is as follows:

$$DA_0 = OFF + S_0 \cdot \frac{DN_{15,pre} + DN_0}{2}$$

$$DA_{2k} = OFF + S_l \cdot \frac{DN_{k-1} + DN_k}{2}, k = 1,...,15$$

$$DA_{2k+1} = OFF + S_l \cdot DN_k, k = 0,1,...,15$$

$$l = \begin{cases} 0, & \text{if } 8 > k \geq 0 \\ 1, & \text{if } 15 \geq k \geq 8 \end{cases}$$

where **DA** = the data to present to the D/A converter,
DN = the normalized data which is stored in the register **APC_PF*n***,
S_0 = the left scaling factor stored in register **APC_SCAL*nL***,
S_1 = the right scaling factor stored in register **APC_SCAL*nR***, and
OFF = the offset value stored in the register **APC_OFFSET*n***.

The subscript ***n*** denotes the index of the ramp profile.

The ramp calculation before interpolation is as depicted in Figure 48 錯誤! 找不到參照來源。.

During each ramp process, each word of the normalized profile is first multiplied by 10-bit scaling factors and added to an offset value to form a bank of 18-bit words. The first 8 words (in the left half part as in **Figure 48** 錯誤! 找不到參照來源。) are multiplied by the left scaling factor $\mathbf{S_0}$ and the last 8 words (in the right half part as in **Figure 48** 錯誤! 找不到參照來源。) are multiplied by the right scaling factor $\mathbf{S_1}$. The lowest 8 bits of each word are then truncated to get a 10-bit result. The scaling factor is 0x100, which represents no scaling on reset. A value smaller than 0x100 scales the ramp profile down, and a value larger than 100 scales the ramp profile up.

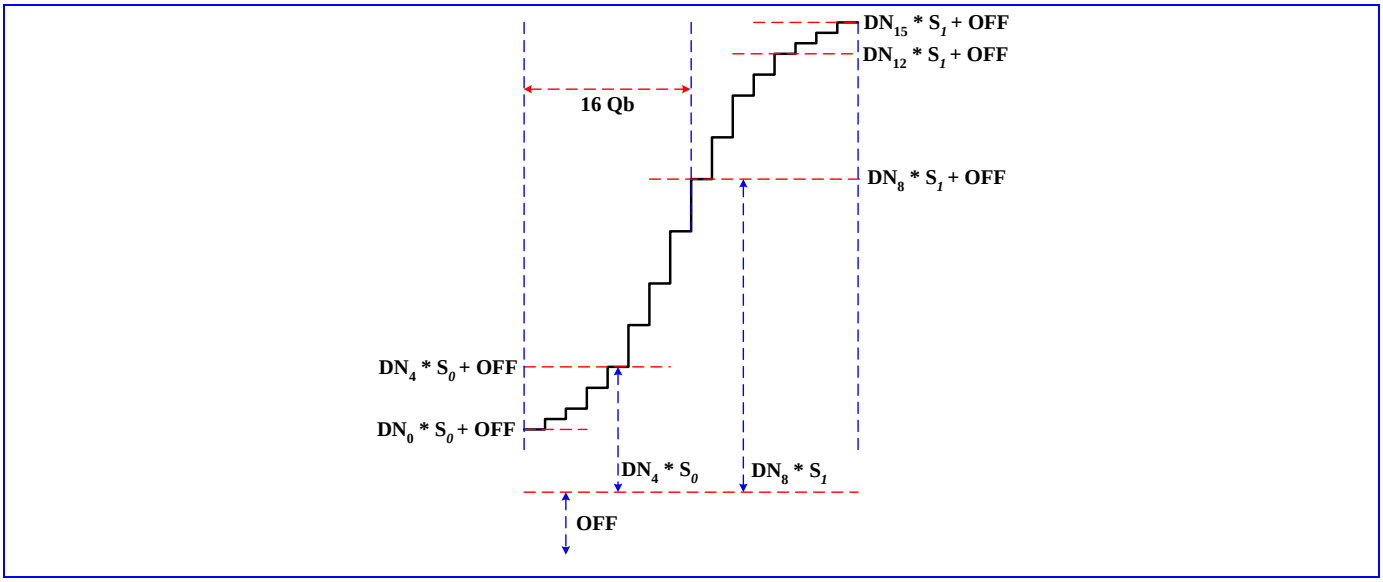


Figure 48 **The timing diagram of the APC ramp.**

The 16 10-bit words are linearly interpolated into 32 10-bit words. A 10-bit D/A converter is then used to convert these 32 ramp values at a rate of 1.0833 MHz, that is, at quarter-bit rate. The timing diagram is shown in **Figure 49 錯誤! 找不到參照來源。** and the final value is retained on the output until the next event occurs.

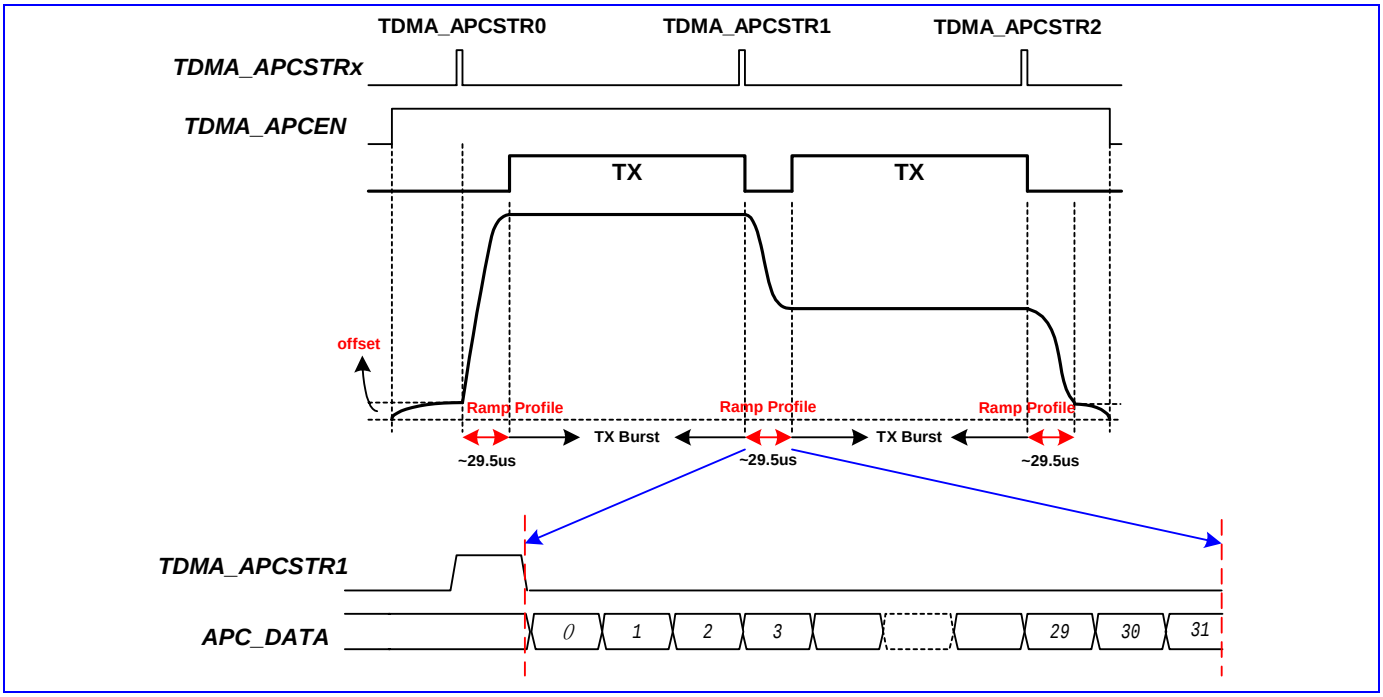


Figure 49 **Timing diagram of the APC ramping.**

The APC unit is only powered up when the APC window is open. The APC window is controlled by configuring the TDMA registers TDMA_BULCON1 and TDMA_BULCON2. Please refer to the TDMA timer unit for more detailed information.

The first offset value stored in the register APC_OFFSET0 also serves as the pedestal value, which is used to provide the initial power level for the PA.

Since the profile is not double-buffered, the timing to write the ramping profile is critical. The programmer must be restricted from writing to the data buffer during the ramping process, otherwise the ramp profile may be incorrect and lead to a malfunction.

4.4 Automatic Frequency Control (AFC) Unit

4.4.1 General description

The Automatic Frequency Control (AFC) unit provides the direct control of the oscillator for frequency offset and Doppler shift compensation. The block diagram is of the AFC unit depicted in **Figure 50.** The module utilizes a 13-bit D/A converter to achieve high-resolution control. Two modes of operation provide flexibility when controlling the oscillator; they are described as follows.

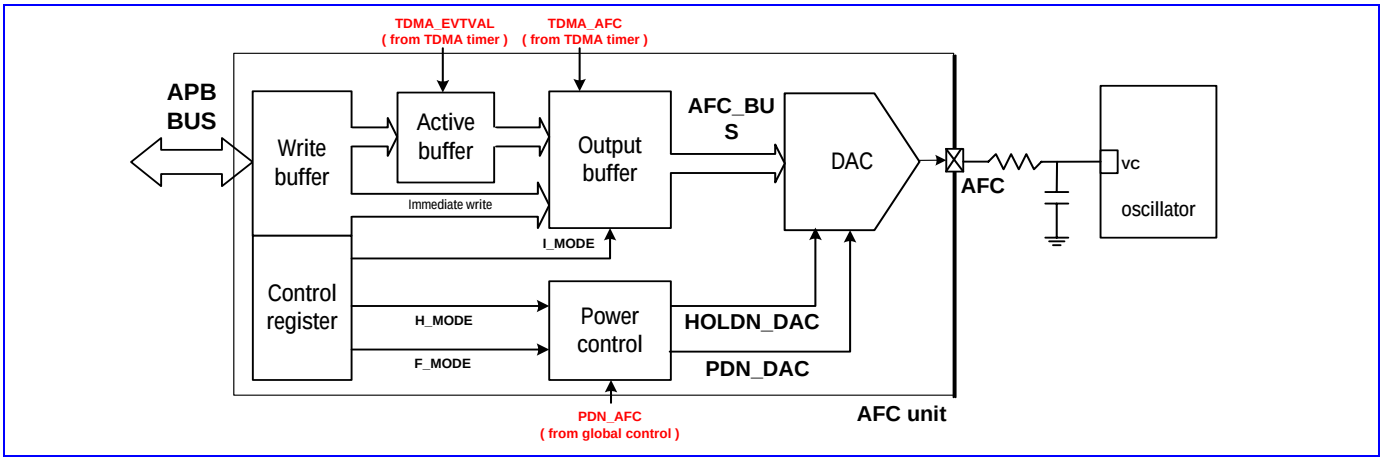


Figure 50 **The block diagram of the AFC controller**

In timer-triggered mode, the TDMA timer controls the AFC enabling events. Each TDMA frame can pulse at most four events. Double buffer architecture is supported. AFC values can be written to the write buffers. When the signal TDMA_EVTVAL is received, the values in the write buffers are latched into the active buffers. However, AFC values can also be written to the active buffers directly. Each event is associated with an active buffer sharing the same index. When a TDMA event is triggered by TDMA_AFC, the value in the corresponding active buffer takes effect. **Figure 51** shows a timing diagram of AFC events with respect to TX/RX/MX windows. In this mode, the D/A converter can stay powered on or be powered on for a programmable duration (256 quarter-bits, by default). The latter option is for power saving.

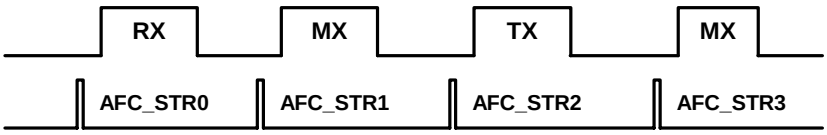


Figure 51 **Timing Diagram for the AFC Controller**

In immediate mode, the MCU can directly control the AFC value without event-triggering. The value written by the MCU takes effect immediately. In this mode, the D/A converter must be powered on continuously. When transitioning from immediate mode into timer-triggered mode (by setting flag I_MODE in the register AFC_CON to be 0), the D/A converter is kept powered on for a programmable duration (256 quarter-bits by default) if a TDMA_AFC is not been pulsed. The duration is prolonged upon receiving events.

In order to support Wifi & BlueTooth, SRCLKENAi will turn on AFC DAC and the output voltage is the previous value if AFC does not enter the hold mode.

4.4.2 Register Definitions

AFC+0000h AFC control register AFC_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ALY_ON	H_MODE	RDACT	F_MODE	FETENV	I_MODE
Type											R/W	R/W	R/W	R/W	R/W	R/W
Reset											0	0	0	0	0	0

Four control modes are defined and can be controlled through the AFC control register. F_MODE enables the force power up mode. FETENV enables the direct write operation to the active buffer. I_MODE enables the immediate mode. RDACT enables the direct read operation from the active buffer. HOLD_ON enables the AFC DAC hold mode.

RDACT The flag enables the direct read operation from the active buffer. Note the control flag is only applicable to the four data buffer including AFC_DAT0, AFC_DAT1, AFC_DAT2, and AFC_DAT3.

0 APB read from the write buffer.

1 APB read from the active buffer.

FETENV The flag enables the direct write operation to the active buffer. Note the control flag is only applicable to the for data buffer including AFC_DAT0, AFC_DAT1, AFC_DAT2, and AFC_DAT3.

0 APB write to the write buffer.

1 APB write to the active buffer.

F_MODE The flag enables the force power up mode.

0 The force power up mode is not enabled.

1 The force power up mode is enabled.

I_MODE The flag enables the immediate mode. To enable the immediate mode also enable the force power up mode.

0 The immediate mode is not enabled.

1 The immediate mode is enabled.

H_MODE The flag enables the hold mode of AFC DAC. If this mode is enabled, the DAC will keep the previous voltage level instead of power down.

0 The hold mode is not enabled.

1 The hold mode is enabled.

ALY_ON Force AFC DAC power on regardless of PDN_CONx setting in software power down control

0 Normal power down procedure of PDN_CONx

1 Force AFC DAC to keep power up state

AFC +0004h AFC data register 0 AFC_DAT0

Bit	15	14	13	12	11	10	9	8	7	6	15	4	3	2	1	0
Name				AFCD												
Type				R/W												

The register stores the AFC value for the event 0 triggered by the TDMA timer in timer-triggered mode. When the RDACT or FETENV bit (of the AFC_CON register) is set, the data transfer operates on the active buffer. When neither flag is set, the data transfer operates on the write buffer.

AFCD The AFC sample for the D/A converter.

Four registers (AFC_DAT0, AFC_DAT1, AFC_DAT2, AFC_DAT3) of the same type correspond to the event triggered by the

TDMA timer. The four registers are summarized in **Table 1**.

Register Address	Register Function	Acronym
AFC +0004h	AFC control value 0	AFC_DAT0
AFC +0008h	AFC control value 1	AFC_DAT1
AFC +000Ch	AFC control value 2	AFC_DAT2
AFC +0010h	AFC control value 3	AFC_DAT3

Table 1 **AFC Data Registers**

Immediate mode can only use AFC_DAT0. In this mode, only the control value in the AFC_DAT0 write buffer is used to control the D/A converter. Unlike timer-triggered mode, the control value in AFC_DAT0 write buffer can bypass the active buffer stage and be directly coupled to the output buffer in immediate mode. To use immediate mode, program the AFC_DAT0 in advance and then enable immediate mode by setting the I_MODE flag in the AFC_CON register.

The registers AFC_DATA0, AFC_DAT1, AFC_DAT2, and AFC_DAT3 have no initial values, thus the register must be programmed before any AFC event takes place. The AFC value for the D/A converter, i.e., the output buffer value, is initially 0 after power up before any event occurs.

AFC +0014h AFC power up period AFC_PUPER

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PU_PER												
Type				R/W												
Reset				ff												

This register stores the AFC power up period, which is 13 bits wide. The value ranges from 0 to 8191. If the I_MODE or F_MODE flag is set, this register has no effect since the D/A converter is powered up continuously. If neither flag is set, the register controls the power up duration of the D/A converter. During that period, the signal PDN_DAC in **Figure 50** is set to 1(power up).

PU_PER Stores the AFC power up period. After hardware power up, the field is initialized to 255.

5 Baseband Front End

Baseband Front End is a modem interface between TX/RX mixed-signal modules and digital signal processor (DSP). We can divide this block into two parts (see **Figure 52** Block Diagram of Baseband Front End). The first is the uplink (transmitting) path, which converts bit-stream from DSP into digital in-phase (I) and quadrature (Q) signals for TX mixed-signal module. The second part is the downlink (receiving) path, which receives digital in-phase (I) and quadrature (Q) signals from RX mixed-signal module, performs FIR filtering and then sends results to DSP. **Figure 52** Block Diagram of Baseband Front End illustrates interconnection around Baseband Front End. In the figure the shadowed blocks compose Baseband Front End.

The uplink path is mainly composed of GMSK Modulator and uplink parts of Baseband Serial Ports, and the downlink path is mainly composed of RX digital FIR filter, RX interference detection filter (ITD) including power measurement blocks, downlink parts of Baseband Serial Ports and DSP I/O. Baseband Serial Ports is a serial interface used to communicate with DSP. In addition, there is a set of control registers in Baseband Front End that is intended for control of TX/RX mixed-signal modules, inclusive of several compensation circuit: calibration of I/Q DC offset, I/Q Quadrature Phase Compensation and I/Q Gain Mismatch of uplink analog-to-digital (D/A) converters as well as I/Q Gain Mismatch for downlink digital-to-analog (A/D) converters in TX/RX mixed-signal modules. The timing of bit streaming through Baseband Front End is completely under control of TDMA timer. Usually only either of uplink and downlink paths is active at one moment. However, both of the uplink and downlink paths will be active simultaneously when Baseband Front End is in loopback mode.

When either of TX windows in TDMA timer is opened, the uplink path in Baseband Front End will be activated. Accordingly components on the uplink path such as GMSK Modulator will be powered on, and then TX mixed-signal module is also powered on. The sub-block Baseband Serial Ports will sink TX data bits from DSP and then forward them to GMSK Modulator. The outputs from GMSK Modulator are sent to TX mixed-signal module in format of I/Q signals. Finally D/A conversions are performed in TX mixed-signal module and the output analog signal is output to RF module.

Similarly, while either of RX windows in TDMA timer is opened, the downlink path in Baseband Front End will be activated. Accordingly components on the downlink path such as RX mixed-signal module and RX digital FIR filter are then powered on. First A/D conversions are performed in RX mixed-signal module, and then the results in format of I/Q signals are sourced to Low Pass Filtering with different bandwidth (Narrow one about F_C = 90 kHz, Wide one about F_C = 110khz), Interference Detection Circuit to determine which Filter to be used by judging receiving power on current burst. Additionally, “I/Q Compensation Circuit” is an option in data path for modifying Receiving I/Q pair gain mismatch. Finally the results will be sourced to DSP through Baseband Serial Ports.

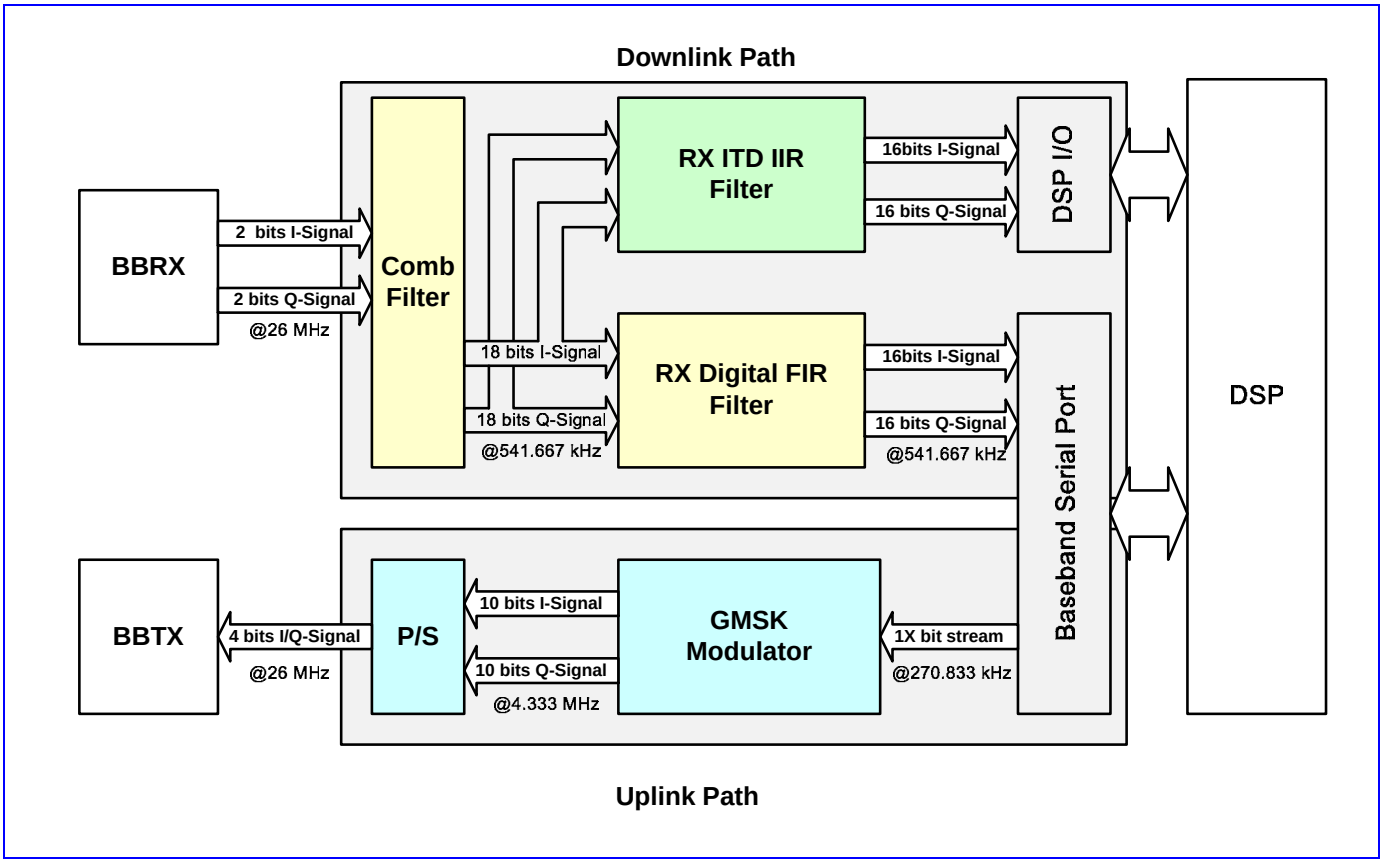


Figure 52 Block Diagram of Baseband Front End

5.1 Baseband Serial Ports

5.1.1 General Description

Baseband Front End communicates with DSP through the sub block of Baseband Serial Ports. Baseband Serial Ports interfaces with DSP in serial manner. This implies that DSP must be configured carefully in order to have Baseband Serial Ports cooperate with DSP core correctly.

If downlink path is programmed in bypass-filter mode (**NOT** bypass-filter loopback mode), behavior of Baseband Serial Ports will be completely be different from that in normal function mode. The special mode is for testing purpose. Please see the subsequent section of Downlink Path for more details.

TX and RX windows are under control of TDMA timer. Please refer to functional specification of TDMA timer for the details on how to open/close a TX/RX window. Opening/Closing of TX/RX windows have two major effects on Baseband Front End: power on/off of corresponding components and data souring/sinking. It is worth noticing that Baseband Serial Ports is only intended for sinking TX data from DSP or sourcing data to DSP. It does not involve power on/off of TX/RX mixed-signal modules.

As far as downlink path is concerned, if a RX window is opened by TDMA timer Baseband Front End will have RX mixed-signal module proceed to make A/D conversion, two parallel RX digital filter proceed to perform filtering and Baseband Serial Ports be activated to source data from RX digital filter to Master DSP while Power Measurement through DSP I/O to DSP no matter the data is meaningful or not. However, the interval between the moment that RX mixed-signal module is powered on and the moment that data proceed to be dumped by Baseband Serial Ports can be well controlled in TDMA timer. Let us denote RX enable window as the interval that RX mixed-signal module is powered on and denote RX dump window as the interval that data is dumped by Baseband Serial Ports. If the first samples from RX digital filter desire

to be discarded, the corresponding RX enable window must cover the corresponding RX dump window. Note that RX dump windows always win over RX enable windows. It means that a RX dump window will always raise a RX enable window. RX enable windows can be raised by TDMA timer or by programming RX power-down bit in global control registers to be '0'. This is useful in debugging environment.

Similarly, a TX dump window refers to the interval that Baseband Serial Ports sinks data from DSP on uplink path and a TX enable window refers to the interval that TX mixed-signal module is powered on. A TX window controlled by TDMA timer involves a TX dump window and a TX enable window simultaneously. The interval between the moment that TX mixed-signal module is powered on and the moment that data proceed to be forwarded from DSP to GMSK or 8PSK modulator by Baseband Serial Ports can be well controlled in TDMA timer. TX dump windows always win over TX enable windows. It means that a TX dump window will always raise a TX enable window. TX enable windows can be raised by TDMA timer or by programming TX power-down bit in global control registers to be '0'. It is useful in debugging environment.

Accordingly, Baseband Serial Ports are only under the control of TX/RX dump window. Note that if TX/RX dump window is not integer multiplies of bit-time it will be extended to be integer multiplies of bit-time. For example, if TX/RX dump window has interval of 156.25 bit-times then it will be extended to 157 bit-times in Baseband Serial Ports.

For uplink path, if uplink path is enabled, then the bit BULEN (Baseband Up-Link Enable) will be '1'. Otherwise the bit BULEN will be 0.

For downlink path, if BDLEN (Baseband DownLink Enable) is enabled, RX mixed-signal module will also be powered on. Similarly, once uplink path is enabled, TX mixed-signal module will also be powered on. Furthermore, enabling BDLFS (Baseband Down-Link FrameSync) Baseband Serial Ports for downlink path refers to dumping results from RX digital FIR filter to DSP.

5.1.2 Register Definitions

BFE+0000h Base-band Common Control Register BFE_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BCIEN
Type																R/W
Reset																0

This register is for common control of Baseband Front End. It consists of ciphering encryption control.

BCIEN The bit is for ciphering encryption control. If the bit is set to '1', XOR will be performed on some TX bits (payload of Normal Burst) and ciphering pattern bit from DSP, and then the result is forwarded to GMSK Modulator only. Meanwhile, Baseband Front End will generate signals to drive DSP ciphering process and produce corresponding ciphering pattern bits if the bit is set to '1'. If the bit is set to '0', the TX bit from DSP will be forwarded to GMSK modulator directly. Baseband Front End will not activate DSP ciphering process.

0 Disable ciphering encryption.

1 Enable ciphering encryption.

BFE +0004h Base-band Common Status Register BFE_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name							BULEN4	BULEN3	BULEN2	BULEN1	BULFS4	BULFS3	BULFS2	BULFS1	BDLFS	BDLEN
Type							RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset							0	0	0	0	0	0	0	0	0	0

This register indicates status of Baseband Front End. Under control of TDMA timer, Baseband Front End can be driven in several statuses. If downlink path is enabled, then the bit BDLEN will be '1'. Otherwise the bit BDLEN will be '0'. If downlink parts of Baseband Serial Ports is enabled, the bit BDLFS will be '1'. Otherwise the bit BDLFS will be '0'. If uplink path is enabled, then the bit BULEN will be '1'. Otherwise the bit BULEN will be 0. If uplink parts of Baseband Serial Ports is enabled, the bit BULFS will be '1'. Otherwise the bit BULFS will be '0'. Once downlink path is enabled, RX mixed-signal module will also be powered on. Similarly, once uplink path is enabled, TX mixed-signal module will also be powered on. Furthermore, enabling Baseband Serial Ports for downlink path refers to dumping results from RX digital FIR filter to DSP. Similarly, enabling Baseband Serial Ports for uplink path refers to forwarding TX bit from DSP to GMSK modulator. BDLEN stands for "**B**aseband **D**own**L**ink **EN**able". BULEN stands for "**B**aseband **U**p**L**ink **EN**able". BDLFS stands for "**B**aseband **D**own**L**ink **F**rame**S**ync". BULFS stands for "**B**aseband **U**pLink **F**rame**S**ync".

BDLEN Indicate if downlink path is enabled.

0 Disabled

1 Enabled

BDLFS Indicate if Baseband Serial Ports for downlink path is enabled.

0 Disabled

1 Enabled

BULFS1 Indicate if Baseband Serial Ports for uplink path is enabled in 1st burst

0 Disabled

1 Enabled

BULFS2 Indicate if Baseband Serial Ports for uplink path is enabled in 2nd burst

0 Disabled

1 Enabled

BULFS3 Indicate if Baseband Serial Ports for uplink path is enabled in 3rd burst

0 Disabled

1 Enabled

BULFS4 Indicate if Baseband Serial Ports for uplink path is enabled in 4th burst

0 Disabled

1 Enabled

BULEN1 Indicate if uplink path is enabled in 1st burst.

0 Disabled

1 Enabled

BULEN2 Indicate if uplink path is enabled in 2nd burst.

0 Disabled

1 Enabled

BULEN3 Indicate if uplink path is enabled in 3rd burst.

0 Disabled

1 Enabled

BULEN4 Indicate if uplink path is enabled in 4th burst.

0 Disabled

1 Enabled

5.2 Downlink Path (RX Path)

5.2.1 General Description

On the downlink path, the sub-block between RX mixed-signal module and Baseband Serial Ports is RX Path. It mainly consists of two parallel digital FIR filter with programmable tap number, two sets of multiplexing paths for loopback modes, interface for RX mixed-signal module, Interference Detection Circuit, I/Q Gain Mismatch compensation circuit, and interface for Baseband Serial Ports. The block diagram is shown in **Figure 53** .

While RX enable windows are open, RX Path will issue control signals to have RX mixed-signal module proceed to make A/D conversion. As each conversion is finished, one set of I/Q signals will be latched. There exists a digital FIR filter for these I/Q signals. The result of filtering will be dumped to Baseband Serial Ports whenever RX dump windows are opened.

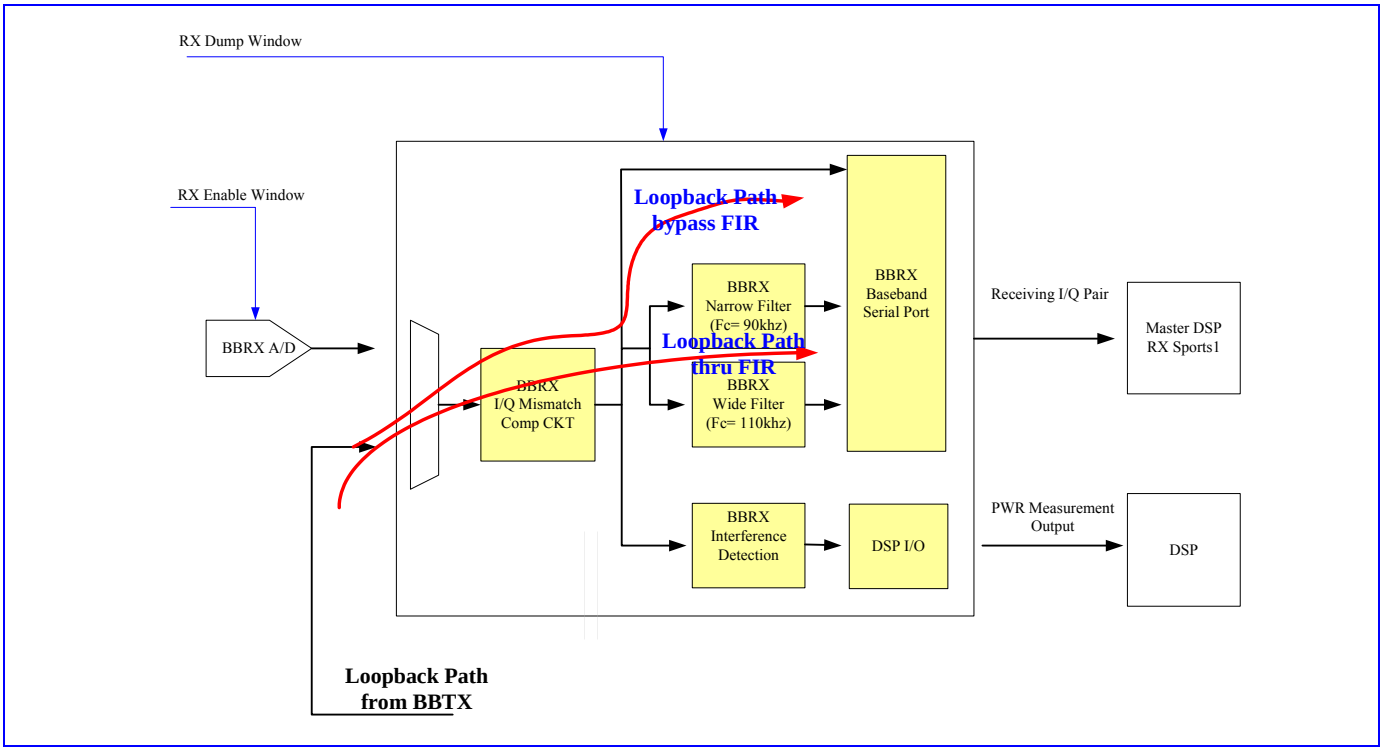


Figure 53 Block diagram of RX path

5.2.2 Comb Filter

The comb filter which takes the 2-bit A/D converter as input, and output the 18-bit I/Q data words to the baseband receiving path. The system is designed as 48X over-sampling with symbol period 541.7 kHz, thus the data inputs are 26MHz 2-bit signal. The input 2-bit signals are formed in (sign, magnitude) manner; that is, total 3 values are permitted as input: (-1, 0, +1).

The data path is mainly a decimation filter which contains the integration stages and the decimation stages. For a 3rd order design with 48X over-sampling, gain of the data path is 48^3 = 110592, which locates between 2^{16} and 2^{17}. Thus the internal word-length must be set to 18-bit to avoid overflow in the integration process.

5.2.3 Compensation Circuit - I/Q Gain Mismatch

In order to compensate I/Q Gain Mismatch , configure IGAINSEL(I Gain Selection) in RX_CON control register, the I over Q ratio can be compensate for 0.3 dB/step, totally 11 steps resulted in dynamic range up to +/-1.5dB.

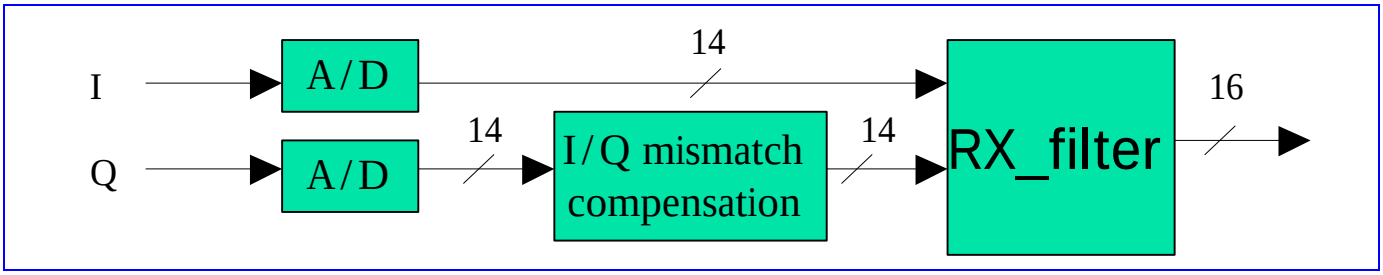


Figure 54 I/Q Mismatch Compensation Block Diagram

The I/Q swap functionality can be setting “1” for SWAP(I/Q Swapping) in RX_CFG control register, which is used to swap I/Q channel signals from RX mixed-signal module before they are latched into RX digital FIR filter. It is intended to provide flexibility for I/Q connection with RF modules

5.2.4 Phase De-rotation Circuit

Phase De-rotation Mode will usually turn on during FCB Detection for down conversion the wide spread receiving power to 67.7 kHz single tone.

Two separate control for implement this mode on data path through NarrowFIR filter or WideFIR filter by setting ‘1’ to PHROEN_N (Phase Rotate Enable for NarrowFIR) or PHROEN_W(Phase Rotate Enable for WideFIR) in RX_CON control register, respectively.

5.2.5 Adaptive Bandwidth & Programmable Digital FIR Filter

For the two parallel digital FIR Filter, the total tap number is programmable by FIRTPNO(FIR Tap number) in RX_CFG control register, which will configure the filter with different tap buffer depth.

5.2.5.1 Programmable tap & programmable Coefficient for FIR

In order to satisfy the signal requirements in both of idle and traffic modes, two sets of coefficients must be provided for the RX digital FIR filter. Therefore, the RX digital FIR filter is implemented as a FIR filter with programmable coefficients which can be accessed on the APB bus. The coefficient number can be programmable, range from 1~31. Each coefficient is ten-bit wide and coded in 2’s complement.

Take 21 Tap Coefficient for example, based on assumption that the FIR filter has symmetric coefficients, only 11 coefficients are implemented as programmable registers to save gate count. Denoting these digital filter coefficients as RX_RAM0_CS0 ~ RX_RAM0_CS11(RX_RAM0 Coefficient Set 0~11), and these tap registers for I/Q channel signals as I/QTAPR [0:20], then the RX digital FIR filtering can be represented as the following equation:

$$I_{out}(m) = \sum_{i=0}^{20} BDLDFCR[i] * ITAPR[i]\Big|_{\text{at time n+4m}} = BDLDFCR[11] * ITAPR[11] + \sum_{i=0}^{11} BDLDFCR[i] * (ITAPR[i] + ITAPR[20-i])\Big|$$

$$Q_{out}(m) = \sum_{i=0}^{20} BDLDFCR[i] * QTAPR[i]\Big|_{\text{at time n+4m}} = BDLDFCR[11] * QTAPR[11] + \sum_{i=0}^{11} BDLDFCR[i] * (QTAPR[i] + QTAPR[20-i])\Big|$$

$$BDLDFCR[i] = BDLDFCR[20-i], i = 0,1,...,11$$

where ITAPR [0] and QTAPR [0] are the latest samples for I- and Q-channel respectively and assume $I_{out}(0), Q_{out}(0)$ are obtained based on the content of tap registers at time moment *n*. From the equation above it follows that the digital RX FIR filter will produce one output every four data conversions out of A/D converters. That is, filtering and decimation are performed simultaneously to achieve low power design.

However, different "Coefficient Set ID"(CS ID) will be dump to Slave DSP RX buffer to represent the current selecting of coefficient Set from either 2 ROM table or 2 set of programmable RAM table according to different burst mode, while ROM table are fixed coefficient and RAM table can be programmed through 2set of 16 control register (RX_RAM0_CS0~ RX_RAM_CS15, (RX_RAM1_CS0~RX_RAM1_CS15). Generally, CSID = 0 represent ROM table selection, while CSID 2~ CSID 15 represent RAM table selection. Please be noted that the total coefficient number in a RAM table should be greater than half of the FIRTPNO (total FIR Tap number) and smaller than half of maximum tap number (15) since the FIR function in symmetric behavior.

Additionally, the data sequence of two parallel FIR filter output will dump to Master DSP RX buffer in following order : "I channel output from Narrow FIR"=> " I channel output from Wide FIR""=>"Q channel output from Narrow FIR=>" Q channel output from Wide FIR.

5.2.5.1.1 Coefficient Set Selection

The Coefficient Set used for digital FIR can be changed during different burst mode switching. For example, during Normal Burst while no FB_STROBE (Frequency Burst Strobe, comes from TDMA controller) assertion, defined as "State B", "Coefficient Set ID" (CSID) selection for both Narrow/Wide filter can be configured by ST_B_WCOF_SEL (State B Wide FIR Coefficient Selection) and "ST_B_NCOF_SEL" (State B Narrow FIR Coefficient Selection) on RX_FIR_CSID_CON control register, respectively. Usually during State B, Layer 1 software will select RAM table coefficient from either RAM0 or RAM1 table in condition I for Narrow FIR and Wide FIR, respectively. The CS ID for both Narrow / Wide FIR filter be stored at Slave DSP RX buffer once TDMA trigger RX interrupt to DSP..ST_A_NCOF_SEL" (State A Narrow FIR Coefficient Selection) on RX_FIR_CSID_CON control register.

During FCB detection, MCU will notice TDMA controller by assertion FB_STROBE, defined as "StateA". "Coefficient Set ID" (CS ID) selection for both Narrow/Wide filter can be configured by ST_A_WCOF_SEL(State A Wide FIR Coefficient Selection) and "ST_A_NCOF_SEL" (State A Narrow FIR Coefficient Selection) on RX_FIR_CSID_CON control register, respectively. Usually during State B, Layer 1 software will select CS ID 2 and CSID 3 from either ROM0 or ROM1 table or RAM0 or RAM1 table in Condition II for Narrow FIR and Wide FIR, respectively.

5.2.5.2 Interference Detection Circuit for Adaptive Bandwidth Scheme

Used to compare the power of Co-channel Interference and Adjacent-channel Interference for determine if WideFIR filter is needed rather than default NarrowFIR filter. Two parallel path of power measurement for evaluating Co-channel effect or Adjacent Channel Effect by analyzing power after High Pass Filter (HPF) or Band Pass Filter (BPF), respectively. If Co-channel effect is worse than Adjacent Channel effect, WideFIR filter is needed.

The power measurement is accumulate I/Q Root Mean Square (RMS) power over the whole RX burst window, while exact accumulation period within the burst can be adjusted the starting point offset and duration length.. The "starting point Offset" and be configured by "RXID_PWR_OFF[7:0]" (RX Interference Detection Power Starting Point Offset) and duration period by " RXID_PWR_PER[7:0]"(RX Interference Detection Power Duration Period) in RX_PM_CON control register, while default value for starting offset is 11 and duration period is 141. The two accumulated power measurement output for

Co-channel and Adjacent-channel will be dump to Slave DSP RX buffer alternatively at the end of the duration period within a burst. However, if the duration period is longer than the RX Dump Window, the accumulated measurement output will be dump out at falling edge of RX_DUMP_Window rather than the end of configured duration period.

Additionally, the power measurement data sequence at Slave DSP RX buffer will be "Coefficient Set ID for NarrowFIR filter"=> "Coefficient Set ID for WideFIR filter"=>"Power output of HPF(Co-channel)=>"Power output of BPF(Adjacent-channel), while the coefficient Set ID (CSID) is for DSP debug purpose.

The power result can be further scale down by control the PWR_SHFT_NO (power right Shift Number) in RX_CON control register. E.g. set to "1" will divide the power output by two.

5.2.5.3 Supporting Single Filter 2X symbol rate Mode

The two parallel FIR filter default output data rate in 1x Symbol rate after 2X decimation. but by programming 2XFIRSEL(2x Symbol Rate FIR Selection) in RX_CFG control register, WideFIR filter will be disable, while NarrowFIR filter will output data rate in 2X symbol rate without 2x decimation.

5.2.6 Debug Mode

5.2.6.1 Normal Mode bypass Filter

By setting "1" for BYPFLTR(Bypass Filter) in RX_CFG control register, the ADC outputs out of RX mixed-signal module will be directed into Baseband Serial Ports directly without through FIR. Limited by bandwidth of the serial interface between Baseband Serial Ports and DSP, only ADC outputs which are from either I-channel or Q-channel ADC can be dumped into DSP. Both I- and Q-channel ADC outputs cannot be dumped simultaneously. Which channel will be dumped is controlled by the register bit SWAP of the control register RX_CFG when downlink path is programmed in "Bypass RX digital FIR filter" mode. See register definition below for more details. The mode is for measurement of performance of A/D converters in RX mixed-signal module.

5.2.6.2 TX-RX Digital Loopback Mode (Debug Mode)

In addition to normal function, there are two loopback modes in RX Path. One is bypass-filter loopback mode, and the other is through-filter loopback mode. They are intended for verification of DSP firmware and hardware. The bypass-filter loopback mode refers to that RX digital FIR filter is not on the loopback path. However, the through-filter loopback mode refers to that RX digital FIR filter is on the loopback path, while " thru-Filter Loopback Mode" can be configured by setting "2'b10" for BLPEN(Baseband Loopback Enable) or "bypass-Filter Loopback Mode" by setting " 2'b01" for BLPEN in RX_CON control register.

5.2.7 Register Definitions

5.2.7.1 APB Register

BFE +0010h RX Configuration Register RX_CFG

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							FIRTPNO							2X FIRSEL	BYPFLTR	SWAP
Type							R/W							R/W	R/W	R/W
Reset							000000							0	0	0

This register is for configuration of downlink path, inclusive of configuration of RX mixed-signal module and RX path in Baseband Front End.

SWAP This register bit is for control of whether I/Q channel signals need to swap before they are inputted to Baseband Front End. It provides flexibility flexible of connection of I/Q channel signals between RF module and baseband module. The register bit has another purpose when the register bit "BYPFLTR" is set to 1. Please see description for the register bit "BYPFLTR".

0 I- and Q-channel signals are not swapped

1 I- and Q-channel signals are swapped

BYPFLTR Bypass RX FIR Filter control. The register bit is used to configure Baseband Front End in the state called "Bypass RX FIR filter state" or not. Once the bit is set to '1', RX FIR filter will be bypassed. That is, ADC outputs of RX mixed-signal module that are has 11-bit resolution and at sampling rate of 1.083MHz can be dumped into DSP by Baseband Serial Ports and RX FIR filtering will not be performed on them. Limited by bandwidth of the serial interface between Baseband Serial Ports and DSP, these ADC outputs are all from either I-channel or Q-channel ADC. Both of I- and Q-channel ADC outputs cannot be dumped simultaneously. When the bit is set to '1' and the register bit "SWAP" is set to '0', ADC outputs of I-channel will be dumped. When the bit is set to '1' and the register bit "SWAP" is set to '1', ADC outputs of Q-channel will be dumped.

0 Not bypass RX FIR filter

1 Bypass RX FIR filter

2XFIRSEL Enable for single FIR w/ output data rate in 2x Symbol rate output Enable. This mode will disable WideFIR, while Narrow FIR w/ 2x symbol rate without 2x decimation.

0 Disable Single FIR 2X symbol rate output mode.

1 Enable Single FIR 2X symbol rate output mode.

FIRTPNO RX FIR filter tap no. select. This control register will control the two parallel digital filter with different tap buffer depth since the FIR function in symmetric behavior. The maximum tap number is 31, minimum is 1., ODD number only.

BFE+0014h RX Control Register RX_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PWR_SHFT_NO				IGAINSEL				PH_ROEN_N	PH_ROEN_W	BLPEN	
Type					R/W				R/W				R/W	R/W	R/W	
Reset					0000				0000				0	0	00	

This register is for control of downlink path, inclusive of control of RX mixed-signal module and RX path in Baseband Front End module.

BLPEN The register field is for loopback configuration selection in Baseband Front End.

00 Configure Baseband Front End in normal function mode

01 Configure Baseband Front End in bypass-filter loopback mode

10 Configure Baseband Front End in through-filter loopback mode

11 Reserved

PH_ROEN_W Enable for I/Q pair Phase De-rotation in Wide FIR Data Path.

0 Disable Phase De-rotation for I/Q pair.

1 Enable Phase De-rotation for I/Q pair.

PH_ROEN_N Enable for I/Q pair Phase De-rotation in Narrow FIR Data Path.

0 Disable Phase De-rotation for I/Q pair.

1 Enable Phase De-rotation for I/Q pair.

IGAINSEL RX I data Gain Compensation Select. 0.3dB/step, totally 11 steps and dynamic range up to +/-1.5dB for

0000 compensate 0dB for I/Q

0001 compensate 0.3dB for I/Q

0010 compensate 0.6dB for I/Q

0011 compensate 0.9dB for I/Q

0100 compensate 1.2dB for I/Q

0101 compensate 1.5dB for I/Q

1001 compensate –0.3dB for I/Q

1010 compensate -0.6dB for I/Q

1011 compensate –0.9dB for I/Q

1100 compensate –1.2dB for I/Q

1101 compensate –1.5dB for I/Q

Default No compensation for I/Q

PWR_SHFT_NO Power measuring Result Right Shift Number. The Power level measurement result can be right shift from 0 to 16 bits.

BFE+0018h RX Interference Detection Power Measurement Control Register RX_PM_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RXID_PWR_PER								RXID_PWR_OFF							
Type	R/W								R/W							
Reset	8D								B							

RXID_PWR_OFF RX Interference Detection Power Measurement Starting Offset. Setting this register will delay the starting time of Interference Detection Power Measurement in symbol time unit. Maximum value is 156, while default value is 11 (0xB).

RXID_PWR_PER RX Interference Detection Power Measurement Accumulation Period. By setting this control register will determine the length of accumulation duration for power Measurement. Minimum value is 0, Maximum value is 156, while default value is 141(0x8D). Please notice that RXID_PWR_OFF + RXID_PWR_PER should less than 154 due to hardware implementation limitation.

BFE+001Ch RX FIR Coefficient Set ID Control Register RX_FIR_CSID_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_A_NCOF_SEL								ST_B_NCOF_SEL				ST_B_WCOF_SEL			
Type	R/W								R/W				R/W			
Reset	0000								0010				0011			

These three set of Coefficient Set ID will be dump to slave DSP RX Buffer for indicating the current selection of FIR coefficient from either RAM or ROM table, while CSID= 0 represents ROM table selection, and CSID2~CSID15 represent RAM table selection.

ST_B_WCOF_SEL State B Coefficient Set Selection for Wide FIR.

ST_B_NCOF_SEL State B Coefficient Set Selection for Narrow FIR.

ST_A_NCOF_SEL State A Coefficient Set Selection for Narrow FIR.

BFE +0070h RX RAM0Coefficient Set 0Register RX_RAM0_CS0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RX_RAM0_CS0									
Type							R/W									
Reset							000000000									

This register is 1st of the 16 coefficient in RAM0 table, Coefficient Set ID 2 or 4. The content is coded in 2's complement. That is, its maximum is 255 and its minimum is –256, while the total coefficient number in this Coefficient Set has to be greater than half of TAPNO(programmable Tap no.) and smaller than half of maximum tap no(15).

Register Address	Register Function	Acronym
BFE +0070h	RX RAM0Coefficient Set 0 Register	RX_RAM0_CS0
BFE +0074h	RX RAM0Coefficient Set 1 Register	RX_RAM0_CS1
BFE +0078h	RX RAM0Coefficient Set 2 Register	RX_RAM0_CS2
BFE +007Ch	RX RAM0Coefficient Set 3 Register	RX_RAM0_CS3
BFE +0080h	RX RAM0Coefficient Set 4 Register	RX_RAM0_CS 4
BFE +0084h	RX RAM0Coefficient Set 5 Register	RX_RAM0_CS 5
BFE +0088h	RX RAM0Coefficient Set 6 Register	RX_RAM0_CS 6

BFE +008Ch	RX RAM0Coefficient Set 7 Register	RX_RAM0_CS 7
BFE +0090h	RX RAM0Coefficient Set 8 Register	RX_RAM0_CS 8
BFE +0094h	RX RAM0Coefficient Set 9 Register	RX_RAM0_CS 9
BFE +0098h	RX RAM0Coefficient Set 10 Register	RX_RAM0_CS 10
BFE +009Ch	RX RAM0Coefficient Set 11Register	RX_RAM0_CS 11
BFE +00a0h	RX RAM0Coefficient Set 12Register	RX_RAM0_CS 12
BFE +00a4h	RX RAM0Coefficient Set 13Register	RX_RAM0_CS 13
BFE +00a8h	RX RAM0Coefficient Set 14 Register	RX_RAM0_CS 14
BFE +00aCh	RX RAM0Coefficient Set 15 Register	RX_RAM0_CS 15

BFE +0020h RX RAM1 Coefficient Set 0 Register RX_RAM1_CS 0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RX_RAM1_CS 0									
Type							R/W									
Reset							000000000									

This register is 1st of the 16 coefficient in RAM1 table, Coefficient Set ID 2 or 4. The content is coded in 2's complement. That is, its maximum is 255 and its minimum is –256, while the total coefficient number in this Coefficient Set has to be greater than half of TAPNO(programmable Tap no.) and smaller than half of maximum tap no(15).

Register Address	Register Function	Acronym
BFE +0020h	RX RAM1 Coefficient Set 0 Register	RX_RAM1_CS 0
BFE +0024h	RX RAM1 Coefficient Set 1Register	RX_RAM1_CS 1
BFE +0028h	RX RAM1 Coefficient Set 2 Register	RX_RAM1_CS 2
BFE +002Ch	RX RAM1 Coefficient Set 3 Register	RX_RAM1_CS 3
BFE +0030h	RX RAM1 Coefficient Set 4 Register	RX_RAM1_CS 4
BFE +0034h	RX RAM1 Coefficient Set 5 Register	RX_RAM1_CS 5
BFE +0038h	RX RAM1 Coefficient Set 6 Register	RX_RAM1_CS 6
BFE +003Ch	RX RAM1 Coefficient Set 7 Register	RX_RAM1_CS 7
BFE +0040h	RX RAM1 Coefficient Set 8 Register	RX_RAM1_CS 8
BFE +0044h	RX RAM1 Coefficient Set 9 Register	RX_RAM1_CS 9
BFE +0048h	RX RAM1 Coefficient Set 10 Register	RX_RAM1_CS 10

BFE +004Ch	RX RAM1 Coefficient Set 11 Register	RX_RAM1_CS 11
BFE +0050h	RX RAM1 Coefficient Set 12 Register	RX_RAM1_CS 12
BFE +0054h	RX RAM1 Coefficient Set 13 Register	RX_RAM1_CS 13
BFE +0058h	RX RAM1 Coefficient Set 14 Register	RX_RAM1_CS 14
BFE +005Ch	RX RAM1 Coefficient Set 15 Register	RX_RAM1_CS 15

BFE+00B0h RX Interference Detection HPF Power Register RX_HPWR_STS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PWR_HPF															
Type	R/O															
Reset	0000000000000000															

This register is for read the power measurement result of the HPF interference detection filter.

RX_PWR_HPF Value of the power measurement result for the outband interference detection.

BFE+00B4h RX Interference Detection BPF Power Register RX_BPWR_STS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PWR_BPF															
Type	R/O															
Reset	0000000000000000															

This register is for read the power measurement result of the BPF interference detection filter.

RX_PWR_BPF Value of the power measurement result for the inband interference detection

5.2.7.2 DSP I/O Register

BFE+0743h RX HPF ITD Power Register of Window0 DSPIO_ITD_H_0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ITD_H_DATA_0															
Type	R/O															

Reset	0000000000000000

This register is for **DSP** to read the power measurement result of the BPF interference detection filter through DSP I/O.

DSPIO_ITD_H_0 Value of the power measurement result for the outband interference detection of window 0.

Register Address	Register Function	Acronym
BFE +0743h	RX HPF ITD Power Register of Window0	DSPIO_ITD_H_0
BFE +0747h	RX HPF ITD Power Register of Window1	DSPIO_ITD_H_1
BFE +074Bh	RX HPF ITD Power Register of Window2	DSPIO_ITD_H_2
BFE +074Fh	RX HPF ITD Power Register of Window3	DSPIO_ITD_H_3
BFE +0753h	RX HPF ITD Power Register of Window4	DSPIO_ITD_H_4
BFE +0757h	RX HPF ITD Power Register of Window5	DSPIO_ITD_H_5

BFE+0744h RX BPF ITD Power Register of Window0 DSPIO_ITD_B_0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ITD_B_DATA_0															
Type	R/O															
Reset	0000000000000000															

This register is for **DSP** to read the power measurement result of the BPF interference detection filter through DSP I/O.

DSPIO_ITD_B_0 Value of the power measurement result for the inband interference detection of window 0.

Register Address	Register Function	Acronym
BFE +0744h	RX BPF ITD Power Register of Window0	DSPIO_ITD_B_0
BFE +0748h	RX BPF ITD Power Register of Window1	DSPIO_ITD_B_1
BFE +074Ch	RX BPF ITD Power Register of Window2	DSPIO_ITD_B_2
BFE +0750h	RX BPF ITD Power Register of Window3	DSPIO_ITD_B_3
BFE +0754h	RX BPF ITD Power Register of Window4	DSPIO_ITD_B_4
BFE +0758h	RX BPF ITD Power Register of Window5	DSPIO_ITD_B_5

BFE+0759h RX ITD Power Measurement Ready Flag DSPIO_RXID_RDY

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name											RXID_RDY_5	RXID_RDY_4	RXID_RDY_3	RXID_RDY_2	RXID_RDY_1	RXID_RDY_0
Type											R/O	R/O	R/O	R/O	R/O	R/O
Reset											0	0	0	0	0	0

This register is for **DSP** to see whether the RX ITD power register is ready or not through DSP I/O. When the DSPIO_ITD_H_0 and DSPIO_ITD_B_0 are ready, bit 0 is set to 1. Moreover, while DSP read the data of DSPIO_ITD_H_0 and DSPIO_ITD_B_0, bit 0 is reset to 0.

RXID_RDY_0 Ready flag for DSP to read the ITD power measurement result of window0.

RXID_RDY_1 Ready flag for DSP to read the ITD power measurement result of window1.

RXID_RDY_2 Ready flag for DSP to read the ITD power measurement result of window2.

RXID_RDY_3 Ready flag for DSP to read the ITD power measurement result of window3.

RXID_RDY_4 Ready flag for DSP to read the ITD power measurement result of window4.

RXID_RDY_5 Ready flag for DSP to read the ITD power measurement result of window5.

5.3 Uplink Path (TX Path)

5.3.1 General Description

The purpose of the uplink path inside Baseband Front End is to sink TX symbols, from DSP, then perform GMSK modulation on them, then perform offset cancellation on I/Q digital signals, and finally control TX mixed-signal module to make D/A conversion on I/Q signals out of GMSK Modulator with offset cancellation. Accordingly, the uplink path is composed of uplink parts of Baseband Serial Ports, GSM Encryptor, GMSK Modulator and several compensation circuits including I/Q DC offset, I/Q Quadrature Phase Compensation, and I/Q Gain Mismatch. The block diagram of uplink path is shown as followed.

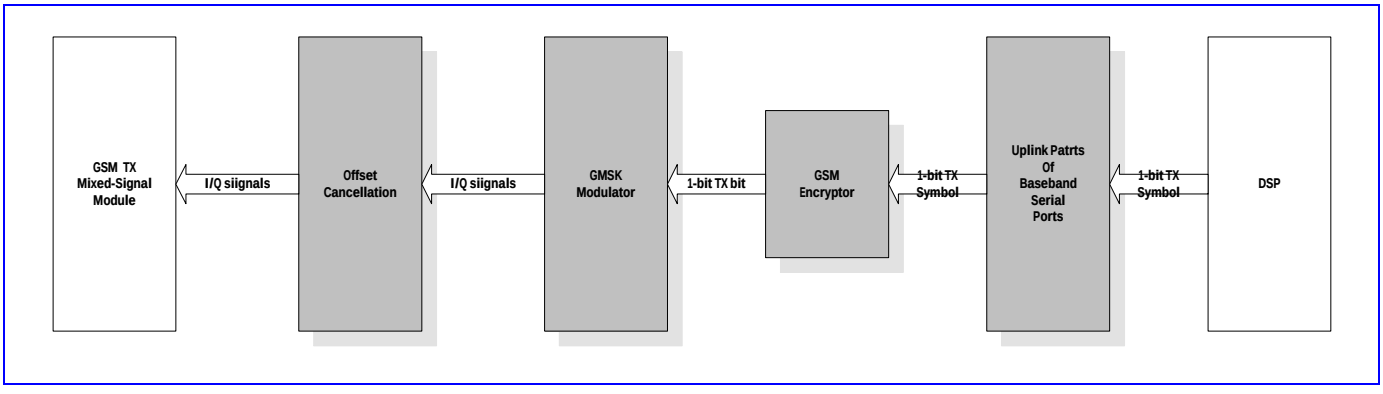


Figure 55 Block Diagram of Uplink Path

On uplink path, the content of a burst, including tail bits, data bits, and training sequence bits is sent from DSP. DSP outputs will be t translated by GMSK Modulator. Where translated bits after modulation will become I/Q digital signals with certain latency.

TDMA timer having a quarter-bit timing accuracy gives the timing windows for uplink operation. Uplink operation is controlled by TX enable window and TX dump window of TDMA timer. Usually, TX enable window is opened earlier than TX dump window. When TX enable window of TDMA timer is opened, uplink path in Baseband Front End will power-on GSK TX mixed-signal module and thus drive valid outputs to RF module. However, uplink parts of Baseband Serial Ports still do not sink data from DSP through the serial interface between Baseband Serial Ports and DSP until TX dump window of TDMA timer is opened.

5.3.2 Compensation Circuit

5.3.2.1 Quadrature Phase

For 8PSK Modulation, in order to improve the EVM performance, use PHSEL[2:0](Phase Select) in TX_CFG control register to compensate the quadrature phase. 6 steps, 1degree/step, up to +/3 degree dynamic range.

5.3.2.2 DC offset Cancellation

Offset cancellation will be performed on these I/Q digital signals to compensate offset error of D/A converters (DAC) in TX mixed-signal module. Finally the generated I/Q digital signals will be input to TX mixed-signal module that contains two DAC for I/Q signal respectively.

5.3.3 Auxiliary Calibration Circuit - 540 kHz Sine Tone Generator

By setting ‘1’ to SGEN(Sine Tone Generation) in TX_CFG control register, the BBTX output will become 540khz single sine tone, which is used for Factory Calibration scheme for Mixed Signal Low Pass Filter Cut-off Frequency Accuracy.

5.3.4 GSM Encryptor

When uplink parts of Baseband Serial Ports pass a TX symbol to GSM Encryptor, GSM Encryptor will perform encryption on the TX symbol if set ‘1’ to BCIEN(Baseband Ciphering Encryption) in BFE_CON register. Otherwise, the TX symbol will be directed to GMSK modulator directly.

5.3.5 Modulation

5.3.5.1 GMSK Modulation

GMSK Modulator is used to convert bit stream of GSM bursts into in-phase and quadrature-phase outputs by means of GMSK modulation scheme. It consists of a ROM table, timing control logic and some state registers for GMSK modulation scheme. GMSK Modulator is activated when TX dump window is opened. There is latency between assertion of TX dump window and the first valid output of GMSK Modulator. The reason is because the bit rate of TX symbols is 270.833 KHz and the output rate of GMSK Modulator is 4.333 MHz, and therefore timing synchronization is necessary between the two rates.

Additionally, in order to prevent phase discontinuity in between the multiple-burst Mode, the GMSK modulator will output continuous 67.7khs sine tone outside the burst once RX DAC Enable window is still asserted. Once RX DAC Enable window is disserted, GMSK modulator will park at DC level.

5.3.5.2 I/Q Swap

By setting ‘1’ to IQSWP in TX_CFG control register, phase on I/Q plane will rotate in inverse direction. This option is to meet the different requirement form RF chip regarding I/Q plane. This control signal is for GMSK Modulation only.

5.3.5.3 Debug Mode

5.3.5.3.1 Modulation Bypass Mode

For DSP debug purpose, set both ‘1’ for MDBYP(Modulator Bypass) in TX_CFG control register and BYPFLR(Bypass RX Filter) in RX_CFG control register for directly loopback DSP 16-bits data (10bits valid data plus sign or zero extension)

through DAC only.

5.3.5.3.2 Force GMSK Modulator turn on

By setting '1' to APNDEN(Append Enable) bit in TX CFG control register, GMSK modulator will park on constant DC level during the non-burst period, while the I/Q pair output phase maybe discontinuous since both modulator will be reset at the beginning of the burst. However, the reset of the modulator will be helpful for the debugging purpose.

5.3.6 Register Definitions

BFE +0060h TX Configuration Register TX_CFG

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ALL_10_EN		SGEN	MDBYP				APNDEN
Type									RW		R/W	R/W				R/W
Reset									00		0	0				0

This register is for configuration of uplink path, inclusive of configuration of TX mixed-signal module and TX path in Baseband Front End.

APNDEN Appending Bits Enable. (For DSP digital loopback debug mode) The register bit is used to control the ending scheme of GPRS Mode GMSK modulation only.

0 Suitable for GPRS /EDGE mode. If a TX enable window contains several TX dump window, then GMSK modulator will still output in the intervals between two TX dump window and all 1's will be fed into GMSK modulator. In the other word, mainly used PA to perform the power ramp up/down, while Modulator output low amplitude sinewave. **Note that when the bit is set to '0', the interval between the moment at which TX enable window is activated and the moment at which TX dump window is activated must be multiples of one bit time.**

1 Suitable for GSM only. After a TX dump window, GMSK modulator will only output for some bit time.

MDBYP Modulator Bypass (For DSP Debug Mode) Select. The register bit is used to select the bypass mode for I/Q pair outputs bypass the GMSK modulator

0 Regular Modulation Mode

1 Bypass Modulator Mode (DSP Debug Mode).

SGEN SineTone Generator Enable. (For Factory Calibration Purpose). The register bit is used to select the TX modulator output switch to 540 kHz Sine Tone.

0 BBTX output from regulator modulator output.

1 BBTX output switch to 540 kHz sine Tone

ALL_10GEN For Debug mode of BBTX. Generate all 1's or zero's input during BBTX valid burst. For GMSK modulation, set 2'b1 or 2'b10 will generate 67.7 kHz sine tone. Default value 2'b00 is normal mode.

0 Normal Mode, regular modulator input from Slave DSP TX Buffer.

1 Debug Mode, All zero's input pattern generated; GMSK modulator will generate 67.7 kHz sine tone.

2 Debug Mode All 1's input pattern generated; GMSK modulator will generate 67.7 kHz sine tone.

BFE +0064h TX Control Register TX_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						PHSEL										IQSWP
Type						R/W										R/W
Reset						000										0

This register is for control of uplink path, inclusive of control of TX mixed-signal module and TX path in Baseband Front End.

IQSWP The register bit is for swapping the I- and Q-channel of the TX path. Moreover, this register is double buffered by EVENT_VALIDATE.

0: I and Q are not swapped.

1: I and Q are swapped.

PHSEL Quadrature phase compensation select

000: 0 degree compensation.

001: 1 degree compensation.

010: 2 degree compensation.

011: 3 degree compensation.

100: -3 degree compensation.

101: -2 degree compensation.

110: -1 degree compensation.

111: 0 degree compensation.

BFE +0068h TX I/Q Channel Offset Compensation Register TX_OFF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OFF_TYP		OFFQ[5:0]								OFFI[5:0]					
Type	R/W		R/W								R/W					
Reset	0		000000								000000					

The register is for offset cancellation of I-channel DAC in TX mixed-signal module. It is for compensation of offset error caused by I/Q-channel DAC in TX mixed-signal module. It is coded in 2’s complement, that is, with maximum 31 and minimum –32.

OFFI Value of offset cancellation for I-channel DAC in TX mixed-signal module

OFFQ Value of offset cancellation for Q-channel DAC in TX mixed-signal module

OFF_TYP Type of the OFFI and OFFQ register. While OFF_TYP = 1, the offset values are double buffered and can be chaneged burst by burst after EVENT_VALIDATE comes. Otherwise, the offset values would change immidately after the coming of APB commands, which can't be adjusted burst by burst.

0 No double buffer

1 Double buffered

6 Audio Front-End

6.1 General Description

The audio front-end essentially consists of voice and audio data paths. **Figure 56** shows the block diagram of the audio front-end. All voice band data paths comply with the GSM 03.50 specification. Mono hands-free audio or external FM radio playback paths are also provided. The audio stereo path facilitates CD-quality playback, external FM radio, and voice playback through a headset.

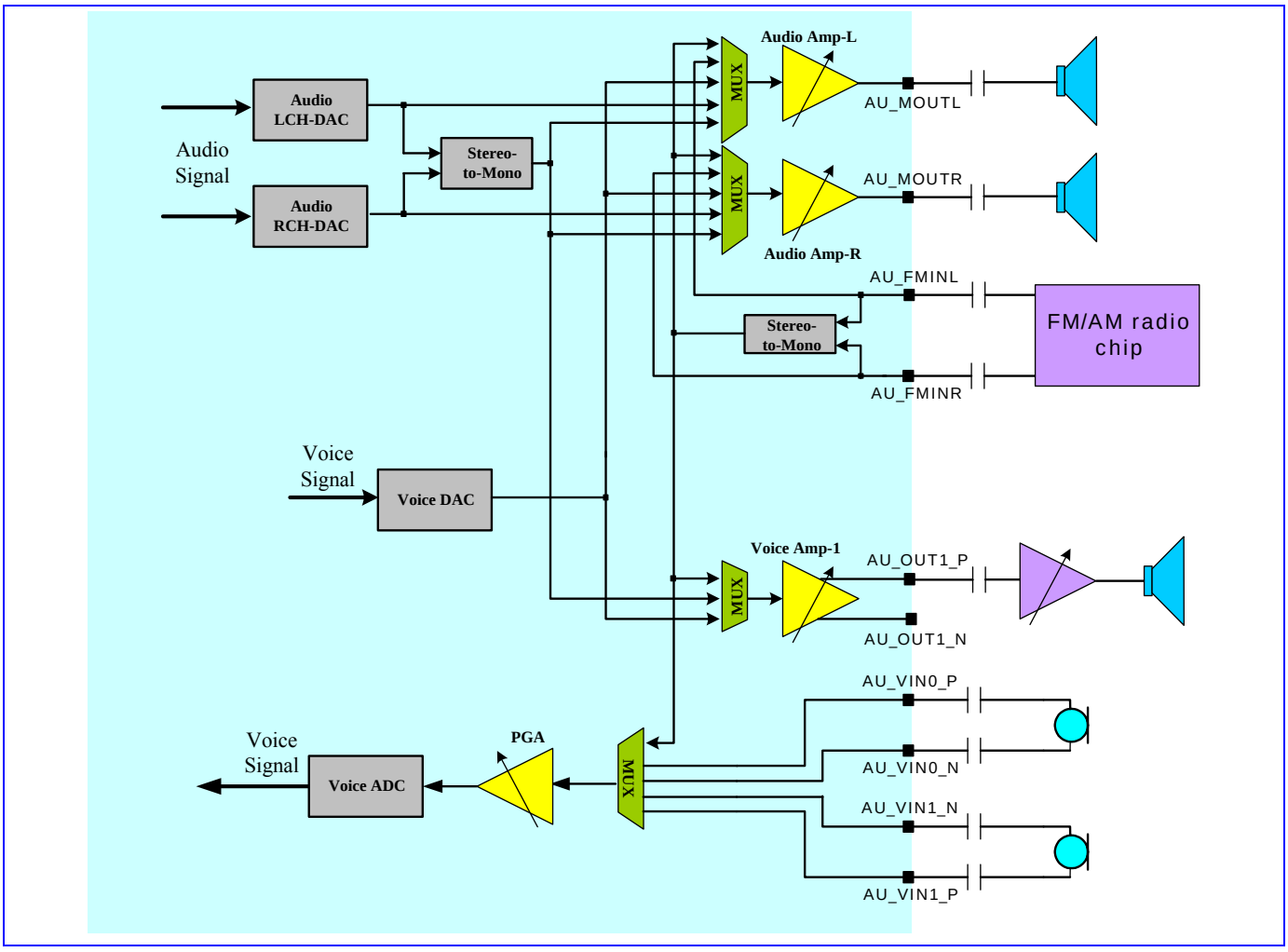


Figure 56 Block diagram of audio front-end

Figure 57 shows the digital circuits block diagram of the audio front-end. The APB register block is an APB peripheral that stores settings from the MCU. The DSP audio port block interfaces with the DSP for control and data communications. The digital filter block performs filter operations for voice band and audio band signal processing. The Digital Audio Interface (DAI) block communicates with the System Simulator for FTA or external Bluetooth modules.

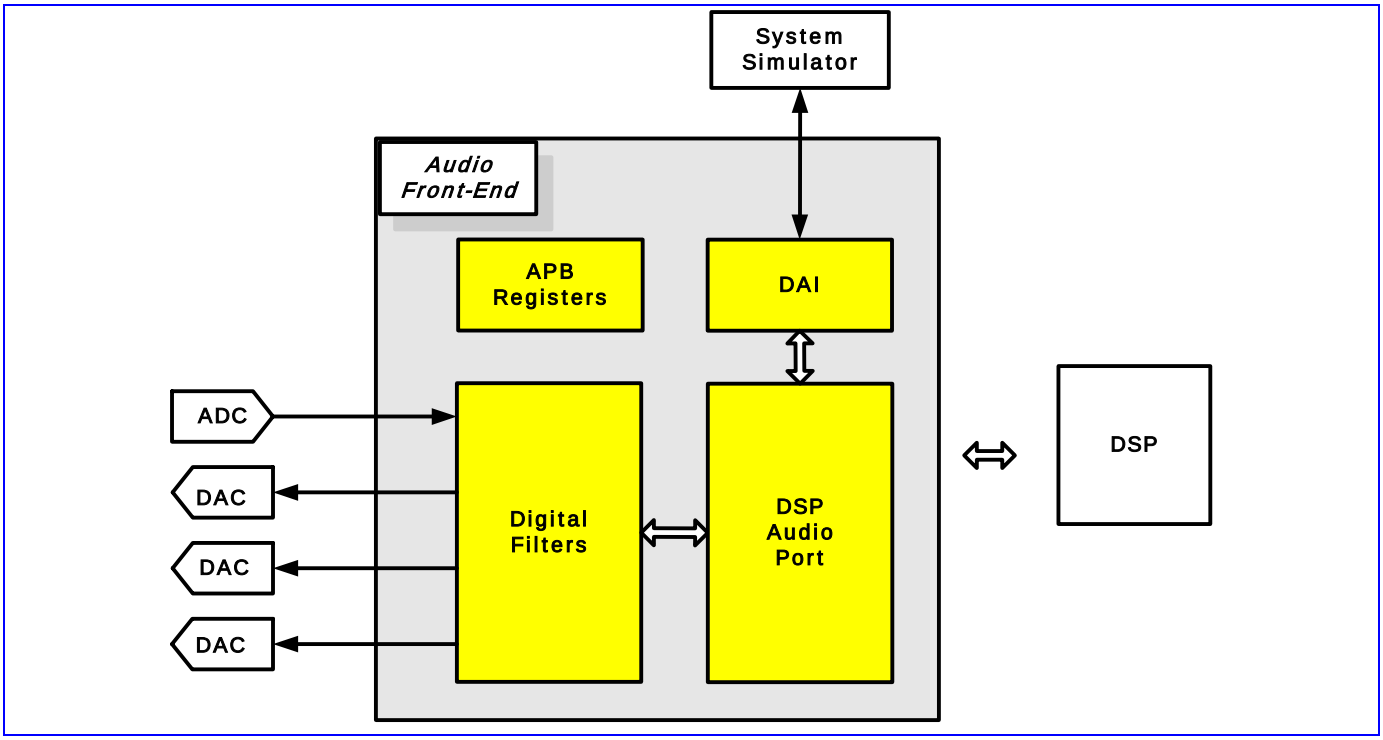


Figure 57 Block diagram of digital circuits of the audio front-end

To communicate with the external Bluetooth module, the master-mode PCM interface and master-mode I2S/EIAJ interface are supported. The clock of PCM interface is 256 kHz, and the frame sync is 8 kHz. Both long sync and short sync interfaces are supported. The PCM interface can transmit 16-bit stereo or 32-bit mono 8 kHz sampling rate voice signal. **Figure 58** shows the timing diagram of the PCM interface. Note that the serial data changes when the clock is rising and is latched when the clock is falling.

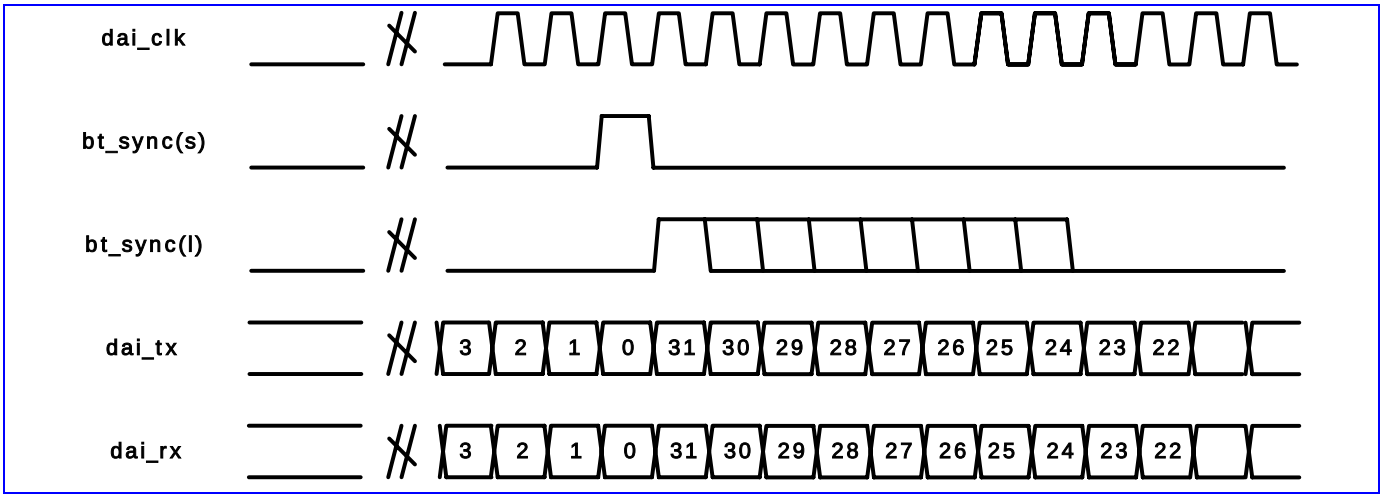


Figure 58 Timing diagram of Bluetooth application

I2S/EIAJ interface is designed to transmit high quality audio data. **Figure 58** and **Figure 59** illustrate the timing diagram of the two types of interfaces. I2S/EIAJ can support 32 kHz, 44.1kHz, and 48kHz sampling rate audio signals. The clock frequency of I2S/EIAJ can be 32×(sampling frequency), or 64×(sampling frequency). For example, to transmit a 44.1 kHz CD-quality music, the clock frequency should be 32 × 44.1 kHz = 1.4112 MHz or 64×44.1 kHz = 2.8224 MHz.

I2S/EIAJ interface is not only used for Bluetooth module, but also for external DAC components. Audio data can easily be sent to the external DAC through the I2S/EIAJ interface.

In this document, the I2S/EIAJ interface is referred to as EDI (External DAC Interface).

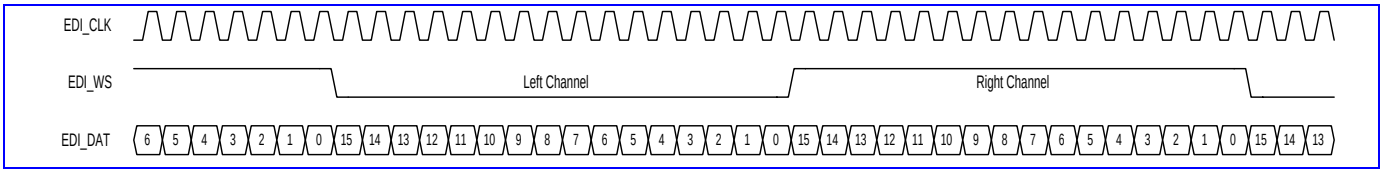


Figure 59 EDI Format 1: EIAJ (FMT = 0).

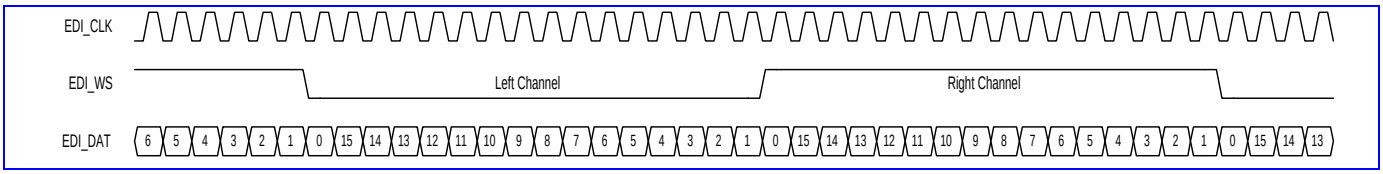


Figure 60 EDI Format 2: I^2S (FMT = 1).

6.1.1 DAI, PCM and EDI Pin Sharing

DAI, PCM, and EDI interfaces share the same pins. The pin mapping is listed in **Table 34**.

PIN NAME	DAI	PCM	EDI
DAI_CLK (OUTPUT)	DAI_CLK	PCM_CLK	EDI_CLK
DAI_TX (OUTPUT)	DAI_TX	PCM_OUT	EDI_DAT
DAI_RX (INPUT)	DAI_RX	PCM_IN	
BT_SYNC (OUTPUT)	-	PCM_SYNC	EDI_WS

Table 34 Pin mapping of DAI, PCM, and EDI interfaces.

Beside the shared pins, the EDI interface can also use other dedicated pins. With the dedicated pins, PCM and EDI interfaces can operate at the same time.

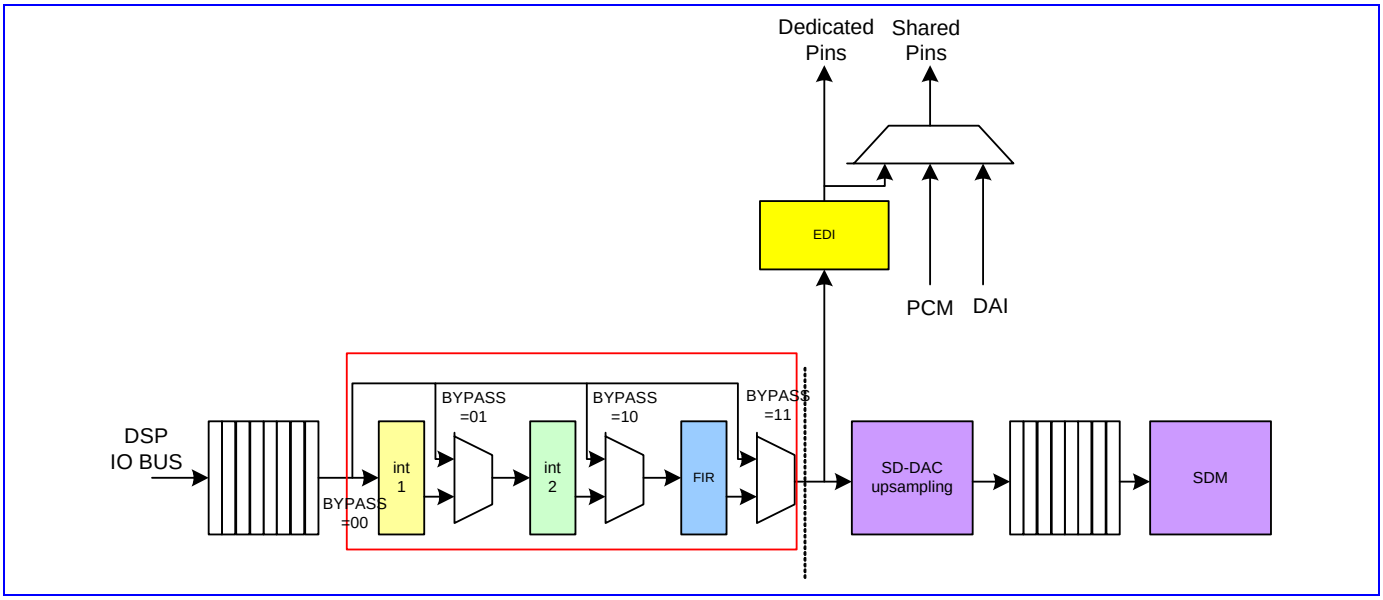


Figure 61 DAI, PCM, EDI interfaces

6.2 Register Definitions

MCU APB bus registers in audio front-end are listed as follows.

AFE+0000h AFE Voice MCU Control Register AFE_VMCU_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																VAFEON
Type																R/W
Reset																0

MCU sets this register to start AFE voice operation. A synchronous reset signal is issued, then periodical interrupts of 8-kHz frequency are issued. Clearing this register stops the interrupt generation.

VAFEON Turn on audio front-end operations.

AFE+000Ch AFE Voice Analog-Circuit Control Register 1 AFE_VMCU_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									VRSDON			VAFECLR_EN		VDITHVAL		VDITHON
Type									R/W			R/W		R/W		R/W
Reset									0			0		00		0

Set this register for consistency of analog circuit setting. Suggested value is 80h.

VRSDON Turn on the voice-band redundant signed digit function.

0: 1-bit 2-level mode

1: 2-bit 3-level mode

VAFECLR_EN Enable signal to reset voice downlink buffer or not while VAFE is powered down.

0 NO reset voice downlink buffer while VAFE is powered down

1 Reset voice downlink buffer while VAFE is powered down

VDITHVAL Voice downlink dither scaling setting

00 1/4

01 1/2

10 1

11 2

VDITHON Turn on the voice downlink dither function.

0 Turn off

1 Turn on

AFE+0014h AFE Voice DAI Bluetooth Control Register AFE_VDB_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										EDION	VDAION	PCMON	VBTSYNC	VBTSLEN		
Type										RW	R/W	R/W	R/W	R/W		
Reset										0	0	0	0	000		

Set this register for DAI test mode and Bluetooth application.

EDION EDI signals are selected as the output of DAI, PCM, EDI shared interface.

0 EDI is not selected. A dedicated EDI interface can be enabled by programming the GPIO selection. Please refer to GPIO section for details.

1 EDI is selected. VDAION and VBTON are not set.

VDAION Turn on the DAI function.

VBTON Turn on the Bluetooth PCM function.

VBTSYNC Bluetooth PCM frame sync type

0: short

1: long

VBTSLEN Bluetooth PCM long frame sync length = VBTSLEN+1

AFE+0018h AFE Voice Look-Back mode Control Register AFE_VLB_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													~~VBYPASSIIR~~	VDAPINMODE	VINTINMODE	VDECINMODE
Type													~~R/W~~	R/W	R/W	R/W
Reset													~~0~~	0	0	0

Set this register for AFE voice digital circuit configuration control. Several loop back modes are implemented for test purposes. Default values correspond to the normal function mode.

~~VBYPASSIIR Bypass hardware IIR filters.~~

VDAPINMODE DSP audio port input mode control

0 Normal mode

1 Loop back mode

VINTINMODE interpolator input mode control

0 Normal mode

1 Loop back mode

VDECINMODE decimator input mode control

0 Normal mode

1 Loop back mode

AFE+0020h AFE Audio MCU Control Register 0 AFE_AMCU_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																AAFEON
Type																R/W
Reset																0

MCU sets this register to start AFE audio operation. A synchronous reset signal is issued, then periodical interrupts of 1/6 sampling frequency are issued. Clearing this register stops the interrupt generation.

AFE+0024h AFE Audio Control Register 1 AFE_AMCU_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		MONO			BYPASS			ADITHON	ADITHVAL		ARAMPSP		AMUTER	AMUTEL	AFS	
Type		R/W			RW			R/W	R/W		R/W		R/W	R/W	R/W	
Reset		0			00			0	00		00		0	0	00	

MCU sets this register to inform hardware of the sampling frequency of audio being played back.

MONO Mono mode select. AFE HW will do (left + right) / 2 operation to the audio sample pair. Thus both DAC at right/left channels will have the same inputs.

0 Disable mono mode.

1 Enable mono mode.

BYPASS To bypass part of the audio hardware path.

00 No bypass. The input data rate is 1/4 sampling frequency. For example, if the sampling frequency is 32 kHz, then the input data rate is 8 kHz.

01 Bypass the first stage of interpolation. The input data rate is 1/2 the sampling frequency.

10 Bypass two stages of interpolation. The input data rate is the same as the sampling frequency.

11 Bypass two stages of interpolation and EQ filter. The input data rate is the same as the sampling frequency.

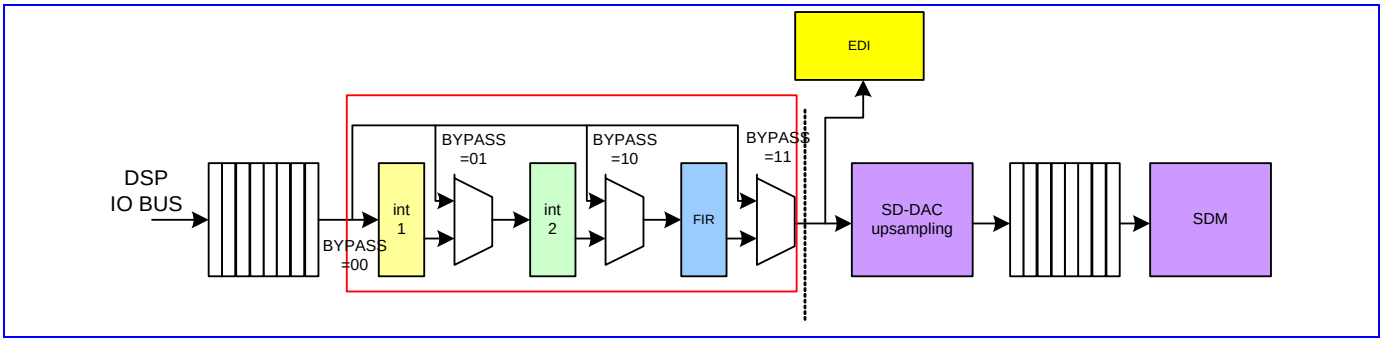


Figure 62 Block diagram of the audio path.

ADITHON Turn on the audio dither function.

ADITHVAL Dither scaling setting.

00 1/4

01 1/2

10 1

11 2

ARAMPSP ramp up/down speed selection

00 8, 4096/AFS

01 16, 2048/AFS

10 24, 1024/AFS

11 32, 512/AFS

AMUTER Mute the audio R-channel, with a soft ramp up/down.

AMUTEL Mute the audio L-channel, with a soft ramp up/down.

AFS Sampling frequency setting.

00 32-kHz

01 44.1-kHz

10 48-kHz

11 reserved

AFE+0028h AFE EDI Control Register AFE_EDI_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DIR	SRC	WCYCLE					FMT	EN
Type								R/W	R/W	R/W					R/W	R/W
Reset								0	0	01111					0	0

This register is used to control the EDI

EN Enable EDI. When EDI is disabled, EDI_DAT and EDI_WS hold low.

0 disable EDI

1 enable EDI

FMT EDI format

0 EIAJ

1 I2S

WCYCLE Clock cycle count in a word. Cycle count = WCYCLE + 1, and WCYCLE can be 15 or 31 only. Any other values result in an unpredictable error.

15 Cycle count is 16.

31 Cycle count is 32.

SRC I2S clock and WS signal source.

0 Internal mode. The clock and word select signals are fed to external device from AFE.

1 External mode. The clock and word select signals are fed externally from the connected device. There is a buffer control mechanism to deal with the clock mismatch between internal and external clocks.

DIR Serial data bit direction

0 Output mode. Audio data is fed out to the external device.

1 Input mode or recording mode. By this recording mechanism, DSP can do some post processing or voice memos.

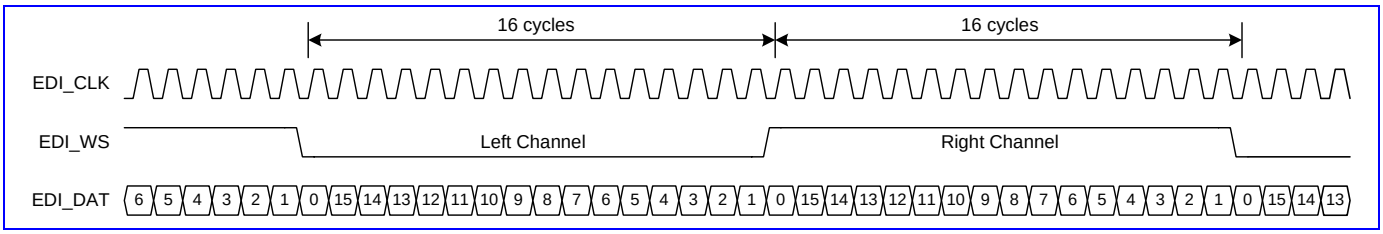


Figure 63 Cycle count is 16 for I2S format.

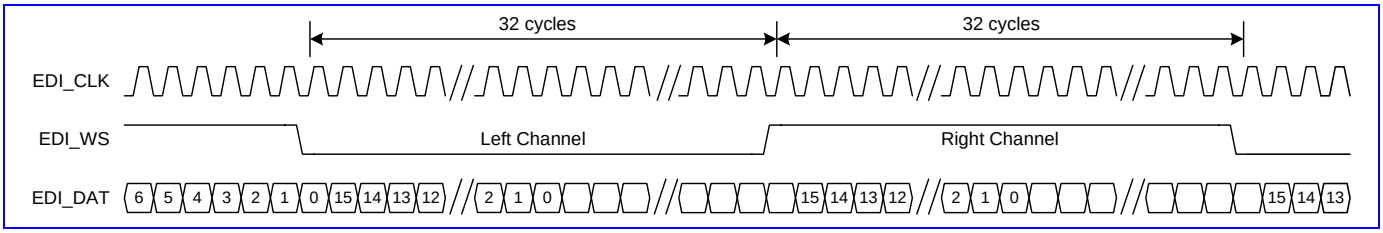


Figure 64 Cycle count is 32 for I2S format.

AFE+0030h Audio/Voice DAC SineWave Generator AFE_DAC_TEST

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VON	AON	MUTE			AMP_DIV			FREQ_DIV							
Type	R/W	R/W	R/W			R/W			R/W							

Reset	0	0	0			111	0000_0001

This register is only for analog design verification on audio/voice DACs.

VON Makes voice DAC output the test sine wave.

0 Voice DAC inputs are normal voice samples

1 Voice DAC inputs are sine waves

AON Makes audio DAC output the test sine wave.

0 Audio DAC inputs are normal audio samples

1 Audio DAC inputs are sine waves

MUTE Mute switch.

0 Turn on the sine wave output in this test mode.

1 Mute the sine wave output.

AMP_DIV Amplitude setting.

FREQ_DIV Frequency setting.

AFE+0034h Audio/Voice Interactive Mode Setting AFE_VAM_SET

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	A2V													PER_VAL		
Type	R/W													R/W		
Reset	0													101		

A2V Redirect audio interrupt to voice interrupt. In other words, replace voice interrupt by audio interrupt.

0 [voice interrupt / audio interrupt] → [voice / audio]

1 [audio interrupt / no interrupt] → [voice / audio]

PER_VAL Counter reset value for audio interrupt generation period setting. For example, by default, the setting = 5 causes interrupt per 6 L/R samples. Changing this value can change the rate of audio interrupt.

AFE+0040h~00F0h AFE Audio Equalizer Filter Coefficient Register AFE_EQCOEF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	A															
Type	WO															

Audio front-end provides a 45-tap equalizer filter. The filter is shown below.

DO = (A44 X DI44 + A43 X DI43 … + A1 X DI1 + A0 X DI0)/32768.

DIn is the input data, and An is the coefficient of the filter, which is a 16-bit 2's complement signed integer. DI0 is the last input data.

The coefficient cannot be programmed when the audio path is enabled, or unpredictable noise may be generated. If coefficient programming is necessary while the audio path is enabled, the audio path must be muted during programming. After programming is complete, the audio path is not to be resumed (unmated) for 100 sampling periods.

A Coefficient of the filter.

Address Offset	Coefficient	Address Offset	Coefficient	Address Offset	Coefficient
0040h	A0	007Ch	A15	00B8h	A30
0044h	A1	0080h	A16	00BCh	A31
0048h	A2	0084h	A17	00C0h	A32
004Ch	A3	0088h	A18	00C4h	A33
0050h	A4	008Ch	A19	00C8h	A34
0054h	A5	0090h	A20	00CCh	A35
0058h	A6	0094h	A21	00D0h	A36
005Ch	A7	0098h	A22	00D4h	A37
0060h	A8	009Ch	A23	00D8h	A38
0064h	A9	00A0h	A24	00DCh	A39
0068h	A10	00A4h	A25	00E0h	A40
006Ch	A11	00A8h	A26	00E4h	A41
0070h	A12	00Ach	A27	00E8h	A42
0074h	A13	00B0h	A28	00ECh	A43
0078h	A14	00B4h	A29	00F0h	A44

6.3 DSP Register Definitions

+0640hDSP AFE Voice Uplink Data Register 0 AFE_VUL_DAT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VUL_DAT0															
Type	RO															
Reset	0															

Voice band uplink transmission data register 0. The content of this register is updated by uplink digital filter outputs. This register is read by DSP in an 8K ISR.

+0641hDSP AFE Voice Uplink Data Register 1 AFE_VUL_DAT1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VUL_DAT1															
Type	RO															

Reset	0

Voice band uplink transmission data register 1. The content of this register is updated by uplink digital filter outputs. This register is read by DSP in an 8K ISR if VBYPASSIIR of AFE_LB_CON is set.

+0642hDSP AFE Voice Downlink Data Register 0 AFE_VDL_DAT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDL_DAT0															
Type	WO															
Reset	0															

Voice band downlink receiving data register 0. This register is written by DSP in an 8K ISR. The content of this register is used as downlink digital filter inputs.

+0643hDSP AFE Voice Downlink Data Register 1 AFE_VDL_DAT1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDL_DAT1															
Type	WO															
Reset	0															

Voice band downlink receiving data register 1. This register is written by DSP in an 8K ISR if VBYPASSIIR of AFE_VLB_CON is set. The content of this register is used as downlink digital filter inputs.

+0644hDSP AFE Voice DAI Bluetooth Transmission Data Register 0 AFE_VDBTX_DAT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDBTX_DAT0															
Type	WO															
Reset	0															

DAI Bluetooth transmission data register 0. This register is written by DSP in an 8K ISR if the Bluetooth function is turned on. The content of this register is shifted out to the Bluetooth interface.

+0645hDSP AFE Voice DAI Bluetooth Transmission Data Register 1 AFE_VDBTX_DAT1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDBTX_DAT 1															
Type	WO															
Reset	0															

DAI Bluetooth transmission data register 1. This register is written by DSP in an 8K ISR if the corresponding DAI test is set or the Bluetooth function is turned on. The content of this register is shifted out to the SS or Bluetooth interface.

+0646hDSP AFE Voice DAI Bluetooth Receiving Data Register 0 AFE_VDBRX_DAT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDBRX_DAT 0															
Type	RO															
Reset	0															

DAI Bluetooth receiving data register 0. This register is read by DSP in an 8K ISR if the Bluetooth function is turned on. The content of this register is shifted in from the Bluetooth interface.

+0647hDSP AFE Voice DAI Bluetooth Receiving Data Register 1 AFE_VDBRX_DAT1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDBRX_DAT 1															
Type	RO															
Reset	0															

DAI Bluetooth receiving data register 1. This register is read by DSP in an 8K ISR if the corresponding DAI test is set or the Bluetooth function is turned on. The content of this register is shifted in from the SS or Bluetooth module.

+0648hDSP AFE Voice DAI Bluetooth Control Register AFE_VDSP_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																VDSP_RDY
Type																R/W
Reset																0

DSP sets this register to inform hardware that it is ready for data transmission. In DAI test modes, DSP starts a test by setting vdsp_rdy when speech samples are required or are ready. In normal mode, the DSP asserts this bit to ungate the downlink path data. Otherwise, the downlink data remains zero.

VDSP_RDY Ready indication to start the voice band data path.

+0649hDSP AFE I2S Input Mode Buffer AFE_EDI_RDATA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDATA															
Type	RO															
Reset	0															

This is the register for reading I2S input data. For each audio interrupt, DSP should read 6 pairs (total 12 reads) of the input data. If DSP is reading too fast or too slow, there is a 2-word margin for repeating or dropping the samples that DSP read rate can not match-up with audio front end.

RDATA Read data port. Left channel first, and then right channel.

+064FhDSP AFE Audio Control Register AFE_ADSP_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															ARST_FIFO	ADSP_RDY
Type															R/W	R/W
Reset															0	0

DSP sets this register to inform hardware that it is ready for data transmission. DSP asserts this bit to ungate the audio path data. Otherwise, the audio path data remains zero.

ADSP_RDY Ready to ungate audio data path.

ARST_FIFO Reset the FIFO read/write pointers and the interrupt counter.

+0650hDSP AFE Audio Right-Channel Data Register 0 AFE_ARCH_DAT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARCH_DAT0															
Type	W															
Reset	0															

Audio right channel data register 0. The content of this register is used as the right channel digital filter inputs.

The frequency of audio interrupts varies with the audio sampling rate and bypass setting, and can be 1/6 the audio sampling rate, or 1/12 the sampling rate, or 1/24 the sampling rate. The frequency depends on the setting of BYPASS.

- BYPASS = 00b: 1/24 the sampling rate.
- BYPASS = 01b: 1/12 the sampling rate.
- BYPASS = 10b: 1/6 the sampling rate.
- BYPASS = 11b: 1/6 the sampling rate.

For DSP, 6 audio samples are written when an interrupt is received.

+0658hDSP AFE Audio Left-Channel Data Register 0 AFE_ALCH_DAT0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ALCH_DAT0															
Type	W															
Reset	0															

Audio left channel data register 0. The content of this register is used as the left channel digital filter inputs.

6.4 Programming Guide

Several cases – including speech call, voice memo record, voice memo playback, melody playback and DAI tests – requires that partial or the whole audio front-end be turned on.

The following are the recommended voice band path programming procedures to turn on audio front-end:

1. MCU programs the AFE_DAI_CON, AFE_LB_CON, AFE_VAG_CON, AFE_VAC_CON0, AFE_VAC_CON1 and AFE_VAPDN_CON registers for specific operation modes. Refer also to the analog chip interface specification.
2. MCU clears the VAFE bit of the PDN_CON2 register to ungate the clock for the voice band path. Refer to the software power down control specification.
3. MCU sets AFE_VMCU_CON to start operation of the voice band path.

The following are the recommended voice band path programming procedures to turn off audio front-end:

1. MCU programs AFE_VAPDN_CON to power down the voice band path analog blocks.
2. MCU clears AFE_VMCU_CON to stop operation of the voice band path.
3. MCU sets VAFE bit of PDN_CON2 register to gate the clock for the voice band path.

To start the DAI test, the MS first receives a GSM Layer 3 TEST_INTERFACE message from the SS and puts the speech transcoder into one of the following modes:

- Normal mode (VDAIMODE[1:0]: 00)
- Test of speech encoder/DTX functions (VDAIMODE[1:0]: 10)
- Test of speech decoder/DTX functions (VDAIMODE[1:0]: 01)
- Test of acoustic devices and A/D & D/A (VDAIMODE[1:0]: 11)

The MS then waits for DAIRST# signaling from the SS. Recognizing this, DSP starts to transmit to and/or receive from the DSP. For further details, refer to the GSM 11.10 specification.

The following are the recommended audio band path programming procedures to turn on audio front-end:

1. MCU programs the AFE_MCU_CON1, AFE_AAG_CON, AFE_AAC_CON, and AFE_AAPDN_CON registers for specific configurations. Refer also to the analog chip interface specification.
2. MCU clears the AAFE bit of the PDN_CON2 register to ungate the clock for the audio band path. Refer to the software power down control specification.
3. MCU sets AFE_AMCU_CON0 to start operation of the audio band path.

The following are the recommended audio band path programming procedures to turn off audio front-end:

1. MCU programs the AFE_AAPDN_CON to power down the audio band path analog blocks. Refer also to the analog block specification for further details.
2. MCU clears AFE_AMCU_CON0 to stop operation of the audio band path.
3. MCU sets the AAFE bit of the PDN_CON2 register to gate the clock for the audio band path.

7 Timing Generator

Timing is the most critical issue in GSM/GPRS applications. The TDMA timer provides a simple interface for the MCU to program all the timing-related events for receive event control, transmit event control and the timing adjustment. Detailed descriptions are mentioned in Section 7.1.

7.1 TDMA timer

The TDMA timer unit is composed of three major blocks: Quarter bit counter, Signal generator and Event registers.

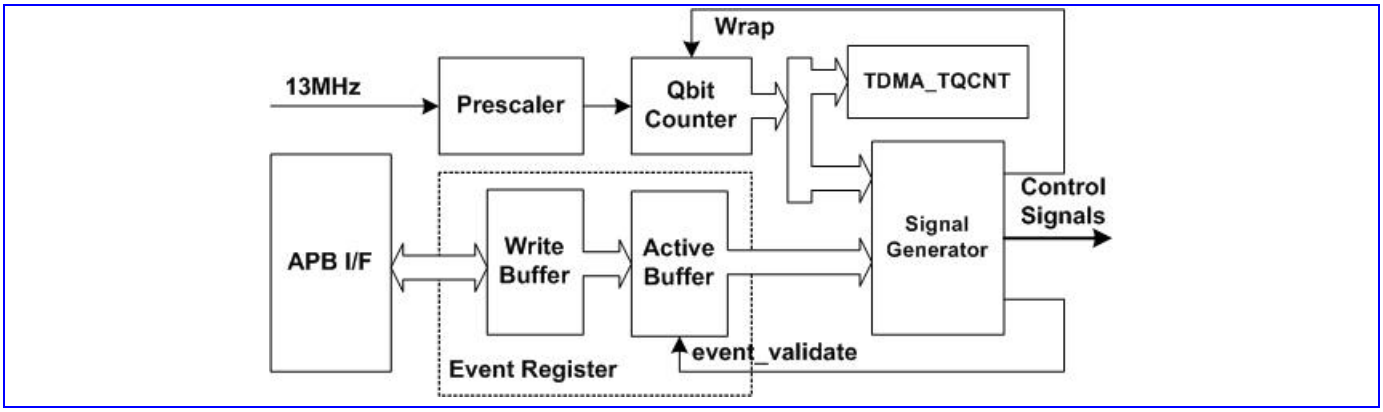


Figure 65 The block diagram of TDMA timer

By default, the quarter-bit counter continuously counts from 0 to the wrap position. In order to apply to cell synchronization and neighboring cell monitoring, the wrap position can be changed by the MCU to shorten or lengthen a TDMA frame. The wrap position is held in the TDMA_WRAP register and the current value of the TDMA quarter bit counter may be read by the MCU via the TDMA_TQCNT register.

The signal generator handles the overall comparing and event-generating processes. When a match has occurred between the quarter bit counter and the event register, a predefined control signal is generated. These control signals may be used for on-chip and off-chip purposes. Signals that change state more than once per frame make use of more than one event register.

The event registers are programmed to contain the quarter bit position of the event that is to occurr. The event registers are double buffered. The MCU writes into the first register, and the event TDMA_EVTVAL transfers the data from the write buffer to the active buffer, which is used by the signal generator for comparison with the quarter bit count. Caution: values in the active buffer is updated at the end of qbit count(TDMA_EVTVAL+1). Do not set the event time at this time (TDMA_EVTVAL+1). The TDMA_EVTVAL signal itself may be programmed at any quarter bit position. These event registers could be classified into four groups:

On-chip Control Events

TDMA_EVTVAL

This event allows the data values written by the MCU to pass through to the active buffers.

TDMA_WRAP

TDMA quarter bit counter wrap position. This sets the position at which the TDMA quarter bit counter resets back to zero. The default value is 4999, changing this value will advance or retard the timing events in the frame following the next TDMA_EVTVAL signal.

TDMA_DTIRQ

DSP TDMA interrupt requests. DTIRQ triggers the DSP to read the command from the MCU/DSP Shard RAM to schedule the activities that will be executed in the current frame.

TDMA_CTIRQ1/CTIRQ2

MCU TDMA interrupt requests.

TDMA_AUXADC [1:0]

This signal triggers the monitoring ADC to measure the voltage, current, temperature, device id etc..

TDMA_AFC [3:0]

This signal powers up the automatic frequency control DAC for a programmed duration after this event.

Note: For both MCU and DSP TDMA interrupt requests, these signals are all active Low during one quarter bit duration and they should be used as edge sensitive events by the respective interrupt controllers.

On-chip Receive Events

TDMA_BDLON [5:0]

These registers are a set of six which contain the quarter bit event that initiates the receive window assertion sequence which powers up and enables the receive ADC, and then enables loading of the receive data into the receive buffer.

TDMA_BDLOFF [5:0]

These registers are a set of six which contain the quarter bit event that initiates the receive window de-assertion sequence which disables loading of the receive data into the receive buffer, and then powers down the receive ADC.

TDMA_RXWIN[5:0]

DSP TDMA interrupt requests. TDMA_RXWIN is usually used to initiate the related RX processing including two modes. In single-shot mode, TDMA_RXWIN is generated when the BRXFS signal is de-asserted. In repetitive mode, TDMA_RXWIN will be generated both regularly with a specific interval after BRXFS signal is asserted and when the BRXFS signal is de-asserted.

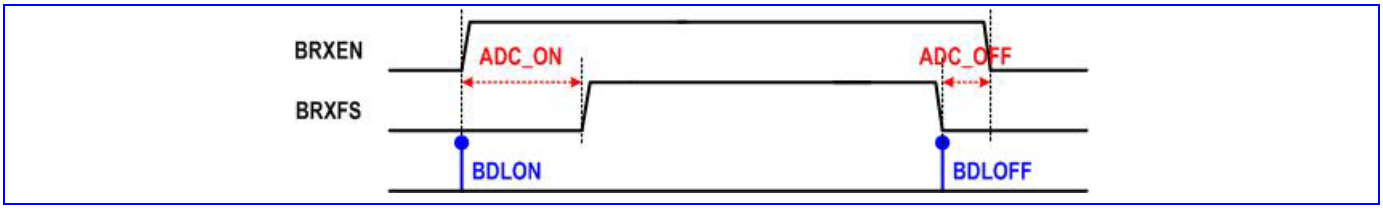


Figure 66 The timing diagram of BRXEN and BRXFS

Note: TDMA_BDLON/OFF event registers, together with TDMA_BDLCON register, generate the corresponding BRXEN and BRXFS window used to power up/down baseband downlink path and control the duration of data transmission to the DSP, respectively.

On-chip Transmit Events

TDMA_APC [6:0]

These registers initiate the loading of the transmit burst shaping values from the transmit burst shaping RAM into the transmit power control DAC.

TDMA_BULON [3:0]

This register contains the quarter bit event that initiates the transmit window assertion sequence which powers up the modulator DAC and then enables reading of bits from the transmit buffer into the GMSK modulator.

TDMA_BULOFF [3:0]

This register contains the quarter bit event that initiates the transmit window de-assertion sequence which disables the reading of bits from the transmit buffer into the GMSK modulator, and then power down the modulator DAC.

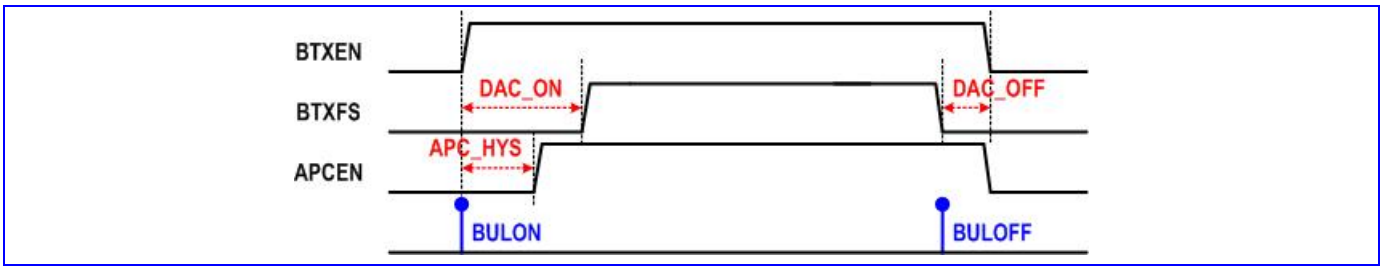


Figure 67 The timing diagram of BTXEN and BTXFS

Note: TDMA_BULON/OFF event registers, together with TDMA_BULCON1, TDMA_BULCON2 register, generate the corresponding BTXEN, BTXFS and APCEN window used to power up/down the baseband uplink path, control the duration of data transmission from the DSP and power up/down the APC DAC, respectively.

Off-chip Control Events

TDMA_BSI [19:0]

The quarter bit positions of these 20 BSI events are used to initiate the transfer of serial words to the transceiver and synthesizer for gain control and frequency adjustment.

TDMA_BPI [29:0]

The quarter bit positions of these 30 BPI events are used to generate changes of state on the output pins to control the external radio components.

7.1.1 Register Definitions

TDMA+0150h Event Enable Register 0 TDMA_EVTENA0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFC3	AFC2	AFC1	AFC0	BDL5	BDL4	BDL3	BDL2	BDL1	BDL0				CTIRQ2	CTIRQ1	DTIRQ
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0				0	0	0

DTIRQ Enable TDMA_DTIRQ

CTIRQ*n* Enable TDMA_CTIRQ*n*

AFC*n* Enable TDMA_AFC*n*

BDL*n* Enable TDMA_BDLON*n* and TDMA_BDLOFF*n*

For all these bits,

0 function is disabled

1 function is enabled

TDMA+0154h Event Enable Register 1 TDMA_EVTENA1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPRS				BUL3	BUL2	BUL1	BUL0		APC6	APC5	APC4	APC3	APC2	APC1	APC0
Type	R/W				R/W	R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0				0	0	0	0		0	0	0	0	0	0	0

APC*n* Enable TDMA_APC*n*

BUL*n* Enable TDMA_BULON*n* and TDMA_BULOFF*n*

For all these bits,

0 function is disabled

1 function is enabled

TDMA +0158h Event Enable Register 2 TDMA_EVTENA2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BSI15	BSI14	BSI13	BSI12	BSI11	BSI10	BSI9	BSI8	BSI7	BSI6	BSI5	BSI4	BSI3	BSI2	BSI1	BSI0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TDMA +015Ch Event Enable Register 3 TDMA_EVTENA3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BSI19	BSI18	BSI17	BSI16
Type													R/W	R/W	R/W	R/W
Reset													0	0	0	0

BSI*n* BSI event enable control

0 Disable TDMA_BSI*n*

1 Enable TDMA_BSI*n*

TDMA +0160h Event Enable Register 4 TDMA_EVTENA4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPI15	BPI14	BPI13	BPI12	BPI11	BPI10	BPI9	BPI8	BPI7	BPI6	BPI5	BPI4	BPI3	BPI2	BPI1	BPI0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TDMA +0164h Event Enable Register 5 TDMA_EVTENA5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BPI31	BPI30	BPI29	BPI28	BPI27	BPI26	BPI25	BPI24	BPI23	BPI22	BPI21	BPI20	BPI19	BPI18	BPI17	BPI16
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BPI*n* BPI event enable control

0 Disable TDMA_BPI*n*

1 Enable TDMA_BPI*n*

TDMA+0168h Event Enable Register 6 TDMA_EVTENA6

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							BPI41	BPI40	BPI39	BPI38	BPI37	BPI36	BPI35	BPI34	BPI33	BPI32
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset							0	0	0	0	0	0	0	0	0	0

BPI*n* BPI event enable control

0 Disable TDMA_BPI*n*

1 Enable TDMA_BPI*n*

TDMA+016Ch Event Enable Register 7 TDMA_EVTENA7

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															AUX1	AUX0
Type															R/W	R/W
Reset															0	0

AUX Auxiliary ADC event enable control

0 Disable Auxiliary ADC event

1 Enable Auxiliary ADC event

TDMA +0170h Qbit Timer Offset Control Register TDMA_WRAPOFS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															TOI[1:0]	
Type															R/W	
Reset															0	

TOI This register defines the value used to advance the Qbit timer in unit of 1/4 quarter bit; the timing advance will be take place as soon as the TDMA_EVTVAL is occurred, and it will be cleared automatically.

TDMA +0174h Qbit Timer Biasing Control Register TDMA_REGBIAS

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			TQ_BIAS[13:0]													
Type			R/W													
Reset			0													

TQ_BIAS This register defines the Qbit offset value which will be added to the registers being programmed. It only takes effects on AFC, BDLON/OFF, BULON/OFF, APC, AUXADC, BSI and BPI event registers.

TDMA +0180h DTX Control Register TDMA_DTXCON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DTX3	DTX2	DTX1	DTX0
Type													R/W	R/W	R/W	R/W

DTX DTX flag is used to disable the associated transmit signals

0 BULON0, BULOFF0, APC_EV0 & APC_EV1 are controlled by TDMA_EVTENA1 register

1 BULON0, BULOFF0, APC_EV0 & APC_EV1 are disabled

TDMA +0184h Receive Interrupt Control Register TDMA_RXCON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MOD5	MOD4	MOD3	MOD2	MOD1	MOD0	RXINTCNT[9:0]									
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W									

RXINTCNT TDMA_RXWIN interrupt generation interval in quarter bit unit

MOD*n* Mode of Receive Interrupts

0 Single shot mode for the corresponding receive window

1 Repetitive mode for the corresponding receive window

TDMA +0188h Baseband Downlink Control Register TDMA_BDLCON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_ON										ADC_OFF					
Type	R/W										R/W					

ADC_ON BRXEN to BRXFS setup up time in quarter bit unit.

ADC_OFF BRXEN to BRXFS hold up time in quarter bit unit.

TDMA +018Ch Baseband Uplink Control Register 1 TDMA_BULCON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DAC_ON								DAC_OFF							
Type	R/W								R/W							

DAC_ON BTXEN to BTXFS setup up time in quarter bit unit.

DAC_OFF BTXEN to BTXFS hold up time in quarter bit unit.

TDMA +0190h Baseband Uplink Control Register 2 TDMA_BULCON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									APC_HYS							
Type									R/W							

APC_HYS APCEN to BTXEN hysteresis time in quarter bit unit.

TDMA +0194h Frequency Burst Indication Register TDMA_FB_FLAG

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											FBDL5	FBDL4	FBDL3	FBDL2	FBDL1	FBDL0
Type											R/W	R/W	R/W	R/W	R/W	R/W

FBDLn Indication of frequency burst for RX window n

The register as a write buffer will be auto-cleared at the next event-validate and its value will be at the same time loaded to the active buffer. The exact FB indication comes from the active buffer and the corresponding mode in register TDMA_RXCON. When the indication is low, it will be updated according to TDMA_EVTVAL; otherwise, the value in the active buffer only depends TDMA_FB_CLRI and the falling edge of the corresponding RX window.

TDMA +0198h Direct Frequency Burst Closing TDMA_FB_CLRI

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																

Type																

As long as the register is selected, active buffer for TDMA_FB_FLAG will be reset then therefore the frequency burst indication will be forced to 0.

Address	Type	Width	Reset Value	Name	Description
+0000h	R	[13:0]	—	TDMA_TQCNT	Read quarter bit counter
+0004h	R/W	[13:0]	0x1387	TDMA_WRAP	Latched Qbit counter reset position
+0008h	R/W	[13:0]	0x1387	TDMA_WRAPIMD	Direct Qbit counter reset position
+000Ch	R/W	[13:0]	0x0000	TDMA_EVTVAL	Event latch position
+0010h	R/W	[13:0]	—	TDMA_DTIRQ	DSP software control
+0014h	R/W	[13:0]	—	TDMA_CTIRQ1	MCU software control 1
+0018h	R/W	[13:0]	—	TDMA_CTIRQ2	MCU software control 2
+0020h	R/W	[13:0]	—	TDMA_AFC0	The 1st AFC control
+0024h	R/W	[13:0]	—	TDMA_AFC1	The 2nd AFC control
+0028h	R/W	[13:0]	—	TDMA_AFC2	The 3rd AFC control
+002Ch	R/W	[13:0]	—	TDMA_AFC3	The 4th AFC control
+0030h	R/W	[13:0]	—	TDMA_BDLON0	Data serialization of the 1st RX block
+0034h	R/W	[13:0]	—	TDMA_BDLOFF0	
+0038h	R/W	[13:0]	—	TDMA_BDLON1	Data serialization of the 2nd RX block
+003Ch	R/W	[13:0]	—	TDMA_BDLOFF1	
+0040h	R/W	[13:0]	—	TDMA_BDLON2	Data serialization of the 3rd RX block
+0044h	R/W	[13:0]	—	TDMA_BDLOFF2	
+0048h	R/W	[13:0]	—	TDMA_BDLON3	Data serialization of the 4th RX block
+004Ch	R/W	[13:0]	—	TDMA_BDLOFF3	
+0050h	R/W	[13:0]	—	TDMA_BDLON4	Data serialization of the 5th RX block
+0054h	R/W	[13:0]	—	TDMA_BDLOFF4	
+0058h	R/W	[13:0]	—	TDMA_BDLON5	Data serialization of the 6th RX block
+005Ch	R/W	[13:0]	—	TDMA_BDLOFF5	
+0060h	R/W	[13:0]	—	TDMA_BULON0	Data serialization of the 1st TX slot
+0064h	R/W	[13:0]	—	TDMA_BULOFF0	

+0068h	R/W	[13:0]	—	TDMA_BULON1	Data serialization of the 2nd TX slot
+006Ch	R/W	[13:0]	—	TDMA_BULOFF1	
+0070h	R/W	[13:0]	—	TDMA_BULON2	Data serialization of the 3rd TX slot
+0074h	R/W	[13:0]	—	TDMA_BULOFF2	
+0078h	R/W	[13:0]	—	TDMA_BULON3	Data serialization of the 4th TX slot
+007Ch	R/W	[13:0]	—	TDMA_BULOFF3	
+0090h	R/W	[13:0]	—	TDMA_APC0	The 1st APC control
+0094h	R/W	[13:0]	—	TDMA_APC1	The 2nd APC control
+0098h	R/W	[13:0]	—	TDMA_APC2	The 3rd APC control
+009Ch	R/W	[13:0]	—	TDMA_APC3	The 4th APC control
+00A0h	R/W	[13:0]	—	TDMA_APC4	The 5th APC control
+00A4h	R/W	[13:0]	—	TDMA_APC5	The 6th APC control
+00A8h	R/W	[13:0]	—	TDMA_APC6	The 7th APC control
+00B0h	R/W	[13:0]	—	TDMA_BSI0	BSI event 0
+00B4h	R/W	[13:0]	—	TDMA_BSI1	BSI event 1
+00B8h	R/W	[13:0]	—	TDMA_BSI2	BSI event 2
+00BCh	R/W	[13:0]	—	TDMA_BSI3	BSI event 3
+00C0h	R/W	[13:0]	—	TDMA_BSI4	BSI event 4
+00C4h	R/W	[13:0]	—	TDMA_BSI5	BSI event 5
+00C8h	R/W	[13:0]	—	TDMA_BSI6	BSI event 6
+00CCh	R/W	[13:0]	—	TDMA_BSI7	BSI event 7
+00D0h	R/W	[13:0]	—	TDMA_BSI8	BSI event 8
+00D4h	R/W	[13:0]	—	TDMA_BSI9	BSI event 9
+00D8h	R/W	[13:0]	—	TDMA_BSI10	BSI event 10
+00DCh	R/W	[13:0]	—	TDMA_BSI11	BSI event 11
+00E0h	R/W	[13:0]	—	TDMA_BSI12	BSI event 12
+00E4h	R/W	[13:0]	—	TDMA_BSI13	BSI event 13
+00E8h	R/W	[13:0]	—	TDMA_BSI14	BSI event 14
+00ECh	R/W	[13:0]	—	TDMA_BSI15	BSI event 15

+00F0h	R/W	[13:0]	—	TDMA_BSI16	BSI event 16
+00F4h	R/W	[13:0]	—	TDMA_BSI17	BSI event 17
+00F8h	R/W	[13:0]	—	TDMA_BSI18	BSI event 18
+00FCh	R/W	[13:0]	—	TDMA_BSI19	BSI event 19
+0100h	R/W	[13:0]	—	TDMA_BPI0	BPI event 0
+0104h	R/W	[13:0]	—	TDMA_BPI1	BPI event 1
+0108h	R/W	[13:0]	—	TDMA_BPI2	BPI event 2
+010Ch	R/W	[13:0]	—	TDMA_BPI3	BPI event 3
+0110h	R/W	[13:0]	—	TDMA_BPI4	BPI event 4
+0114h	R/W	[13:0]	—	TDMA_BPI5	BPI event 5
+0118h	R/W	[13:0]	—	TDMA_BPI6	BPI event 6
+011Ch	R/W	[13:0]	—	TDMA_BPI7	BPI event 7
+0120h	R/W	[13:0]	—	TDMA_BPI8	BPI event 8
+0124h	R/W	[13:0]	—	TDMA_BPI9	BPI event 9
+0128h	R/W	[13:0]	—	TDMA_BPI10	BPI event 10
+012Ch	R/W	[13:0]	—	TDMA_BPI11	BPI event 11
+0130h	R/W	[13:0]	—	TDMA_BPI12	BPI event 12
+0134h	R/W	[13:0]	—	TDMA_BPI13	BPI event 13
+0138h	R/W	[13:0]	—	TDMA_BPI14	BPI event 14
+013Ch	R/W	[13:0]	—	TDMA_BPI15	BPI event 15
+0140h	R/W	[13:0]	—	TDMA_BPI16	BPI event 16
+0144h	R/W	[13:0]	—	TDMA_BPI17	BPI event 17
+0148h	R/W	[13:0]	—	TDMA_BPI18	BPI event 18
+014Ch	R/W	[13:0]	—	TDMA_BPI19	BPI event 19
+01A0h	R/W	[13:0]	—	TDMA_BPI20	BPI event 20
+01A4h	R/W	[13:0]	—	TDMA_BPI21	BPI event 21
+01A8h	R/W	[13:0]	—	TDMA_BPI22	BPI event 22
+01ACh	R/W	[13:0]	—	TDMA_BPI23	BPI event 23
+01B0h	R/W	[13:0]	—	TDMA_BPI24	BPI event 24

+01B4h	R/W	[13:0]	—	TDMA_BPI25	BPI event 25
+01B8h	R/W	[13:0]	—	TDMA_BPI26	BPI event 26
+01BCh	R/W	[13:0]	—	TDMA_BPI27	BPI event 27
+01C0h	R/W	[13:0]	—	TDMA_BPI28	BPI event 28
+01C4h	R/W	[13:0]	—	TDMA_BPI29	BPI event 29
+01C8h	R/W	[13:0]	—	TDMA_BPI30	BPI event 30
+01CCh	R/W	[13:0]	—	TDMA_BPI31	BPI event 31
+01D0h	R/W	[13:0]	—	TDMA_BPI32	BPI event 32
+01D4h	R/W	[13:0]	—	TDMA_BPI33	BPI event 33
+01D8h	R/W	[13:0]	—	TDMA_BPI34	BPI event 34
+01DCh	R/W	[13:0]	—	TDMA_BPI35	BPI event 35
+01E0h	R/W	[13:0]	—	TDMA_BPI36	BPI event 36
+01E4h	R/W	[13:0]	—	TDMA_BPI37	BPI event 37
+01E8h	R/W	[13:0]	—	TDMA_BPI38	BPI event 38
+01ECh	R/W	[13:0]	—	TDMA_BPI39	BPI event 39
+01F0h	R/W	[13:0]	—	TDMA_BPI40	BPI event 40
+01F4h	R/W	[13:0]	—	TDMA_BPI41	BPI event 41
+0400h	R/W	[13:0]	—	TDMA_AUXEV0	Auxiliary ADC event 0
+0404h	R/W	[13:0]	—	TDMA_AUXEV1	Auxiliary ADC event 1
+0150h	R/W	[15:0]	0x0000	TDMA_EVTENA0	Event Enable Control 0
+0154h	R/W	[15:0]	0x0000	TDMA_EVTENA1	Event Enable Control 1
+0158h	R/W	[15:0]	0x0000	TDMA_EVTENA2	Event Enable Control 2
+015Ch	R/W	[3:0]	0x0000	TDMA_EVTENA3	Event Enable Control 3
+0160h	R/W	[15:0]	0x0000	TDMA_EVTENA4	Event Enable Control 4
+0164h	R/W	[13:0]	0x0000	TDMA_EVTENA5	Event Enable Control 5
+0168h	R/W	[1:0]	0x0000	TDMA_EVTENA6	Event Enable Control 6
+016Ch	R/W	[11:0]	0x0000	TDMA_EVTENA7	Event Enable Control 7
+0170h	R/W	[1:0]	0x0000	TDMA_WRAPOFS	TQ Counter Offset Control Register
+0174h	R/W	[13:0]	0x0000	TDMA_REGBIAS	Biasing Control Register

+0180h	R/W	[3:0]	—	TDMA_DTXCON	DTX Control Register
+0184h	R/W	[15:0]	—	TDMA_RXCON	Receive Interrupt Control Register
+0188h	R/W	[15:0]	—	TDMA_BDLCON	Downlink Control Register
+018Ch	R/W	[15:0]	—	TDMA_BULCON1	Uplink Control Register 1
+0190h	R/W	[7:0]	—	TDMA_BULCON2	Uplink Control Register 2
+0194h	R/W	[5:0]	—	TDMA_FB_FLAG	FB indicator
+0198h	W		—	TDMA_FB_CLRI	Direct clear of FB indicator

Table 35 TDMA Timer Register Map

7.2 Slow Clocking Unit

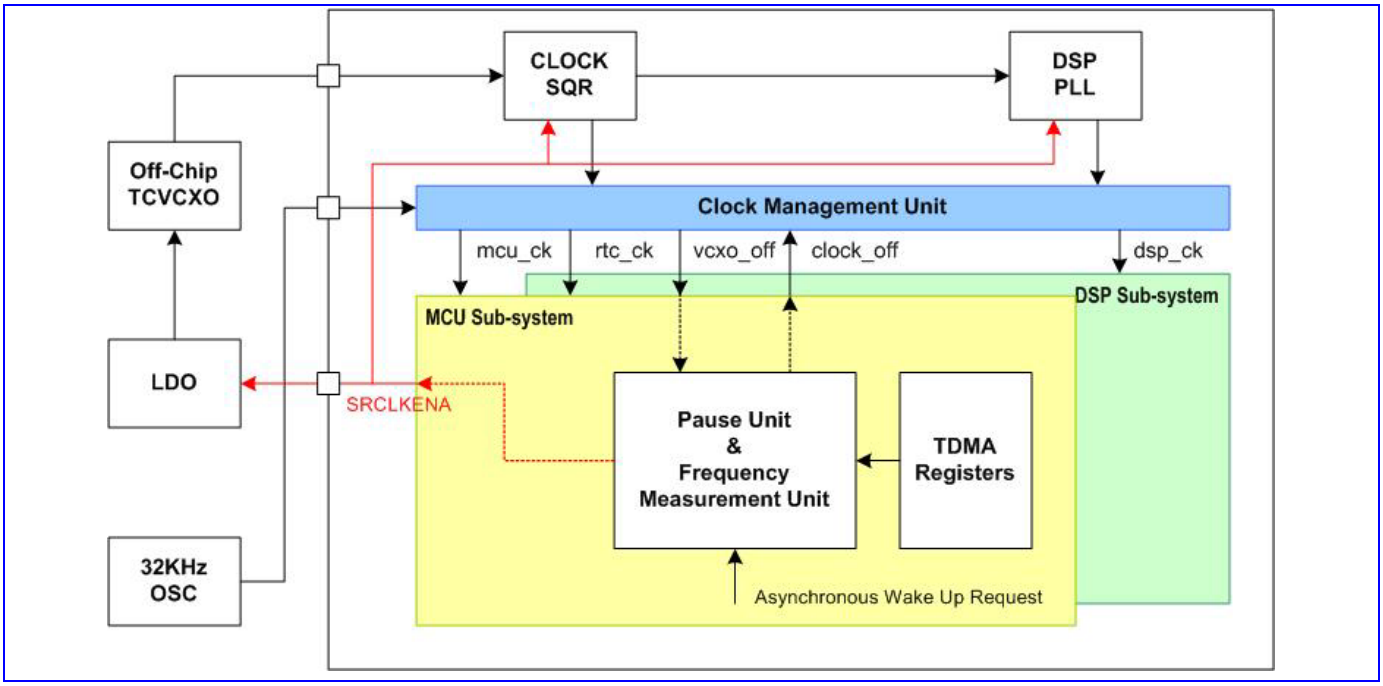


Figure 68 The block diagram of the slow clocking unit

The slow clocking unit is provided to maintain the synchronization to the base-station timing using a 32KHz crystal oscillator while the 13MHz reference clock is switched off. As shown in Figure 68, this unit is composed of frequency measurement unit, pause unit, and clock management unit.

Because of the inaccuracy of the 32KHz oscillator, a frequency measurement unit is provided to calibrate the 32KHz crystal taking the accurate 13MHz source as the reference. The calibration procedure always takes place prior to the pause period.

The pause unit is used to initiate and terminate the pause mode procedure and it also works as a coarse time-base during the pause period.

The clock management unit is used to control the system clock while switching between the normal mode and the pause mode. SRCLKENA is used to turn on/off the clock squarer, DSP PLL and off-chip TCVCXO. CLOCK_OFF signal is used for gating the main MCU and DSP clock, and VCXO_OFF is used as the acknowledgement signal of the CLOCK_OFF

request.

7.2.1 Register Definitions

TDMA +0218h Slow clocking unit control register SM_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE_START	FM_START
Type															W	W
Reset															0	0

FM_START Initiate the frequency measurement procedure

PAUSE_START Initiate the pause mode procedure at the next timer wrap position

TDMA +021Ch Slow clocking unit status register SM_STA

Bit	15	14	13	12	11	10	9	8
Name								PAUSE_ABORT
Type								R
Bit	7	6	5	4	3	2	1	0
Name	SETTLE_CPL	PAUSE_CPL	PAUSE_INT	PAUSE_RQST			FM_CPL	FM_RQST
Type	R	R	R	R			R	R

FM_RQST Frequency measurement procedure is requested

FM_CPL Frequency measurement procedure is completed

PAUSE_RQST Pause mode procedure is requested

PAUSE_INT Asynchronous wake up from pause mode

PAUSE_CPL Pause period is completed

SETTLE_CPL Settling period is completed

PAUSE_ABORT Pause mode is aborted because of the reception of interrupt prior to entering pause mode

TDMA +022Ch Slow clocking unit configuration register SM_CNF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RTC	EINT	KP	SM	FM
Type												R/W	R/W	R/W	R/W	R/W
Reset												0	0	0	1	1

FM Enable interrupt generation upon completion of frequency measurement procedure

SM Enable interrupt generation upon completion of pause mode procedure

KP Enable asynchronous wake-up from pause mode by key press

EINT Enable asynchronous wake-up from pause mode by external interrupt

RTC Enable asynchronous wake-up from pause mode by real time clock interrupt

TDMA +0300h Power-down indication of DSP ROM DSPROMPD

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PD_11	PD_10	PD_9	PD_8	PD_7	PD_6	PD_5	PD_4	PD_3	PD_2	PD_1	PD_0
Type					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset					0	0	0	0	0	0	0	0	0	0	0	0

PD_X Power-down indication of page X of DSP CM ROM, X = 0:5

0 power down disabled

1 power down enabled

PD_X Power-down indication of page X of DSP PM ROM, X = 10:6

0 power down disabled

1 power down enabled

The register is for controlling the VIA-ROM, in which a reset signal is required whenever the ROM is waked up from power-down mode. It means that as long as MCU plans to interrupt DSP from slow idle, the register should be programmed in advance by 15us, and otherwise the read data would be unknown. The reason why totally 12 pages are programmable is reserved for future use, by which MCU can dynamically wake-up the pages those shall be accessed. However, by now MCU can just simply program the register to all one's or all zero's. In view of the hardware, the 12 bits are ANDED as a power-down indication. As the indication turns from high to low, a counter will be triggered to account for 15-us interval according to the MCU clock, then a negative pulse will be generated as the ROM reset.

Address	Type	Width	Reset Value	Name	Description
+0200h	R/W	[2:0]	—	SM_PAUSE_M	MSB of pause duration
+0204h	R/W	[15:0]	—	SM_PAUSE_L	16 LSB of pause duration
+0208h	R/W	[13:0]	—	SM_CLK_SETTLE	Off-chip VCXO settling duration
+020Ch	R	[2:0]	—	SM_FINAL_PAUSE_M	MSB of final pause count
+0210h	R	[15:0]	—	SM_FINAL_PAUSE_L	16 LSB of final pause count
+0214h	R	[13:0]	—	SM_QBIT_START	TQ_ COUNT value at the start of the pause
+0218h	W	[1:0]	0x0000	SM_CON	SM control register

+021Ch	R	[7:3,1:0]	0x0000	SM_STA	SM status register
+0220h	R/W	[15:0]	—	SM_FM_DURATION	32KHz measurement duration
+0224h	R	[9:0]	—	SM_FM_RESULT_M	10 MSB of frequency measurement result
+0228h	R	[15:0]	—	SM_FM_RESULT_L	16 LSB of frequency measurement result
+022Ch	R/W	[4:0]	0x0000	SM_CNF	SM configuration register
+0230	R	[23:0]	0x000000	RTCCOUNT	RTC count
+0300h	R/W	[11:0]	0x0000	DSPROMPD	DSP ROM power donw

8 Power and Clocks

8.1 Software Power Down Control

In addition to Pause Mode capability during Standby State, the software program can also put each peripheral independently into Power Down Mode during Active State by gating off their clock. The typical logic implementation is depicted as in **Figure 69**. For all of the configuration bits, 1 means that the function is in Power Down Mode and 0 means that it is in the Active Mode.

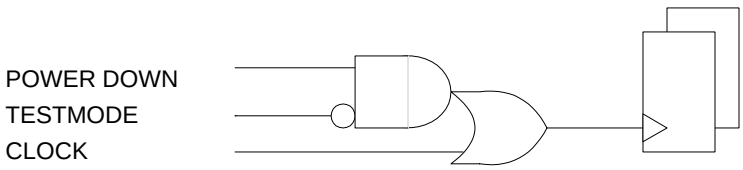


Figure 69 Power Down Control at Block Level

8.1.1 Register Definitions

CONFG+300h Power Down Control 0 Register PDN_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DSP_DIV2		PLL	MCU_DIV2	CLKSQ					IRDMA			WAVETABLE	GCU		DMA
Type	R/W		R/W	R/W	R/W					R/W			R/W	R/W		R/W
Reset	1		1	1	0					1			1	1		1

DMA Controls the DMA Controller Power Down

GCU Controls the GCU Controller Power Down

WAVETABLE Controls the DSP Wave-Table DMA Power Down

CLKSQ Controls the Clock squarer Power Down

MCU_DIV2 Controls the MUC DIV2 Power Down

PLL Controls the PLL Power Down

DSP_DIV2 Controls the DSP DIV2 Power Down

CONFG +304h Power Down Control 1 Register PDN_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		UART3			SWDBG	PWM2		UART2	LCD	ALTER	PWM	SIM	UART1	GPIO	KP	GPT
Type		R/W			R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		1			1	1		1	1	1	1	1	0	1	1	1

GPT Controls the General Purpose Timer Power Down

KP Controls the Keypad Scanner Power Down

GPIO Controls the GPIO Power Down

UART1 Controls the UART1 Controller Power Down

SIM Controls the SIM Controller Power Down

PWM Controls the PWM Generator Power Down

ALTER Controls the Alerter Generator Power Down

LCD Controls the LCD Controller Power Down

UART2 Controls the UART2 Controller Power Down

PWM2 Controls the PWM2 Generator Power Down

SWDBG Controls the SWDBG Generator Power Down

UART3 Controls the UART3 Controller Power Down

CONFG +308h Power Down Control 2 Register PDN_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMSK	BBRX	I2C	AAFE	DIV	GCC	BFE	VAFE	AUXAD	FCS	APC	AFC	BPI	BSI	RTC	TDMA
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

TDMA Controls the TDMA Power Down

RTC Controls the RTC Power Down

BSI Controls the BSI Power Down. This control will not be updated until both tdma_evtval and qbit_en are asserted.

BPI Controls the BPI Power Down. This control will not be updated until both tdma_evtval and qbit_en are asserted.

AFC Controls the AFC Power Down. This control will not be updated until both tdma_evtval and qbit_en are asserted.

APC Controls the APC Power Down. This control will not be updated until both tdma_evtval and qbit_en are asserted.

FCS Controls the FCS Power Down

AUXAD Controls the AUX ADC Power Down

VAFE Controls the Audio Front End of VBI Power Down

BFE Controls the Base-Band Front End Power Down

GCU Controls the GCU Power Down

DIV Controls the Divider Power Down

AAFE Controls the Audio Front End of MP3 Power Down

I2C Controls the I2C Power Down

BBRX Controls the BB RX Power Down

GMSK Controls the GMSK Power Down

CONFG +30Ch Power Down Control 3 Register PDN_CON3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ICE
Type																R/W
Reset																1

ICE Enables the debug feature of the ARM7EJS core. It controls the DBGEN pin of the ICEBreaker.

CONFG+0310h Power Down Set 0 Register PDN_SET0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DSP_DIV2		PLL	MCU_DIV2	CLKSQ					IRDMA			WAVETABLE	GCU		DMA
Type	W1S		W1S	W1S	W1S					W1S	W1S		W1S	W1S		W1S

CONFG+0314h Power Down Set 1 Register PDN_SET1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		UART3			TRC	PWM2		UART2	LCD	ALTER	PWM1	SIM	UART1	GPIO	KP	GPT
Type		W1S			W1S	W1S		W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S

CONFG+0318h Power Down Set 2 Register PDN_SET2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMSK	BBRX	I2C	AAFE	DIV	GCC	BFE	VAFE	AUXAD	FCS	APC	AFC	BPI	BSI	RTC	TDMA
Type	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S

CONFG+031Ch Power Down Set 3 Register PDN_SET3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ICE
Type																W1S

These registers are used to individually set power down control bit. Only the bits set to 1 are in effect. Setting the bits to 1 also sets the corresponding power down control bits will to 1. Otherwise, the bits keep their original value.

EACH BIT Set the Associated Power Down Control Bit to 1.

0 no effect

1 Set corresponding bit to 1

CONFG+0320h Power Down Clear 0 Register PDN_CLR0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DSP_DIV2		PLL	MCU_DIV2	CLKSQ					IRDMA			WAVETABLE	GCU		DMA
Type	W1C		W1C	W1C	W1C					W1C			W1C	W1C		W1C

CONFG+0324h Power Down Clear 1 Register PDN_CLR1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		UART3			TRC	PWM2		UART2	LCD	ALTER	PWM1	SIM	UART1	GPIO	KP	GPT
Type		W1C			W1C	W1C		W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C

CONFG+0328h Power Down Clear 2 Register PDN_CLR2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMSK	BBRX	SCCB	AAFE	DIV	GCC	BFE	VAFE	AUXAD	FCS	APC	AFC	BPI	BSI	RTC	TDMA
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C

CONFG+032Ch Power Down Clear 3 Register PDN_CLR3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																ICE
Type																W1C

These registers are used to individually clear power down control bit. Only the bits set to 1 are in effect. Setting the bits to 1 also sets the corresponding power down control bits to 0. Otherwise, the bits keep their original value.

EACH BIT Clear the Associated Power Down Control Bit.

0 no effect

1 Set corresponding bit to 0

CONFG+0200h Debug-mode Select IDN_SEL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TDMA_IDN	CLKSQ_IDN			PLL_IDN
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PLL_IDN Enable PLL power-on no matter what SRLKENA(from TDMA timer) is

0 Disable debug mode

1 Enable debug mode

CLKSQ_IDN Enable CLKSQ power-on no matter what SRLKENA(from TDMA timer) is

0 Disable debug mode

1 Enable debug mode

TDMA_IDN Enable TDMA debug message output. The debug mode should go accompanied with appropriate GPIO setting

0 Disable debug mode

1 Enable debug mode

CONFG+0114h Sleep Control SLEEP_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													PDN_DSP2	PDN_DSP1	AHB_SLEEP	MCU_SLEEP
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MCU_SLEEP_REQUEST Power down AHB cycles launched by MCU

0 no effect

1 sleep request

AHB_SLEEP_REQUEST Force AHB for sleep mode

0 no effect

1 sleep request

PDN_DSP1 Turn off host DSP's clock

PDN_DSP2 Turn off slave DSP's clock

CONFG+0110h Software Misc. usage, low byte SW_MISC_L

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SW_MISC_L															
Type	R/W															
Reset	0															

CONFG+0114h Software Misc. usage, high byte SW_MISC_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SW_MISC_H															
Type	R/W															
Reset	0															

8.2 Clocks

There are two major time bases in the MT6223. For the faster one is the 13 MHz clock originating from an off-chip temperature-compensated voltage controlled oscillator (TCVCXO) that can be either 13MHz or 26MHz. This signal is the input from the SYSCLK pad then is converted to the square-wave signal. The other time base is the 32768 Hz clock generated by an on-chip oscillator connected to an external crystal. **Figure 70** shows the clock sources as well as their utilizations inside the chip.

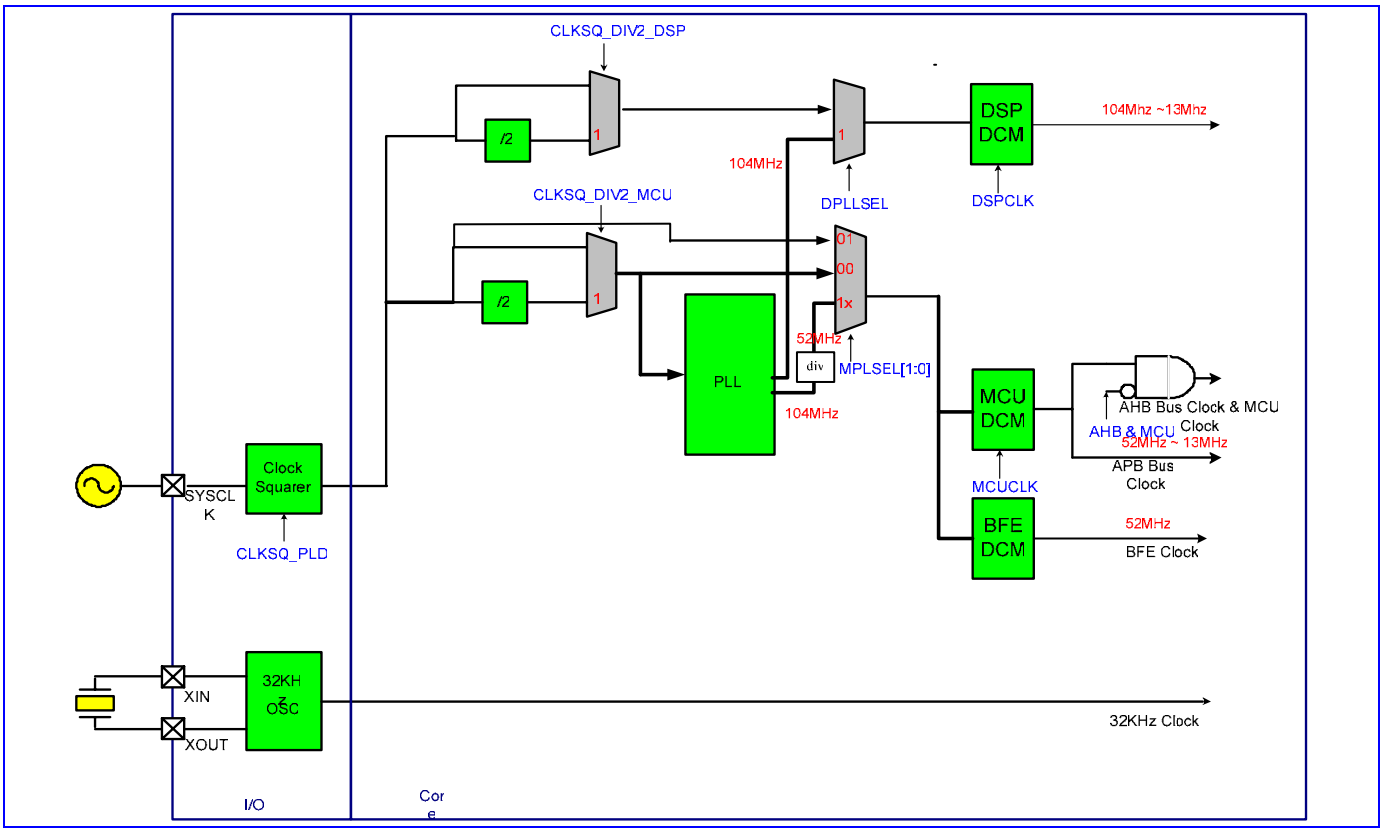


Figure 70 Clock distributions inside the MT6223.

8.2.1 32.768 KHz Time Base

The 32768 Hz clock is always running. It's mainly used as the time base of the Real Time Clock (RTC) module, which maintains time and date with counters. Therefore, both the 32768Hz oscillator and the RTC module is powered by separate voltage supplies that shall not be powered down when the other supplies do.

In low power mode, the 13 MHz time base is turned off, so the 32768 Hz clock shall be employed to update the critical TDMA timer and Watchdog Timer. This time base is also used to clocks the keypad scanner logic.

8.2.2 13 MHz Time Base

One 1/2-dividers for PLL existing to allow using 26 or 13 MHz TCVCXO.
One phase-locked loops (PLL) to generate 624Mhz clock output, then a frequency divider futher divide 6, 6, 13 to generate 104Mhz, 104Mhz, 48Mhz for three primary clocks, DSP_CLOCK, MCU_CLOCK and USB_CLOCK, respectively. This three primary clocks then feed to DSP Clock Domain and MCU Clock Domain and USB, respectively. The PLL require no off-chip components for operations and can be turn off in order to save power. After power-on, the PLLs are off by default and the source clock signal is selected through multiplexers. The software shall take cares of the PLL lock time while changing the clock selections. The PLL and usages are listed below.

- **PLL** supplies two clock source
- DSP system clock, *DSP_CLOCK*. The outputted 104MHz clock is connected to DSP DCM (dynamic clock manager) for dynamically adjusting clock rate by digital clock divider.
- MCU system clock, *MCU_CLOCK*, which paces the operations of the MCU cores, MCU memory system, and MCU peripherals as well. The outputted 52MHz clock is connected to ARM DCM and MCU DCM for dynamically adjusting clock rate by digital clock divider.

Note that PLL need some time to become stable after being powered up. The software shall take cares of the PLL lock time before switching them to the proper frequency. Usually, a software loop longer than the PLL lock time is employed to deal with the problem.
For power management, the MCU software program may stop MCU Clock by setting the Sleep Control Register. Any interrupt requests to MCU can pause the sleep mode, and thus MCU return to the running mode.
AHB also can be stop by setting the Sleep Control Register. However the behavior of AHB in sleep mode is a little different from that of MCU. After entering Sleep Mode, it can be temporarily waken up by any “hreq” (bus request), and then goes back to sleep automatically after all “hreqs” de-assert. Any transactions can take place as usual in sleep mode, and it can save power while there is no transaction on it. However the penalty is losing a little system efficiency for switching on and off bus clock, but the impact is small.

8.2.3 Dynamic Clock Switch of MCU Clock

Dynamic Clock Manager is implemented to allow MCU and DSP switching clock dynamically without any jitter, and enabling signal drift, and system can operate stably during any clock rate switch.
Please note that PLL must be enabled and the frequency shall be set as 624MHz, therefore the required MCU/DSP/USB clocks can be generated from 624MHz. Before switching to 52MHz clock rate, the clock from PLL DIV2 will feed through dynamic clock manager (DCM) directly. That means if PLL DIV2 is enabled, the internal clock rate is the half of SYSCLK. Contrarily, the internal clock rate is identical to SYSCLK.
However, the settings of some hardware modules is required to be changed before or after clock rate change. Software has the responsibility to change them at proper timing. The following table is list of hardware modules needed to be changed their setting during clock rate change.

Module Name	Programming Sequence
EMI	Low clock speed -> high clock speed Changing wait state before clock change. New wait state will not take effect until current EMI access is complete. Software should insert a period of time before switching clock. High clock speed -> low clock speed Changing wait state after clock change.
LCD	Change wait state while LCD in IDLE state.

Table 36 Programming sequence during clock switch

8.2.4 Register Definitions

CONFG+0100h PLL Frequency Register PLL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIV_CTRL			CALI					RST	UPLLSEL	DPLLSEL	MPLLSEL		PLLTME	PLLVCOSEL	
Type	R/W			R/W					R/W	R/W	R/W	R/W		R/W	R/W	
Reset	2			0					0	0	0	0		0	00	

PLLVCOSEL Selects VCO in PLL frequency for PLL debug purpose. Default value is 0x0.

PLLTME PLL test mode Enable

0 Disable

1 Enables

MPLLSEL Select MCU Clock source. Using this mux to gate out unstable clock output from PLL after system boot up

00 PLL bypassed, using CLK from CLKSQ, default value after chip power up.

01 PLL bypassed, using CLK from SYSCLK

10 Using PLL Clock for MCU

11 Reserved

DPLLSEL Select DSP Clock source. Using this mux to gate out unstable clock output from PLL after system boot up

0 PLL bypassed, using CLK from CLKSQ

1 Using PLL Clock for DSP

~~UPLLSEL Select USB Clock source. Using this mux to gate out unstable clock output from PLL after system boot up~~

~~0 PLL bypassed, using CLK from CLKSQ~~

~~1 Using PLL Clock for USB~~

RST Reset Control of PLL

0 Normal Operation

1 Reset the PLL

CALI Calibration Control for PLL

DIV_CTRL Control the frequency of the PLL output, PLL output operates at (DIV_CTRL + 2) x 13MHz

CONFG+110h Clock Control Register CLK_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLKSQ_TME											DSP_EXTCK	USB_EXTCK	CLKSQ_PLD	CLKSQ_DIV2_MCU	CLKSQ_DIV2_DSP
Type	R/W											R/W	R/W	R/W	R/W	R/W
Reset	0											0	0	0	0	0

CLKSQ_DIV2_DSP Control the clock divider for DSP clock domain

0 Divider bypassed

1 Divider not bypassed

CLKSQ_DIV2_MCU Control the x2 clock divider for MCU clock domain

0 Divider bypassed

1 Divider not bypassed

CLKSQ_PLD Pull Down Control

0 Disable

1 Enables

~~USB_EXTCK Use external USB clock source.~~

~~0 Not use external clock.~~

~~1 Use external clock.~~

DSP_EXTCK Use external DSP clock source.

0 Not use external clock.

1 Use external clock.

CLKSQ_TME CLKSQ test-mode enable

0 test mode disable

1 test mode enable

CONFG+114h Sleep Control Register SLEEP_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SLAVE DSP	HOSTD SP	AHB	MCU
Type													WO	WO	WO	WO
Reset													0	0	0	0

MCU Stop the MCU Clock to force MCU Processor entering sleep mode. MCU clock will be resumed as long as there comes an interrupt request or system is reset.

0 MCU Clock is running

1 MCU Clock is stopped

AHB Stop the AHB Bus Clock to force the entire bus entering sleep mode. AHB clock will be resumed as long as there comes an interrupt request or system is reset.

0 AHB Bus Clock is running

1 AHB Bus Clock is stopped

HOST/SLAVE DSP Stop the DSP Clock.

0 DSP Bus Clock is running

1 DSP Bus Clock is stopped

CONFG+0118h MCU Clock Control Register MCUCLK_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ARM_FSEL				SRCCLK				MCU_FSEL			
Type					R/W				R/W				R/W			
Reset					3				1				3			

MCU_FSEL MCU clock frequency selection. This control register is used to control the output clock frequency of MCU Dynamic Clock Manager. The clock frequency is from 13MHz to 52MHz. The waveform of the output clock is shown in Fig. **71.**

0 13MHz

1 26MHz

2 39MHz

3 52MHz

Others reserved

When MCU Clock Source bypass PLL (MPLL_SEL[1]==0), the output frequency is controlled by SRCCLK ,CLKSQ_DIV2_MCU , MPLL_SEL[0] and MCU_FSEL[0]

SRCCLK	CLKSQ_DIV2_MCU	MPLL_SEL[0]	MCU_FSEL[0]	
0	**0**	**x**	**x**	13Mhz
1	**1**	**0**	**0**	13Mhz
1	**1**	**1**	**1**	26Mhz

Other illegal

SRCCLK off-chip temperature-compensated voltage controlled oscillator (TCVCXO) frequency identifier.

0 13MHz

1 26MHz

ARM_FSEL ARM clock frequency selection. This control register is used to control the output clock frequency of ARM Dynamic Clock Manager. The clock frequency is from 13MHz to 104MHz.

0 13MHz

1 26MHz

2 39MHz

3 52MHz

~~4 65MHz~~

~~5 78MHz~~

~~6 91MHz~~

~~7 104MHz~~

Others reserved

Please note that the clock period of 39MHz is not uniform. The shortest period of 39MHz clock is the same as the period of 52MHz. As a result, the wait states of external interfaces, such as EMI, NAND, and so on, have to be configured based on 52MHz timing. Therefore, the MCU performance executing in external memory at 39MHz may be worse than at 26MHz. 65Mhz, 78MHz and 91MHz are not uniform clocks, either.
Also note that the maximum latency of clock switch is 8 104MHz-clock periods. Software provides at least 8T locking time after clock switch command.

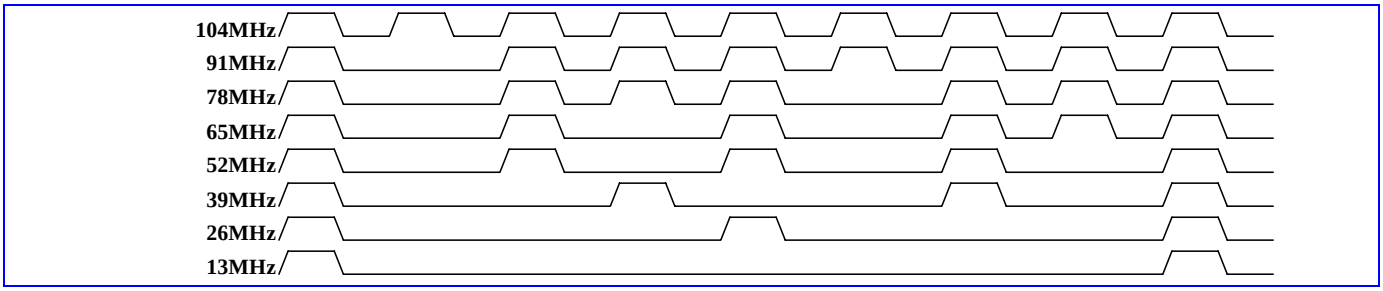


Figure 72 Output of Dynamic Clock Manager

CONFG+011Ch DSP Clock Control Register DSPCLK_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DSP1_FSEL				DSP1_FSEL			
Type									R/W				R/W			
Reset									3				3			

DSP_FSEL DSP clock frequency selection. This control register is used to control the output clock frequency of DSP Dynamic Clock Managers. The clock frequency is from 13MHz to 104MHz. Note that 39MHz, 65MHz, 78MHz, and 91MHz are not a uniform period clock rate.

0 13MHz

1 26MHz

2 39MHz

3 52MHz

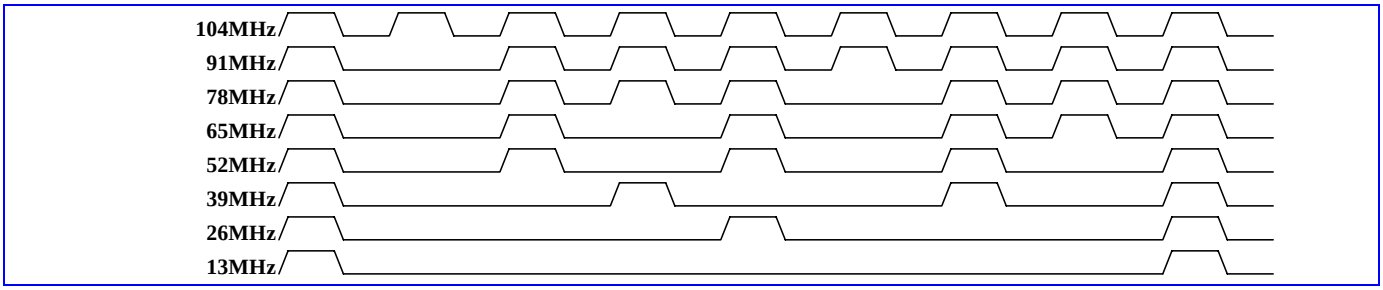
4 65MHz

5 78MHz

6 91MHz

7 104MHz

Others reserved



8.3 Reset Generation Unit (RGU)

Figure 73 shows the reset scheme used in MT6223. MT6223 provides three kinds of resets: hardware reset, watchdog reset, and software reset.

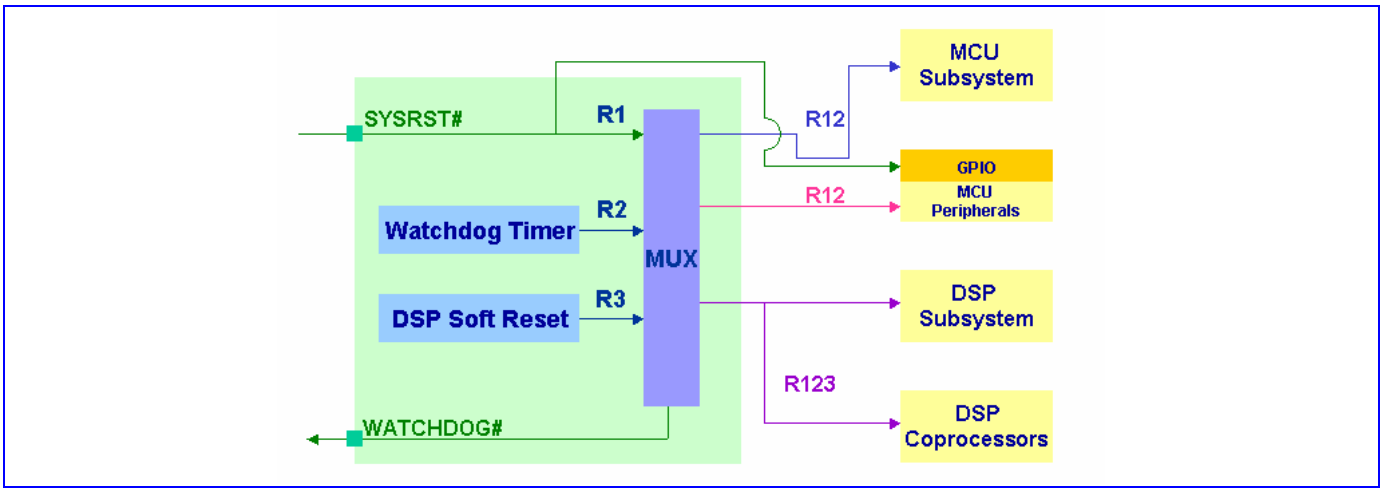


Figure 73 Reset Scheme Used in MT6223

8.3.1 General Description

8.3.1.1 Hardware Reset

This reset is input through the SYSRST# pin, which is driven low during power-on. The hardware reset has a global effect on the chip: all digital and analog circuits are initialized, except the Real Time Clock module. The initial states of the MT6223 sub-blocks are as follows:.

- All analog circuits are turned off.
- All PLLs are turned off and bypassed. The 13 MHz system clock is the default time base.
- Special trap states in GPIO.

8.3.1.2 Watchdog Reset

A watchdog reset is generated when the Watchdog Timer expires: the MCU software failed to re-program the timer counter in time. This situation is typically induced by abnormal software execution, which can be aborted by a hardwired watchdog reset. Hardware blocks that are affected by the watchdog reset are:

- MCU subsystem,
- DSP subsystem, and
- External components (trigged by software).

8.3.1.3 Software Resets

Software resets are local reset signals that initialize specific hardware components. For example, if hardware failures are

detected, the MCU or DSP software may write to software reset trigger registers to reset those specific hardware modules to their initial states.
The following modules have software resets.

- DSP Core
- DSP Coprocessors

8.3.2 Register Definitions

RGU +0000h Watchdog Timer Control Register WDT_MODE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY[7:0]											AUTO-RESTART	IRQ	EXTEN	EXTPOL	ENABLE
Type												R/W	R/W	R/W	R/W	R/W
Reset												0	0	0	0	1

ENABLE Enables the Watchdog Timer.

0 Disables the Watchdog Timer.

1 Enables the Watchdog Timer.

EXTPOL Defines the polarity of the external watchdog pin.

0 Active low.

1 Active high.

EXTEN Specifies whether or not to generate an external watchdog reset signal.

0 The watchdog does not generate an external watchdog reset signal.

1 If the watchdog counter reaches zero, an external watchdog signal is generated.

IRQ Issues an interrupt instead of a Watchdog Timer reset. For debug purposes, RGU issues an interrupt to the MCU instead of resetting the system.

0 Disable.

1 Enable.

AUTO-RESTART Restarts the Watchdog Timer counter with the value of WDT_LENGTH while task ID is written into Software Debug Unit.

0 Disable. The counter restarts by writing KEY into the WDT_RESTART register.

1 Enable. The counter restarts by writing KEY into the WDT_RESTART register or by writing task ID into the software debug unit.

KEY Write access is allowed if KEY=0x22.

RGU +0004h Watchdog Time-Out Interval Register WDT_LENGTH

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TIMEOUT[10:0]											KEY[4:0]				
Type	WO															
Reset	111_1111_1111b															

KEY Write access is allowed if KEY=08h.

TIMEOUT The counter is restarted with {TIMEOUT [10:0], 1_1111_1111b}. Thus the Watchdog Timer time-out period is a multiple of $512*T_{32k}$=15.6ms.

RGU +0008h Watchdog Timer Restart Register WDT_RESTART

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY[15:0]															
Type																
Reset																

KEY Restart the counter if KEY=1971h.

RGU +000Ch Watchdog Timer Status Register WDT_STA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDT	SW_WDT														
Type	RO	RO														
Reset	0	0														

WDT Indicates the cause of the watchdog reset.

0 Reset not due to Watchdog Timer.

1 Reset because the Watchdog Timer time-out period expired.

SW_WDT Indicates if the watchdog was triggered by software.

0 Reset not due to software-triggered Watchdog Timer.

1 Reset due to software-triggered Watchdog Timer.

NOTE: A system reset does not affect this register. This bit is cleared when the WTU_MODE register ENABLE bit is written.

RGU +0010h CPU Peripheral Software Reset Register SW_PERIPH_RSTN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DAMRST	USBRST						KEY							
Type		R/W	R/W													
Reset		0	0													

KEY Write access is allowed if KEY=37h.

DMARST Reset the DMA peripheral.

0 No reset.

1 Invoke a reset.

USBRST Reset the USB.

0 No reset.

1 Invoke a reset.

RGU +0014h DSP Software Reset Register SW_DSP_RSTN

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RST															
Type	R/W															
Reset	0															

RST Controls the DSP System Reset Control.

0 No reset.

1 Invoke a reset.

RGU +0018h Watchdog Timer Reset Signal Duration Register WDT_RSTINTREVAL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					LENGTH[11:0]											
Type					R/W											
Reset					FFFh											

LENGTH This register indicates the reset duration when Watchdog Timer times out. However, if the WDT_MODE register IRQ bit is set to 1, an interrupt is issued instead of a reset.

RGU+001Ch Watchdog Timer Software Reset Register WDT_SWRST

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY[15:0]															
Type																
Reset																

Software-triggered Watchdog Timer reset. If the register content matches the KEY, a watchdog reset is issued. However, if the WDT_MODE register IRQ bit is set to 1, an interrupt is issued instead of a reset.

KEY 1209h

9 Analog Front-end & Analog Blocks

9.1 General Description

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface translates APB bus write and read cycle for specific addresses related to analog front-end control. During writing or reading of any of these control registers, there is a latency associated with transferring of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. The Analog Blocks includes the following analog function for complete GSM/GPRS base-band signal processing:

1. *Base-band RX*: For I/Q channels base-band A/D conversion
2. *Base-band TX*: For I/Q channels base-band D/A conversion and smoothing filtering, DC level shifting
3. *RF Control*: Two DACs for automatic power control (APC) and automatic frequency control (AFC) are included. Their outputs are provided to external RF power amplifier and VCXO), respectively.
4. *Auxiliary ADC*: Providing an ADC for battery and other auxiliary analog function monitoring
5. *Audio mixed-signal blocks:* It provides complete analog voice signal processing including microphone amplification, A/D conversion, D/A conversion, earphone driver, and etc. Besides, dedicated stereo D/A conversion and amplification for audio signals are included).
6. *Clock Generation*: A clock squarer for shaping system clock, and two PLLs that provide clock signals to DSP, MCU units.
7. *XOSC32*: It is a 32-KHz crystal oscillator circuit for RTC application Analog Block Descriptions

9.1.1 BBRX

9.1.1.1 Block Descriptions

The receiver (RX) performs base-band I/Q channels downlink analog-to-digital conversion:

1. *Analog input multiplexer:* For each channel, a 4-input multiplexer that supports offset and gain calibration is included.
2. *A/D converter:* Two 14-bit sigma-delta ADCs perform I/Q digitization for further digital signal processing.

9.1.1.2 Functional Specifications

The functional specifications of the base-band downlink receiver are listed in the following table.

Symbol	Parameter	Min	Typical	Max	Unit
N	Resolution		14		Bit
FC	Clock Rate		26		MHz
FS	Output Sampling Rate		13/12		MSPS
	Input Swing				

	When GAIN='0' When GAIN='1'		0.8*AVDD 0.4*AVDD		Vpk Vpk
OE	Offset Error		+/- 10		mV
FSE	Full Swing Error		+/- 30		mV
	I/Q Gain Mismatch			0.5	dB
SINAD	Signal to Noise and Distortion Ratio - 45kHz sine wave in [0:90] kHz bandwidth - 145kHz sine wave in [10:190] kHz bandwidth	 65 65			 dB dB
ICN	Idle channel noise - [0:90] kHz bandwidth - [10:190] kHz bandwidth			 -74 -70	 dB dB
DR	Dynamic Range - [0:90] kHz bandwidth - [10:190] kHz bandwidth	 74 70			 dB dB
RIN	Input Resistance	75			kΩ
DVDD	Digital Power Supply	1.6	1.8	2.0	V
AVDD	Analog Power Supply	2.5	2.8	3.1	V
T	Operating Temperature	-20		80	℃
	Current Consumption Power-up Power-Down		 5 5		 mA μA

Table 37 Base-band Downlink Specifications

9.1.2 BBTX

9.1.2.1 Block Descriptions

The transmitter (TX) performs base-band I/Q channels up-link digital-to-analog conversion. Each channel includes:

1. *10-Bits D/A Converter:* It converts digital GMSK modulated signals to analog domain. The input to the DAC is sampled at 4.33-MHz rate with 10-bits resolution.
2. *Smoothing Filter:* The low-pass filter performs smoothing function for DAC output signals with a 350-kHz 2nd-order Butterworth frequency response.

9.1.2.2 Function Specifications

The functional specifications of the base-band uplink transmitter are listed in the following table.

Symbol	Parameter	Min	Typical	Max	Unit
N	Resolution		10		Bit
FS	Sampling Rate		4.33		MSPS
SINAD	Signal to Noise and Distortion Ratio	57	60		dB
	Output Swing	0.18*AVDD		0.89*AVDD	V
VOCM	Output CM Voltage	0.34*AVDD	0.5*AVDD	0.62*AVDD	V
	Output Capacitance			20	PF
	Output Resistance	10			KΩ
DNL	Differential Nonlinearity		+/- 0.5		LSB
INL	Integral Nonlinearity		+/- 1.0		LSB
OE	Offset Error		+/- 15		mV
FSE	Full Swing Error		+/- 30		mV
FCUT	Filter –3dB Cutoff Frequency	300	350	400	KHz
ATT	Filter Attenuation at 100-KHz 270-KHz 4.33-MHz	 0.1 2.2 46.4	 0.0 1.3 43.7	 0.0 0.8 41.4	 dB dB dB
	I/Q Gain Mismatch		+/- 0.5		dB
	I/Q Gain Mismatch Correction Range	-1.18		+1.18	dB
DVDD	Digital Power Supply	1.6	1.8	2.0	V
AVDD	Analog Power Supply	2.5	2.8	3.1	V
T	Operating Temperature	-20		80	℃
	Current Consumption Power-up Power-Down		 5 5		 mA μA

Table 38 Base-band Uplink Transmitter Specifications

9.1.3 AFC-DAC

9.1.3.1 Block Descriptions

As shown in the following figure, together with a 2nd-oder digital sigma-delta modulator, AFC-DAC is designed to produce a single-ended output signal at AFC pin. AFC pin should be connected to an external 1st-order R-C low pass filter to meet the 13-bits resolution (DNL) requirement[1].

The AFC_BYP pin is the mid-tap of a resistor divider inside the chip to offer the AFC output common-mode level. Nominal value of this common-mode voltage is half the analog power supply, and typical value of output impedance of AFC_BYP pin is about 21kΩ. To suppress the noise on common mode level, it is suggested to add an external capacitance between AFC_BYP pin and ground. The value of the bypass capacitor should be chosen as large as possible but still meet the settling time requirement set by overall AFC algorithm[2].

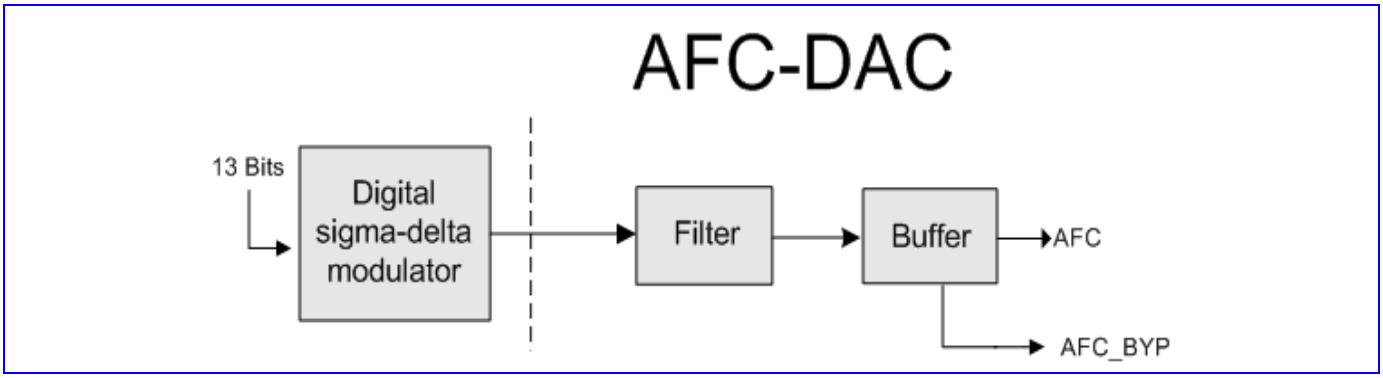


Figure 74 Block diagram of AFC-DAC

9.1.3.2 Functional Specifications

The following table gives the electrical specification of AFC-DAC.

Symbol	Parameter	Min	Typical	Max	Unit
N	Resolution		13		Bit
FS	Sampling Rate		6500		KHz
DVDD	Digital Power Supply	1.6	1.8	2.0	V
AVDD	Analog Power Supply	2.6	2.8	3.1	V
T	Operating Temperature	-20		80	℃

[1] DNL performance depends on external output RC filter bandwidth: the narrower the bandwidth, the better the DNL. Thus, there exists a tradeoff between output setting speed and DNL performance

[2] AFC_BYP output impedance and bypass capacitance determine the common-mode settling RC time constant. Insufficient common-mode settling will affect the INL performance. A typical value of 1nF is suggested.

	Current Consumption Power-up Power-Down		1.2	 1	 mA µA
	Output Swing		0.75*AVDD		V
	Output Resistor (in AFC output RC network)	1			KΩ
DNL	Differential Nonlinearity		+1/-1		LSB
INL	Integral Nonlinearity		+4.0/-4.0		LSB

Table 39 Functional specification of AFC-DAC

9.1.4 APC-DAC

9.1.4.1 Block Descriptions

The APC-DAC is a 10-bits DAC with output buffer aimed for automatic power control. Here blow are its analog pin assignment and functional specification tables.

9.1.4.2 Function Specifications

Symbol	Parameter	Min	Typical	Max	Unit
N	Resolution		10		Bit
FS	Sampling Rate			1.0833	MSPS
SINAD	Signal to Noise and Distortion Ratio (10-KHz Sine with 1.0V Swing & 100-KHz BW)		50		dB
	99% Settling Time (Full Swing on Maximal Capacitance)			5	µS
	Output Swing			AVDD-0.2	V
	Output Capacitance			200	pF
	Output Resistance	10			KΩ
DNL	Differential Nonlinearity		+/- 0.5		LSB
INL	Integral Nonlinearity		+/- 1.0		LSB
OE	Offset Error		+/- 10		mV
FSE	Full Swing Error		+/- 10		mV
DVDD	Digital Power Supply	1.6	1.8	2.0	V
AVDD	Analog Power Supply	2.5	2.8	3.1	V
T	Operating Temperature	-20		80	℃

	Current Consumption Power-up Power-Down		 600 1		 µA µA

Table 40 APC-DAC Specifications

9.1.5 Auxiliary ADC

9.1.5.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

1. *Analog Multiplexer:* The analog multiplexer selects signal from one of the seven auxiliary input pins. Real word message to be monitored, like temperature, should be transferred to the voltage domain.
2. *10 bits A/D Converter:* The ADC converts the multiplexed input signal to 10-bit digital data.

9.1.5.2 Function Specifications

The functional specifications of the auxiliary ADC are listed in the following table.

Symbol	Parameter	Min	Typical	Max	Unit
N	Resolution		10		Bit
FC	Clock Rate	0.1	1.0833	5	MHz
FS	Sampling Rate @ N-Bit			5/(N+1)	MSPS
	Input Swing	1.0		AVDD	V
VREFP	Positive Reference Voltage (Defined by AUX_REF pin)	1.0		AVDD	V
CIN	Input Capacitance Unselected Channel Selected Channel			 50 1.2	 fF pF
RIN	Input Resistance Unselected Channel Selected Channel	 10 1.8			 MΩ MΩ
RS	Resistor String Between AUX_REF pin & ground Power Up Power Down	 35 10	 50	 65	 KΩ MΩ
	Clock Latency		11		1/FC
DNL	Differential Nonlinearity		+0.5/-0.5		LSB

INL	Integral Nonlinearity		+1.0/-1.0		LSB
OE	Offset Error		+/- 10		mV
FSE	Full Swing Error		+/- 10		mV
SINAD	Signal to Noise and Distortion Ratio (10-KHz Full Swing Input & 13-MHz Clock Rate)		50		dB
DVDD	Digital Power Supply	1.6	1.8	2.0	V
AVDD	Analog Power Supply	2.5	2.8	3.1	V
T	Operating Temperature	-20		80	℃
	Current Consumption Power-up Power-Down		 300 1		 µA µA

Table 41 The Functional specification of Auxiliary ADC

9.1.6 Audio mixed-signal blocks

9.1.6.1 Block Descriptions

Audio mixed-signal blocks (AMB) integrate complete voice uplink/downlink and audio playback functions. As shown in the following figure, it includes mainly three parts. The first consists of stereo audio DACs and speaker amplifiers for audio playback. The second is the voice downlink path, including voice-band DACs and amplifiers, which produces voice signal to earphone or other auxiliary output device. Amplifiers in these two blocks are equipped with multiplexers to accept signals from internal audio/voice or external radio sources. The last is the voice uplink path, which is the interface between microphone (or other auxiliary input device) input and MT6223 DSP. A set of bias voltage is provided for external electret microphone..

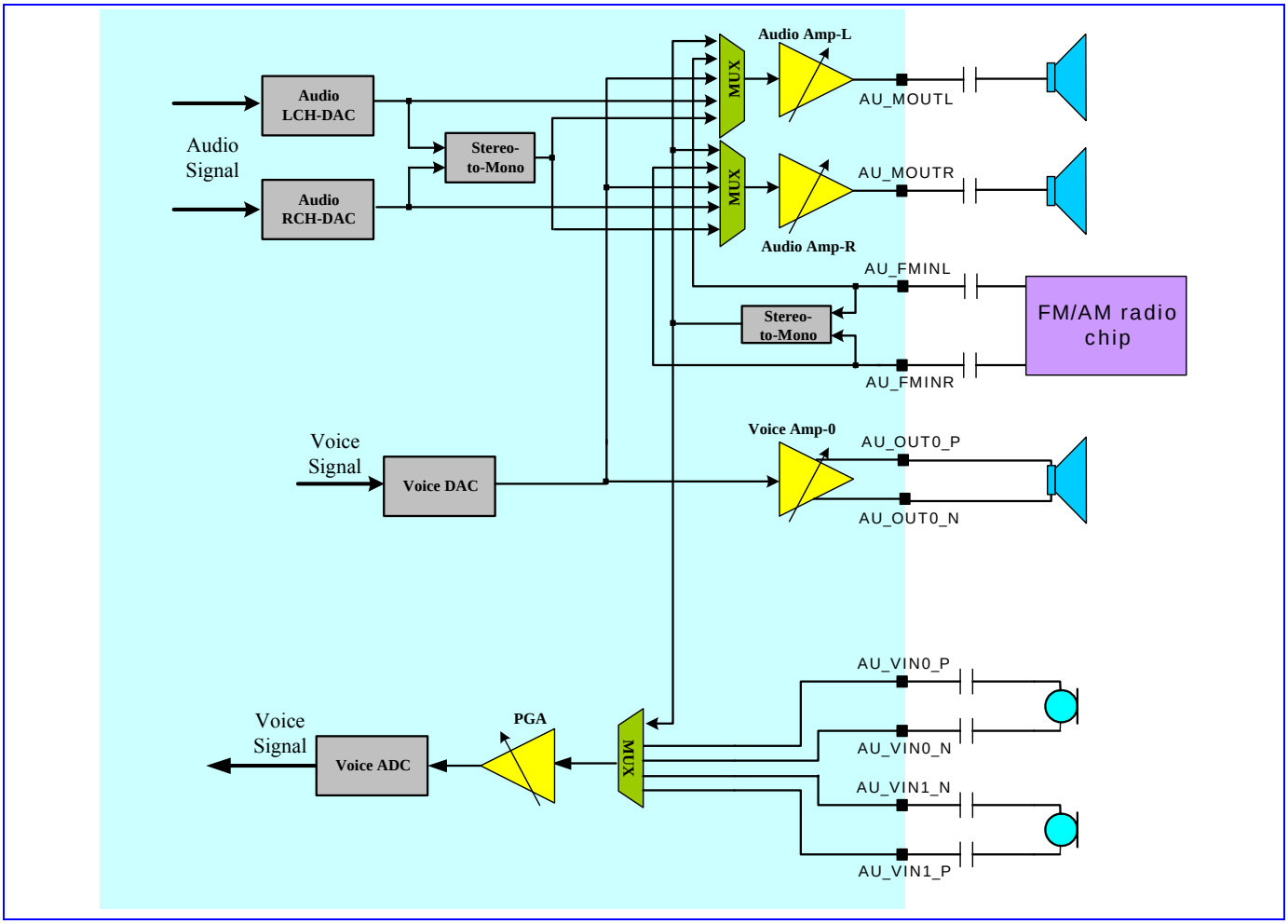


Figure 75 Block diagram of audio mixed-signal blocks.

9.1.6.2 Functional Specifications

The following table gives functional specifications of voice-band uplink/downlink blocks.

Symbol	Parameter	Min	Typical	Max	Unit
FS	Sampling Rate		4096		KHz
CREF	Decoupling Cap Between AU_VREF_P And AU_VREF_N		47		NF
DVDD	Digital Power Supply	1.6	1.8	2.0	V
AVDD	Analog Power Supply	2.5	2.8	3.1	V
T	Operating Temperature	-20		80	℃
IDC	Current Consumption		5		mA
VMIC	Microphone Biasing Voltage		1.9		V
IMIC	Current Draw From Microphone Bias			2	mA

	Pins				
Uplink Path[3]					
SINAD	Signal to Noise and Distortion Ratio Input Level: -40 dbm0 Input Level: 0 dbm0	29	 69		 dB dB
RIN	Input Impedance (Differential)	13	20	27	KΩ
ICN	Idle Channel Noise			-67	dBm0
XT	Crosstalk Level			-66	dBm0
Downlink Path[4]					
SINAD	Signal to Noise and Distortion Ratio Input Level: -40 dBm0 Input Level: 0 dBm0	29	 69		 dB dB
RLOAD	Output Resistor Load (Differential)	28			Ω
CLOAD	Output Capacitor Load			200	pF
ICN	Idle Channel Noise of Transmit Path			-67	dBm0
XT	Crosstalk Level on Transmit Path			-66	dBm0

Table 42 Functional specifications of analog voice blocks

Functional specifications of the audio blocks are described in the following.

Symbol	Parameter	Min	Typical	Max	Unit
FCK	Clock Frequency		Fs*128		KHz
Fs	Sampling Rate	32	44.1	48	KHz
AVDD	Power Supply	2.6	2.8	3.1	V
T	Operating Temperature	-20		80	℃
IDC	Current Consumption		5		mA
PSNR	Peak Signal to Noise Ratio		80		dB

[3] For uplink-path, not all gain setting of VUPG meets the specification listed on table, especially for the several highest gains. The maximum gain that meets the specification is to be determined.

[4] For downlink-path, not all gain setting of VDPG meets the specification listed on table, especially for the several lowest gains. The minimum gain that meets the specification is to be determined.

DR	Dynamic Range		80		dB
VOUT	Output Swing for 0dBFS Input Level		0.85		Vrms
THD	Total Harmonic Distortion 45mW at 16 Ω Load 22mW at 32 Ω Load			 -40 -60	 dB dB
RLOAD	Output Resistor Load (Single-Ended)	16			Ω
CLOAD	Output Capacitor Load			200	pF
XT	L-R Channel Cross Talk			TBD	dB

Table 43 Functional specifications of the analog audio blocks

9.1.7 Clock Squarer

9.1.7.1 Block Descriptions

For most VCXO, the output clock waveform is sinusoidal with too small amplitude (about several hundred mV) to make MT6223 digital circuits function well. Clock squarer is designed to convert such a small signal to a rail-to-rail clock signal with excellent duty-cycle. It provides also a pull-down function when the circuit is powered-down.

9.1.7.2 Function Specifications

The functional specification of clock squarer is shown in Table 44.

Symbol	Parameter	Min	Typical	Max	Unit
Fin	Input Clock Frequency		13		MHz
Fout	Output Clock Frequency		13		MHz
Vin	Input Signal Amplitude		500	AVDD	mVpp
DcycIN	Input Signal Duty Cycle		50		%
DcycOUT	Output Signal Duty Cycle	DcycIN-5		DcycIN+5	%
TR	Rise Time on Pin CLKSQOUT			5	ns/pF
TF	Fall Time on Pin CLKSQOUT			5	ns/pF
DVDD	Digital Power Supply	1.3	1.5	1.7	V
AVDD	Analog Power Supply	2.5	2.8	3.1	V
T	Operating Temperature	-20		80	℃
	Current Consumption		TBD		MA

Table 44 The Functional Specification of Clock Squarer

9.1.7.3 Application Notes

Here below in the figure is an equivalent circuit of the clock squarer. Please be noted that the clock squarer is designed to accept a sinusoidal input signal. If the input signal is not sinusoidal, its harmonic distortion should be low enough to not produce a wrong clock output. As an reference, for a 13MHz sinusoidal signal input with amplitude of 0.2V the harmonic distortion should be smaller than 0.02V.

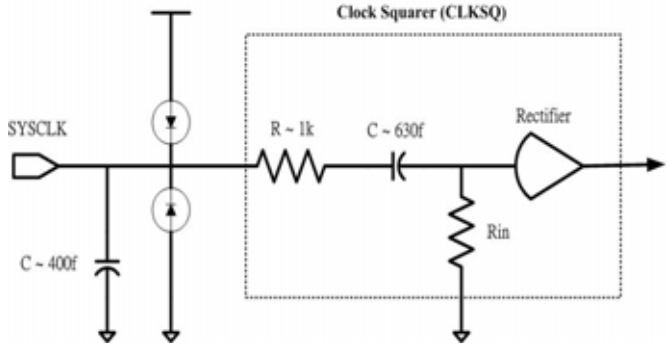


Figure 76 Equivalent circuit of Clock Squarer.

9.1.8 Phase Locked Loop

9.1.8.1 Block Descriptions

MT6223 includes two PLLs: DSP PLL and MCU PLL. DSP PLL and MCU PLL are identical and programmable to provide 104MHz and 52MHz output clock while accepts 13MHz signal.

9.1.8.2 Function Specifications

The functional specification of DSP/MCU PLL is shown in the following table.

Symbol	Parameter	Min	Typical	Max	Unit
Fin	Input Clock Frequency		13		MHz
Fout	Output Clock Frequency	52		78	MHz
	Lock-in Time		TBD		Ms
	Output Clock Duty Cycle	40	50	60	%
	Output Clock Jitter		650		ps
DVDD	Digital Power Supply	1.6	1.8	2.0	V
AVDD	Analog Power Supply	2.5	2.8	3.1	V
T	Operating Temperature	-20		80	℃
	Current Consumption		TBD		μA

Table 45 The Functional Specification of DSP/MCU PLL

9.1.9 32-KHz Crystal Oscillator

9.1.9.1 Block Descriptions

The low-power 32-KHz crystal oscillator XOSC32 is designed to work with an external piezoelectric 32.768kHz crystal and a load composed of two functional capacitors, as shown in the following figure.

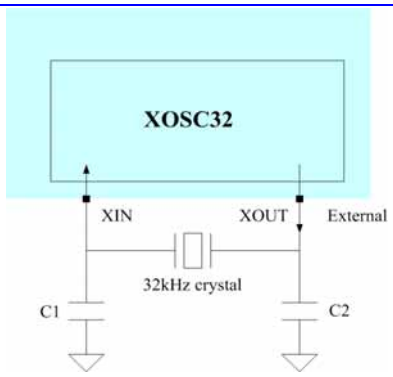


Figure 77 Block diagram of XOSC32

9.1.9.2 Functional specifications

The functional specification of XOSC32 is shown in the following table.

Symbol	Parameter	Min	Typical	Max	Unit
AVDDRTC	Analog power supply	1.2	1.5	2	V
Tosc	Start-up time			5	sec
Dcyc	Duty cycle		50		%
TR	Rise time on XOSCOUT		TBD		ns/pF
TF	Fall time on XOSCOUT		TBD		ns/pF
	Current consumption			5	μA
	Leakage current		1		μA
T	Operating temperature	-20		80	℃

Table 46 Functional Specification of XOSC32

Here below are a few recommendations for the crystal parameters for use with XOSC32.

Symbol	Parameter	Min	Typical	Max	Unit
F	Frequency range		32768		Hz
GL	Drive level			5	uW
Δf/f	Frequency tolerance		+/- 20		Ppm
ESR	Series resistance			50	KΩ

C0	Static capacitance			1.6	pF
CL[5]	Load capacitance	6		12.5	pF

Table 47 Recommended Parameters of the 32kHz crystal

9.2 MCU Register Definitions

9.2.1 BBRX

MCU APB bus registers for BBRX ADC are listed as followings.

MIXED+0300h BBRX ADC Analog-Circuit Control Register BBRX_AC_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DITHEN	QSEL		ISEL		RSV	GAIN		CALBIAS				
Type				R/W	R/W		R/W		R/W	R/W		R/W				
Reset				0	00		00		0	00		00000				

Set this register for analog circuit configuration controls.

CALBIAS The register field is for control of biasing current in BBRX mixed-signal module. It is coded in 2's complement. That is, its maximum is 15 and minimum is –16. Biasing current in BBRX mixed-signal module has impact on the performance of A/D conversion. The larger the value of the register field, the larger the biasing current in BBRX mixed-signal module, and the larger the SNR.

GAIN The register bit is for configuration of gain control of analog inputs in GSM RX mixed-signal module.

00 Input range is 0.8x AVDD for analog inputs in GSM RX mixed-signal module.

01 Input range is 0.4x AVDD for analog inputs in GSM RX mixed-signal module.

10 Input range is 0.57x AVDD for analog inputs in GSM RX mixed-signal module.

11 Input range is 0.33x AVDD for analog inputs in GSM RX mixed-signal module.

ISEL Loopback configuration selection for I-channel in BBRX mixed-signal module

00 Normal mode

01 Loopback TX analog I

10 Loopback TX analog Q

11 Select the grounded input

QSEL Loopback configuration selection for Q-channel in BBRX mixed-signal module

[5] CL is the parallel combination of C1 and C2 in the block diagram.

00 Normal mode

01 Loopback TX analog Q

10 Loopback TX analog I

11 Select the grounded input

DITHDIS Dither feature Disable control register, which can effectively reduce the THD (total harmonic distortion) of the BBRX ADC.

0 turn on the dither (default value)

1 Disable the dither

9.2.2 BBTX

MCU APB bus registers for BBTX DAC are listed as followings.

MIXED+0400h BBTX DAC Analog-Circuit Control Register 0 BBTX_AC_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CALRCDONE	STARTCALRC	GAIN			CALRCSEL			TRIMI				TRIMQ			
Type	R	R/W	R/W			R/W			R/W				R/W			
Reset	0	0	000			000			0000				0000			

Set this register for analog circuit configuration controls. The procedure to perform calibration processing for smoothing filter in BBTX mixed-signal module is as follows:

1. Write 1 to the register bit STARTCALRC. Start calibration process.
2. Read the register bit CALRCDONE. If read as 1, then calibration process finished. Otherwise repeat the step.
3. Write 0 to the register bit STARTCALRC. Stop calibration process.
4. The result of calibration process can be read from the register field CALRCOUT of the register BBTX_AC_CON1. Software can set the value to the register field CALRCSEL for 3-dB cutoff frequency selection of smoothing filter in DAC of BBTX.

Remember to set the register field CALRCCONT of the register BBTX_AC_CON1 to 0xb before the calibration process. It only needs to be set once.

TRIMQ The register field is used to control gain trimming of Q-channel DAC in BBTX mixed-signal module. It is coded in 2's complement, that is, with maximum 7 and minimum –8.

TRIMI The register field is used to control gain trimming of I-channel DAC in BBTX mixed-signal module. It is coded in 2's complement, that is, with maximum 7 and minimum –8.

CALRCSEL The register field is for selection of cutoff frequency of smoothing filter in BBTX mixed-signal module. It is coded in 2's complement. That is, its maximum is 3 and minimum is –4.

GAIN The register field is used to control gain of DAC in BBTX mixed-signal module. It has impact on both of I- and Q-channel DAC in BBTX mixed-signal module. It is coded in 2's complement, that is, with maximum 3 and minimum –4.

STARTCALRC Whenever 1 is writing to the bit, calibration process for smoothing filter in BBTX mixed-signal module will be triggered. Once the calibration process is completed, the register bit CARLDONE will be read as 1.

CALRCDONE The register bit indicates if calibration process for smoothing filter in BBTX mixed-signal module has finished. When calibration processing finishes, the register bit will be 1. When the register bit STARTCALRC is set to 0, the register bit becomes 0 again.

MIXED+0404h BBTX DAC Analog-Circuit Control Register 1 BBTX_AC_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CALRCOUT			FLOAT	CALRCCNT					CALBIAS				CMV		
Type	R/O			R/W	R/W					R./W				R/W		
Reset	-			0	00000					0000				000		

Set this register for analog circuit configuration controls.

CMV The register field is used to control common voltage in BBTX mixed-signal module. It is coded in 2's complement, that is, with maximum 3 and minimum –4.

CALBIAS The register field is for control of biasing current in BBTX mixed-signal module. It is coded in 2's complement. That is, its maximum is 7 and minimum is –8. Biasing current in BBTX mixed-signal module has impact on performance of D/A conversion. Larger the value of the register field, the larger the biasing current in BBTX mixed-signal module.

CALRCCNT Parameter for calibration process of smoothing filter in BBTX mixed-signal module. Default value is '22'. Note that it is **NOT** coded in 2's complement. Therefore the range of its value is from 0 to 31. Remember to set it to 0x16 before BBTX calibration process if clock sent to BBTX is 26Mhz. Otherwise set to 0xb if clock is 13Mhz. It only needs to be set once. In MT6223, only 26MHz clock is available

FLOAT The register field is used to have the outputs of DAC in BBTX mixed-signal module float or not.

CALRCOUT After calibration processing for smoothing filter in BBTX mixed-signal module, a set of 3-bit value is obtained. It is coded in 2's complement.

MIXED+0408h BBTX DAC Analog-Circuit Control Register 2 BBTX_AC_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DCCOARSEQ		DCCOARSEI		DAC_PTR			DWAEN		COARSE		CALRC AUTOL	CALRC OPEN
Type				R/W		R/W		R/W			R/W		R/W		R/W	R/W
Reset				00		00		000			0		0		0	0

Set this register for analog circuit configuration controls.

CALRCOPEN The register field is used to control normal Mode(close loop) or debug mode (open loop) for BBTX comparator in mixed signal

0 normal Mode (close loop)

1 debug Mode (open Loop)

CALRCAUTO The register field is used to control the result of calibration process of smoothing filter can automatically load to control the smoothing filter or not.

0 Not auto load, need manual load (default)

1 Auto load

COARSE The register field is used to control the central nominal value of BBTX DAC output

00 central nominal @ 1V

01 central nominal @ 1V –0.2V

10 reserved

11 central nominal @ 1V +0.2V

DWAEN The register field is used to turn on the DWA scheme of the BBTX DAC,

0 DWA scheme off (default)

1 DWA scheme on

DACPTR The register field is used to configured the staring pointer of 1 hot pulling of LSB[7:0] signal to BBTX DAC, range from 0~7. There is two different configuration. For DWAEN = 0, pointer always starts from the configuration value (e.g. if DACPTR = 3'b1, 1 hot will start pulling from LSB[1]). However, for DWAEN=1, the initial starting pointer will follow the configuration, while the pointer will move to most significant 1 hot pointer + 1 from the last LSB[7:0] input. (e.g. if DACPTR = 3'b1,and LSB[7:0] maybe 8'b00001110, then the next starting poiter will starts from LSB[4].). Defulat value is 0h.

DCCOARSEI The register field is used to control the central nominal value of BBTX DAC for I channel offset

00 central nominal @ +0mV

01 central nominal @ +30mV

11 central nominal @ - 30mV

10 reserved

DCCOARSEQ The register field is used to control the central nominal value of BBTX DAC for Q channel offset

00 central nominal @ +0mV

01 central nominal @ +30mV

11 central nominal @ - 30mV

10 reserved

9.2.3 AFC DAC

MCU APB bus registers for AFC DAC are listed as follows.

MIXED+0500h AFC DAC Analog-Circuit Control Register AFC_AC_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name								GAINSEL			CALI
Type								R/W			R/W
Reset								0			0

Set this register for analog circuit configuration controls. Please refer to analog functional specification for more details.

GAINSEL gain selection of output swing

0 3/4VDD

1 Full VDD

CALI biasing current control

9.2.4 APC DAC

MCU APB bus registers for APC DAC are listed as followings.

MIXED+0600h APC DAC Analog-Circuit Control Register APC_AC_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											BYP	CALI				
Type											R/W	R/W				
Reset											0	0				

Set this register for analog circuit configuration controls. Please refer to analog functional specification for more details.

BYP bypass output buffer

CALI biasing current control

9.2.5 Auxiliary ADC

MCU APB bus registers for AUX ADC are listed as followings.

MIXED+0700h Auxiliary ADC Analog-Circuit Control Register AUX_AC_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											GAINEN	CALI				
Type											R/W	R/W				
Reset											0	0				

Set this register for analog circuit configuration controls. Please refer to analog functional specification for more details.

CALI Biasing current control

GAINEN Comparator switch enable signal.

9.2.6 Voice Front-end

MCU APB bus registers for speech are listed as followings.

MIXED+0100h AFE Voice Analog Gain Control Register AFE_VAG_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				VUPG					VDPG0							
Type				R/W					R/W							
Reset				0000					0000							

Set this register for analog PGA gains. VUPG is set for microphone input volume control. And VDPG0 and VDPG1 are set for two output volume controls

VUPG voice-band up-link PGA gain control bits. For VCFG[3] = 1, it is only valid for INPUT 1.

VCFG [3] =’0’		VCFG [3] =’1’	
VUPG [4:0]	Gain	VUPG [4:0]	Gain
11111	42 dB	XX111	-21dB
11110	40 dB	XX110	-18dB
11101	38 dB	XX101	-15dB
11100	36 dB	XX100	-12dB
11011	34 dB	XX011	-9dB
11010	32 dB	XX010	-6dB
11001	30 dB	XX001	-3dB
11000	28 dB	XX000	0dB
10111	26 dB		
10110	24 dB		
10101	22 dB		
10100	20 dB		
10011	18 dB		
10010	16 dB		
10001	14 dB		
10000	12 dB		
01111	10 dB		

01110	8 dB		
01101	6 dB		
01100	4 dB		
01011	2 dB		
01010	0 dB		
01001	-2 dB		
01000	-4 dB		
00111	-6 dB		
00110	-8 dB		
00101	-10 dB		
00100	-12 dB		
00011	-14 dB		
00010	-16 dB		
00001	-18 dB		
00000	-20 dB		

VDPG0 voice-band down-link PGA0 gain control bits

VDPG0 [3:0]	Gain
1111	8dB
1110	6dB
1101	4dB
1100	2dB
1011	0dB
1010	-2dB
1001	-4dB
1000	-6dB
0111	-8dB
0110	-10dB
0101	-12dB

0100	-14dB
0011	-16dB
0010	-18dB
0001	-20dB
0000	-22dB

MIXED+0104h AFE Voice Analog-Circuit Control Register 0 AFE_VAC_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDC_COUPLE	VMIC_SHORT	VMIC_VREF		VCFG						VDSEND0	VCALI				
Type	R/W	R/W	R/W		R/W						R/W	R/W				
Reset	0	0	00		00000						00	00000				

Set this register for analog circuit configuration controls.

VDC_COUPLE Selectively choose DC couple microphone sense.

- 0 Disable DC couple sense of microphone
- 1 Enable DC couple sense of microphone

VMIC_SHORT Selectively short AU_MICBIASP / AU_MICBIASN.

- 0 float MIC_BIASN and short it to MIC_BIASP when handsfree mode mic is plugged in
- 1 short MIC_BIASN to ground when handsfree mode mic is plugged in. In this mode, differential mic has current leakage and cause power loss.

VMIC_VREF Tuning MICBIASP DC voltage.

- 00 1.9V
- 01 2.0V
- 10 2.1V
- 11 2.2V

VCFG[4] microphone biasing control

- 0 differential biasing
- 1 single-ended biasing

VCFG[3] gain mode control. This control register is only valid to input 1. Others can be amplification mode only.

- 0 amplification
- 1 attenuation

VCFG[2] coupling control

0 AC

1 DC

VCFG[1:0] input select control

00 input 0

01 input 1

10 FM

11 reserved

VDSEND0 single-ended configuration control for out0

VCALI biasing current control, in 2's complement format

MIXED+0108h AFE Voice Analog-Circuit Control Register 1 AFE_VAC_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VUPOP_EN	VBIAS_EN	VOC_EN	VBG_CTRL			VIBOOT	VFLOAT	VRSDON						VADCINMODE	VDACINMODE
Type	R/W	R/W	R/W	R/W			R/W	R/W	R/W						R/W	R/W
Reset	0	0	0	000			1	0	0						0	0

Set this register for analog circuit configuration controls. There are several loop back modes and test modes implemented for test purposes. Suggested value is 0280h.

VUPOP_EN de-pop noise enable

0: disable

1: enable

VBIAS_EN voice downlink buffer bias current control

0: normal bias current

1: increase bias current

VOC_EN voice downlink buffer over current protection

0: disable

1: enable

VBG_CTRL voice-band bandgap control

IBOOT voice downlink DAC bias current control

0: increase bias current

1: normal bias current

VFLOAT voice-band output driver float

0: normal operating mode

1: float mode

VRSDON voice-band redundant signed digit function on

0: 1-bit 2-level mode

1: 2-bit 3-level mode

VADCINMODE Voice-band ADC output mode.

0: normal operating mode

1: the ADC input from the DAC output

VDACINMODE Voice-band DAC input mode.

0: normal operating mode

1: the DAC input from the ADC output

MIXED+010Ch AFE Voice Analog Power Down Control Register AFE_VAPDN_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											VPDN_BIAS	VPDN_LNA	VPDN_ADC	VPDN_DAC		VPDN_OUT0
Type											R/W	R/W	R/W	R/W		R/W
Reset											0	0	0	0		0

Set this register to power up analog blocks. 0: power down, 1: power up.

VPDN_BIAS bias block

VPDN_LNA low noise amplifier block

VPDN_ADC ADC block

VPDN_DAC DAC block

VPDN_OUT0 OUT0 buffer block

MIXED+0110h AFE Voice AGC Control Register AFE_VAGC_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		AAGCEN	AGCTEST	RELNOIDURSEL		RELNOILEVSEL		FRELCKSEL		SRELCKSEL		ATTTHDCAL		ATTCKSEL	HYSTEREN	DAGCEN
Type		R/W	R/W	R/W		R/W		R/W		R/W		R/W		R/W	R/W	R/W
Reset		0	0	00		00		00		00		00		0	0	0

Set this register for analog circuit configuration controls. There are several loop back modes and test modes implemented for test purposes. Suggested value is 4dcfh.

DAGCEN Digital AGC function enable. The loop-back path of AGC comprises analog comparators and digital gain control circuitry. This control register is used to enable the digital gain control circuitry. For normal function, DAGCEN and AAGCEN shall be set to “1” to enable voice AGC function.

HYSTEREN AGC hysteresis function enable

ATTCKSEL attack clock selection

0: 16 KHz

1: 32 KHz

ATTTHDCAL attack threshold calibration

SRELCKSEL release slow clock selection

00: 1000/512 Hz

01: 1000/256 Hz

10: 1000/128 Hz

11: 1000/64 Hz

FRELCKSEL release fast clock selection

00: 1000/64 Hz

01: 1000/32 Hz

10: 1000/16 Hz

11: 1000/8 Hz

RELNOILEVSEL release noise level selection

00: -8 dB

01: -14 dB

10: -20 dB

11: -26 dB

RELNOIDURSEL release noise duration selection

00: 64 ms

01: 32 ms

10: 16 ms

11: 8 ms, 32768/4096

AAGCEN Analog AGC function enable. This control bit is used to enable the comparators of AGC loop-back path.

9.2.7 Audio Front-end

MCU APB bus registers for audio are listed as followings.

MIXED+0200h AFE Audio Analog Gain Control Register AFE_AAG_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							AMUTER	AMUTEL	APGR				APGL			
Type							R/W	R/W	R/W				R/W			
Reset							0	0	0000				0000			

Set this register for analog PGA gains.

AMUTER audio PGA L-channel mute control

AMUTEL audio PGA R-channel mute control

APGR audio PGA R-channel gain control

APGL audio PGA L-channel gain control

APGR [3:0] / APGL [3:0]	Gain
1111	23dB
1110	20dB
1101	17dB
1100	14dB
1011	13dB
1010	8dB
1001	5dB
1000	2dB
0111	-1dB
0110	-4dB
0101	-7dB
0100	-10dB
0011	-13dB
0010	-16dB
0001	-19dB
0000	-22dB

MIXED+0204h AFE Audio Analog-Circuit Control Register AFE_AAC_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			APRO_SC	ADEPOP		ABUFSELR			ABUFSELL			ACALI				
Type			R/W	R/W		R/W			R/W			R/W				
Reset			0	0		000			000			00000				

Set this register for analog circuit configuration controls.

APRO_SC Short circuit protection.

0 disable

1 enable

ADEPOP De-POP noise.

0 disable

1 enable

ABUFSELR audio buffer R-channel input selection

000: audio DAC R/L-channel output; stereo to mono

001: audio DAC R-channel output

010: voice DAC output

100: external FM R/L-channel radio output, stereo to mono

101: external FM R-channel radio output

OTHERS: reserved.

ABUFSELL audio buffer L-channel input selection

000: audio DAC R/L-channel output; stereo to mono

001: audio DAC L-channel output

010: voice DAC output

100: external FM R/L-channel radio output, stereo to mono

101: external FM L-channel radio output

OTHERS: reserved.

ACALI audio bias current control, in 2's complement format

MIXED+0208h AFE Audio Analog Power Down Control Register AFE_AAPDN_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												APDN_BIAS	APDN_DACR	APDN_DACL	APDN_OUTR	APDN_OUTL
Type												R/W	R/W	R/W	R/W	R/W
Reset												0	0	0	0	0

Set this register to power up analog blocks. 0: power down, 1: power up. Suggested value is 00ffh.

APDN_BIAS BIAS block

APDN_DACR R-channel DAC block

APDN_DACL L-channel DAC block

APDN_OUTR R-channel OUT buffer block

APDN_OUTL L-channel OUT buffer block

MIXED+020Ch Enhanced Audio Analog Front End Control & Parameters AFE_AAC_NEW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name								MIC_SHORT	BUF_BIAS	DAC_MODE	MUX	VCMBUF_EN	VCM_MODE	DC_COUPLE
Type								R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								0	0	0		0	0	0

MT6223 ehnahced audio DAC application circuitry selection and control parameters.

MIC_SHORT Selectively short AU_MICBIASP and AU_MICBIASN. Useless.

BUF_BIAS Select buffer quasi-current.

- 00 Nominal bias current
- 01 Larger bias current
- 10 Smallest bias current
- 11 Smaller bias current

DAC_MODE Select two different DAC circuitry.

- 0 New DAC
- 1 Old DAC

MUX Mux audio DAC output to DM R/L pins.

- 00 FM input
- 01 FM input
- 10 Left channel DAC
- 11 Right channel O/P

VCMBUF_EN Enable DC couple VCM buffer.

- 0 Disable VCM buffer
- 1 Enable VCM buffer

VCM_MODE Change common mode generation circuitry.

- 0 New VCM circuitry
- 1 Old VCM circuitry

DC_COUPLE Enable DC couple microphone sense. Useless.

- 0 Disable
- 1 Enable

9.2.8 Register setting path

MIXED+000ch Switch the register configuring path CCI_WR_PATH

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name												AD_INF_PATH	PMIC_WR_PATH	MODEM_WR_PATH	VBI_WR_PATH	ABI_WR_PATH
Type												R/W	R/W	R/W	R/W	R/W
Reset												0	0	0	0	0

WR_PATH

0 Switch the register setting to MCU side

1 Switch the register setting to manually control by TRACE32 through JTAG

The bit is to facilitate ACD members for verifying purpose; the hardware supports write path switching, without being disturbed by existing MCU load. However, when with manually control, all register address are offset by 0x1000. For example, MCU configures AFE_AAC_NEW through the address 0x8050020c, while the manually control path take effect when configuring 0x8050120c. Notice that before finishing manual control, the register must be reset to be 0. The modem part includes BBRX, BBTX, APC, AFC, and AUXADC.

AD_INF_PATH The register bit decides the input/output path of the mixed-mode module. For ABI and VBI, it can be configured to feed the pattern from AFE or from CHIP I/O (shared with A_FUNC_MODE). For BBTX, APC, and AFC, the input selection interface is divided at either MIX_DIG or CHIP I/O (also shared with A_FUNC_MODE). As for the BBRX, the output pattern can be bypass to CHIPIO with this register bit being true. The bit is for convenient debug-use in normal mode, such that the data pattern can be observed or be feed-in by external device, while control register setting still comes from the chip internally(By use of JTAG). It should be notice that this special debug mode should be accompanied by proper setting of GPIO, which decides the PAD OE when in normal function.

0 data pattern comes from chip internally, and the output data cannot be bypassed to chip I/O

1 analog debug mode in normal function

9.2.9 Power Management Control

Power management unit, so called PMU, is integrated into analog part. To facilitate software control and interface design, PMU control share the CCI interface along with other analog parts, such as BBTX, BBRX, and ABI, etc.

9.2.9.1 Block Description

Low Dropout Regulator (LDOs) and Reference

The PMU Integrates eight LDOs that are optimized for their given functions by balancing quiescent current, dropout voltage, line/load regulation, ripple rejection, and output noise.

RF LDO (Vrf)

The RF LDO is a regulator that could source 250mA (max) with 2.8V output voltage. It supplies the baseband circuitry of the SoC. The LDO is optimized for high performance and approximate quiescent current.

Digital Core LDO (Vcore)

The digital core LDO is a regulator that could source 200mA (max) with 1.8V, 1.5V or 1.2V output voltage selection based on software register setting. It supplies the baseband circuitry of the SoC. The LDO is optimized for very low quiescent current.

Digital IO LDO (Vio)

The digital IO LDO is a regulator that could source 100mA (max) with 2.8V output voltage. It supplies the baseband circuitry of the SoC. The LDO is optimized for very low quiescent current and will power up at the same time as the digital core LDO.

Analog LDO (Va)

The analog LDO is a regulator that could source 125mA (max) with 2.8V output voltage. It supplies the analog sections of the SoC. The LDO is optimized for low frequency ripple rejection in order to reject the ripple coming from the RF power amplifier burst frequency at 217Hz.

TCXO LDO (Vtcxo)

The TCXO LDO is a regulator that could source 20mA (max) with 2.8V output voltage. It supplies the temperature compensated crystal oscillator, which needs its own ultra low noise supply and very good ripple rejection ratio.

Two-Step RTC LDO (Vrtc)

The two-step RTC LDO is a set of regulators that could source 600µA (max) with 1.5V output voltage. The first-step LDO charges up a capacitor-type backup coin cell to 2.6V; the second-step LDO utilizes the rich-charged backup coin to supply the real-time clock module even at the absence of the battery. The first-step LDO features the reverse current protection and the second-step LDO is optimized for ultra low quiescent current to sustain the function of the RTC module as long as possible.

Memory LDO (Vm)

The memory LDO is a regulator that could source 75mA (max) with 1.8V or 2.8V output voltage selection based on the supply specs of memory chips. It supplies the memory circuitry in the handset. The LDO is optimized for very low quiescent current and will power up at the same time as the digital core LDO.

SIM LDO (Vsim)

The SIM LDO is a regulator that could source 20mA (max) with 1.8V or 3.0V output voltage selection based on the supply specs of subscriber identity modules (SIM) card. It supplies the SIMs in the handset. The LDO is controlled independently of the others LDO.

Reference Voltage Output (Vref)

The reference voltage output is a low noise, high PSRR and high precision reference with a guaranteed accuracy of 1.5% over temperature. It is used as system reference in PMU internally. However for accurate specs of every LDO output voltage, avoid loading the reference voltage and bypass it to GND with 100 nF minimum.

SIM Card Interface

The SIM card interface circuitry of PMU meets all ETSI and IMT-2000 SIM interface requirements. It provides level shifting needs for low voltage GSM controller to communicate with either 1.8V or 3V SIM cards. All SIM cards contain a clock input, a reset input, and a bi-directional data input/output. The clock and reset inputs to SIM cards are level shifted from the supply of digital IO (Vio) of baseband chipset to the SIM supply (Vsim). The bi-directional data bus is internal pull high with 10kohm resistor.

All pins that connect to the SIM card (Vsim, SRST, SCLK, SIO) withstand over ??(5kV) of human body mode ESD. In order to ensure proper ESD protection, careful board layout is required.

Vibrator, Keypad LED, R/G/B LED Switches

Five built-in open-drain output switches drive the vibrator motor, Keypad LED and R/G/B LEDs in the handset. Each switch is controlled by baseband with enable registers. Each switch of R/G/B LED can sink 25mA. The switch of keypad LED can sink 150mA. The switch of vibrator can sink 250mA. And all the open-drain output switches are high impedance when disabled.

Power Sequence and Protection Logic

The PMU handles the powering ON and OFF of the handset. It is possible to start the power on sequence in two different ways:

- Pulling PWRKEY low
- CHRIN exceeds Chr_Det threshold

Pulling PWRKEY low is the normal way of turning on the handset. This will turn on Vcore, Vio, Vm LDOs as long as the PWRKEY is held low. The Vtcxo and Va LDOs is turned on as baseband is on. The microprocessor then starts and pulls internal node PWRBB high after which PWRKEY can be released. Pulling PWRBB high by baseband will also turn on the handset. This is the case when the alarm in the RTC expires.

Applying an external supply on CHRIN will also turn the handset on. If PMU is in the UVLO state, applying the adapter will not start up the LDOs.

Table 1 shows states of the handset and the LDOs

Table 1. States of Mobile Handset and LDO

Phone State	CHRON	UVLO	PWRKEY && (-PWRBB)	Vrtc	Vd,Vio,Vm	Va, Vtcxo
No Battery or Vbat < 2.5V	X	H	X	Off	Off	Off
2.5V < Vbat < 3.2V	L	H	X	On	Off	Off
Pre-Charging	H	H	X	On	Off	Off
Charger-on	H	L	X	On	On	On
Switched off	L	L	H	On	Off	Off
Stand-by	L	L	L	On	On	Off
Active	L	L	L	On	On	On

Undervoltage Lockout (UVLO)

The UVLO function in the PMU prevents startup when initial voltage of the main battery is below the 3.2V threshold. When the battery voltage is greater than 3.2V, the UVLO comparator trips and the threshold is reduced to 2.9V. This allows the handset to start normally until the battery decays to below 2.9V.

Once the PMU enters UVLO state, it draws very low quiescent current. The RTC LDO is still running until the DDLO disables it.

Deep Discharge Lockout (DDLO)

The DDLO in the PMU has two functions:

- To turn off the Vrtc LDO.
- To shut down the handset when the software fails to turn off the phone when the battery drops below 3.0V. The DDLO will shut down the handset when the battery falls below 2.5 V to prevent further discharge and damage to the cells.

Reset

The PMU contains a reset circuit that is active at both power-up and power-down. The RESET pin is held low at initial power-up, and the reset delay timer is started. The delay is set by an external capacitor on RSTCAP:

$$t_{RESET} = 2\frac{ms}{nF} \times C_{RSTCAP} \quad (1)$$

At power-off, RESET will be kept low.

Over-temperature Protection

If the die temperature of PMU exceeds 150°C, the PMU will disable all the LDOs except the RTC LDO. Once the over-temperature state is resolved, a new power on sequence is required to enable the LDOs.

Battery Charger

The PMU battery charger can be used with Li-ion batteries. PMU charges the battery in three phases: pre-charging, constant current mode charging, and constant voltage mode charging. Figure 2 shows the flow chart of charger behavior. The circuitry of PMU combines with a PMOS transistor, diode, current-sense resistor externally to form a simple and low cost linear charger shown.

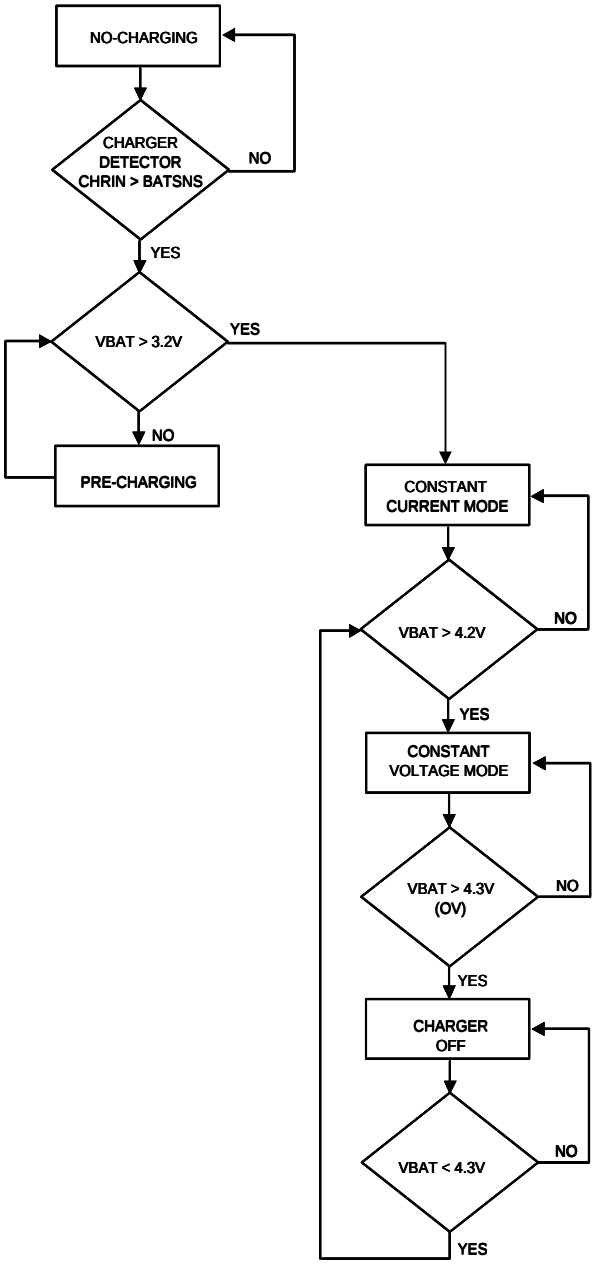


Figure 2. Battery Charger Flow Chart

Charge Detection

The PMU charger block has a detection circuit that determinates if an adapter has been applied to the CHRIN pin and senses the CHRIN voltage. The maximum CHRIN voltage can be up to 8V.

Pre-Charging mode

When the battery voltage is below the UVLO threshold, the charge current is in the pre-charging mode. There are two steps in this mode. While the battery voltage is deeply discharged below 2V, a 10mA trickle current of PMU charges the battery internally. When the battery voltage exceeds 2V, the pre-charge current is enabled, which allows 13mV (typically) across the external current sense resistor (0.2 ohm assumed). This pre-charge current can be calculated:

$$I_{PRE\_CHARGING} = \frac{V_{SENSE}}{R1} = \frac{13mV}{R1} \qquad (2)$$

Constant Current Charging Mode

Once the battery voltage has exceeded the UVLO threshold the charger will switch to the constant current charging mode. The PMU allows a voltage across the external current sense resistor.

If the battery voltage is below 4.2V of Li-ion battery charging, the battery will be in the constant current charging mode.

Constant Voltage Charging Mode

If the battery has reached the final charge voltage, a constant voltage is applied to the battery and keeps it at 4.2V. The charge termination is determined by the baseband, which will set the register CHR_EN to stop the charger.

Once the battery voltage exceeds 4.3V of Li-ion battery, a hardware over voltage protection (OV) should be activated and turn off the charger block of PMU.

External Components Selection

Input Capacitor Selection

For each of input pins (VBAT) of PMU, a local bypass capacitor is recommended. Use a 10μF, low ESR capacitor. MLCC capacitors provide the best combination of low ESR and small size. Using a 10μF Tantalum capacitor with a small (1μF or 2.2μF) ceramic in parallel is an alternative low cost solution.

For charger input pin (CHRIN), a bypass 1μF ceramic capacitor is recommended.

LDO Capacitor Selection

The analog and RF LDOs require a 4.7μF capacitor, the digital core LDO require a 2.2uF capacitor, and the digital IO, SIM, memory and TCXO LDOs require a 1μF capacitor. Large value capacitor may be used for desired noise or PSRR issue. But take consideration of the settling time that is acceptable for system application. The MLCC X5R type capacitors must be used with VRF, VTCXO and VA LDOs for good system performance. For other LDOs, MLCC X5R type capacitors are also recommended to use.

RESET Capacitor Selection

RESET is held low at power-up until a delay time when LDOs are up. The delay is set by an external capacitor on RESCAP pin. It can be determinated by the Eq.(1).

A 100nF capacitor will produce a 200ms delay.

Setting the Charge Current

PMU is capable of charging battery. The charging current is programmed with an external sense resistor, Rsen. It is calculated as the Eq.(3). If the charge current is defined, Rsen can be found.

Appropriate sense resistors are available from the following vendors: Vishay Dale, IRC, Panasonic.

Charger FET Selection

The PMOS FET selection of charger should considerate the minimum drain-source breakdown voltage (BVDS), the minimum turn-on threshold voltage (VGS), and current-handling and power-dissipation qualities.

These specifications can be calculated as below:

$V_{GS} = V_{CHRIN} - V_{GATEDRV}$

$V_{DS} = V_{CHRIN} - V_{DIODE} - V_{SENSE} - VBAT$

$$R_{DS(ON)} = \frac{V_{DS}}{I_{CHR}}$$

$P_{DISS} = (V_{CHRIN}-V_{DIODE}-V_{SENSE}-VBAT) \times I_{CHR}$

Appropriate PMOS FETs are available from the following vendors: Siliconix, IR, Fairchild.

Charger Diode Selection

The diode is used to prevent the battery from discharging through the PMOS's body diode into the charger's internal circuits. Choose a diode with a current rating high enough to handle the battery charging current and a voltage rating greater than Vbat.

Layout Guideline

Use the following general guild-line when designing printed circuit boards:

1. Split battery connection to the VBAT, VBATRF and AVBAT pins of PMU. Locate the input capacitor as close to the pins as possible.
2. Va and Vtcxo capacitors should be returned to AGND. Vrf capacitor should be returned to AGND_RF.
3. Split the ground connection. Use separate traces or planes for the analog, digital, and power grounds (i.e. AGND, AGND_RF, DGND, PGND pins of PMU, respectively) and tie them together at a single point, preferably close to battery return.
4. Run a separate trace from the BATSNS pin to the battery to prevent voltage drop error in the measurement.
5. Kelvin-connect the charge current sense resistor by running separate traces to the BATSNS and ISENSE pins. Make sure that the traces are terminated as close to the resistor's body as possible.
6. Careful use of copper area, weight, and multi-layer construction will contribute to improve thermal performance.

9.2.9.2 Functional Specification

9.2.9.2.1 Electrical Characteristics

VBAT = 3 V ~ 5 V, minimum loads applied on all outputs, unless other noted. Typical values are at T_A = 25 °C.

Parameter	Conditions	Min.	Typical	Max.	Unit
Switch-Off Mode: Supply Current					
VBAT < 2.5 V	RTC LDO OFF		TBD		µA
2.5 V < VBAT < 3.3 V	VBAT=3.3V		TBD		µA
3.3 V < VBAT	VBAT=4.2V		TBD		µA
Operation: Supply Current					
All outputs on	VBAT=4.2V		TBD		µA
VSIM, VTXCO off; all others on	VBAT=4.2V		TBD		µA
Under Voltage (UV)					

Under voltage falling threshold 1	UV_SEL[1:0] = 00	2.85	2.9	2.95	V
Under voltage falling threshold 2	UV_SEL[1:0] = 01	2.7	2.75	2.8	V
Under voltage falling threshold 3	UV_SEL[1:0] = 10	2.55	2.6	2.65	V
Under voltage falling threshold 4	UV_SEL[1:0] = 11	2.35	2.5	2.65	V
Under voltage rising threshold	UV_SEL[1:0] = xx	3.1	3.2	3.3	V
Reset Generator					
Output High		V_{IO}-0.5			V
Output Low				0.2	V
Output Current			1		mA
On Delay Time per Unit Capacitance		1.5	2.5	4	ms/nF
Power Key Input					
High Voltage		0.7*VBAT			V
Low Voltage				0.3*VBAT	V
Control Input Voltage					
Other Control Input High		2.0			V
Other Control Input Low				0.5	
Thermal Shutdown					
Threshold			150		degree
Hysteresis			40		degree
LDO Enable Response Time			250		µs

9.2.9.2.2 Regulator Output

Parameter	Conditions	Min.	Typical	Max.	Unit
Digital Core Voltage					
Output voltage (V_D)	Register VCORE_SEL=00	1.7	1.8	1.9	V
	Register VCORE_SEL=01	1.4	1.5	1.6	V
	Register VCORE_SEL=10	1.1	1.2	1.3	V
Output current (Id_max)			200		mA
Line regulation				5	mV

Load regulation				30	mV
Digital IO Voltage					
Output voltage (V_IO)		2.7	2.8	2.9	V
Output current (Iio_max)			100		mA
Line regulation				5	mV
Load regulation				30	mV
RF Voltage					
Output voltage (V_A)		2.7	2.8	2.9	V
Output current (Ia_max)			250		mA
Line regulation				5	mV
Load regulation				20	mV
Output noise voltage	f = 1k Hz to 100 kHz		40		uVrms
Ripple rejection	at 1kHz		65		dB
Analog Voltage					
Output voltage (V_A)		2.7	2.8	2.9	V
Output current (Ia_max)			125		mA
Line regulation				5	mV
Load regulation				20	mV
Output noise voltage	f = 10 Hz to 100 kHz		50		uVrms
Ripple rejection	10 Hz < freq. < 3 kHz		65		dB
	3 kHz < freq. < 1 MHz		40		dB
VTCXO Voltage					
Output voltage (V_TCXO)		2.7	2.8	2.9	V
Output current (Itcxo_max)			20		mA
Line regulation				4	mV
Load regulation				4	mV
Output noise voltage	f = 10 Hz to 100 kHz		50		µVrms
Ripple rejection	10 Hz < freq. < 3 kHz		65		dB
	3 kHz < freq. < 1 MHz		40		dB
RTC Voltage					

1st stage output voltage		2.6	2.75	2.85	
2nd stage output voltage (V_RTC)	RTC_SEL=H	1.3	1.5	1.65	V
Output current limit (Irtc_max)	1st stage RTC	0.7	1.5		mA
Off reverse input current			1		µA
External Memory Voltage					
Output voltage (V_M)	VMSEL=L	1.7	1.8	1.9	V
	VMSEL=H	2.7	2.8	2.9	V
Output current (Im_max)			75		mA
Line regulation				8	mV
Load regulation				30	mV
SIM Voltage					
Output voltage (V_SIM)	Register VSIM_SEL=L	1.71	1.8	1.89	V
	Register VSIM_SEL=H	2.82	3.0	3.18	V
Output current (Isim_max)			20		mA
Line regulation				4	mV
Load regulation				15	mV
LED/Alerter/Vibrator Driver					
Sink Current of LED Driver	Von<0.5V		75		mA
Sink Current of Key-Pad LED Driver	Von<0.5V		150		mA
Sink Current of Vibrator Driver	Von<0.5V		250		mA

9.2.9.2.3 Switch able Powers

Parameter	Conditions	Min.	Typical	Max.	Unit
VB_OUT	VBSSEL_SPI[1] = 1				
	VBHSEL = 0	VBAT*0.99*0.5		VBAT*1.01*0.5	V
	VBHSEL = 1	VBAT*0.99		VBAT*1.01	V
ISENSE_OUT	VBSSEL_SPI[0] = 1				
	VBHSEL = 0	ISENSE*0.99*0.5		ISENSE*1.01*0.5	V
	VBHSEL = 1	ISENSE*0.99		ISENSE*1.01	V

9.2.9.2.4 SIM interface

Parameter	Conditions	Min.	Typical	Max.	Unit
Interface to 3 V SIM Card					
Volrst	I = 20 µA			0.4	V
Vohrst	I = -200 µA	0.9*VSIM			V
Volclk	I = 20 µA			0.4	V
Vohclk	I = -200 µA	0.9*VSIM			V
Vil				0.4	V
Vihsio , Vohsio	I = ±20 µA	VSIM-0.4			V
Iil	Vil = 0 V			-1	mA
Vol	Iol = 1 mA, SIMIO ≤ 0.23 V			0.4	V
Interface to 1.8 V SIM Card					
Volrst	I = 20 µA			0.2*VSIM	V
Vohrst	I = -200 µA	0.9*VSIM			V
Volclk	I = 20 µA			0.2*VSIM	V
Vohclk	I = -200 µA	0.9*VSIM			V
Vil				0.4	V
Vihsio , Vohsio	I = ±20 µA	VSIM-0.4			V
Iil	Vil = 0 V			-1	mA
Vol	Iol = 1 mA, SIMIO ≤ 0.23 V			0.4	V
SIM Card Interface Timing					
SIO pull-up resistance to VSIM		8	10	12	kΩ
SRST, SIO rise/fall times	VSIM = 3, 1.8 V, load with 30 pF			1	µs
SCLK rise/fall times	VSIM = 3 V, CLK load with 30 pF			18	ns

	VSIM = 1.8 V, CLK load with 30 pF			50	ns
SCLK frequency	CLK load with 30 pF	5			MHz
SCLK duty cycle	SIMCLK Duty = 50%, fsimclk = 5 MHz	47		53	%
SCLK propagation delay			30	50	ns

9.2.9.2.5 Charger Circuit

Parameter	Conditions	Min.	Typical	Max.	Unit
AC charger input voltage		4.2		8	V
AC charger detect on threshold (Vchg_on)	VBAT<3.2V	VBAT		8	V
	VBAT>=3.2V	VBAT +125mV		8	V
Maximum charging current (AC charging)	VBAT>=3.3V		0.16 / R_{sense}		A
Pre-charging current	VBAT<2.3V		10		mA
	VBAT>=2.3V	6/ R_{sense}	13/ R_{sense}	30/ R_{sense}	mA
Pre-charging off threshold			3.3		V
Pre-charging off hysteresis			0.3		V
CC mode to CV mode threshold		4.15	4.2	4.25	V
BAT_ON (Vih)		2.4		2.6	V
GDRVAC/GDRVUSB rising time (T_r)	BAT_ON, or OV	1		5	µs
Over voltage protection threshold (OV)			4.3		V

9.2.9.2.6 LDO and Drivers

Item	LDO	Voltage	Current	Description
1	VD	* 1.8V/1.5V / 1.2V	200 mA	Digital core
2	VIO	2.8V	100 mA	Digital IO
3	VRF	2.8V	250mA	RF chip
4	VA	2.8V	125 mA	Analog and mixed signal

5	VRTC	1.5V	0.6 mA	Real-time clock
6	VM	1.8V / 2.8V	75 mA	External memory, selectable
7	VSIM	1.8V / 3.0V	20 mA	SIM card, selectable
8	VTCXO	2.8V	20 mA	13/26 MHz reference clock

* The VD LDO has options available.

- VD output voltage can be configured as 1.8 V, 1.5V or 1.2 V by register VCORE_SEL<1:0>

Driver	Type	Current	Description
LED_R	Open-drain NMOS switch	25mA	Drives the red LED
LED_G	Open-drain NMOS switch	25mA	Drives the green LED
LED_B	Open-drain NMOS switch	25mA	Drives the blue LED
LED_KP	Open-drain NMOS switch	150 mA	Drives the keypad LEDs
VIBRATOR	Open-drain NMOS switch	250 mA	Drives the vibrator

The output current ratings for the above drivers already include a 50% margin on their nominal current consumption, e.g. if a regulator output is listed as 150 mA, the peak consumption current is 100 mA. In the active state, the phone consumes peak output current at each driver, which must be considered for the thermal design.

9.2.9.2.7 Register Setting

MIXED+0800h Control LDO of V_{RF} and test setting PMIC_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TPSEL						VRF_CAL				ICALRF_EN		VRF_PLNMOS_DIS	VRF_EN_FORCE	VRF_EN	VRF_STATUS
Type	R/W						R/W				R/W		R/W	R/W	R/W	RO
Reset	0						0				0		0	0	0	0

VRF_STATUS RF LDO ON/OFF Status excluding Force-Enable

VRF_EN RF LDO Enable Control Signal

0 Disable

1 Enable

VRF_EN_FORCE RF LDO Force-Enable Control Signal

0 Disable

1 Enable

VRF_PLNMOS_DIS RF LDO Pull-low NMOS disable Signal

0 Enable pull-low

1 Disable pull-low

ICALRF_EN RF LDO Bias Current Calibration Code

0 x1

1 x0.5

2 x2

3 x3

VRF_CAL RF LDO Output Voltage Calibration Code in monotonic transfer function

0000 maximum value

1111 minimum value

TPSEL Internal Node-set Selection for Mux-out in Test Mode

MIXED+0804h Control LDO of V_{CORE} , V_{RTC}, and status of V_{IO} and V_M PMIC_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VM_STATUS	VIO_STATUS	VRTC_EN_FORCE	VRTC_STATUS		VRF_PWRSAVE_EN	VTCXO_PWRSAVE_EN	VCORE_CAL				VCORE_SEL		ICALCORE_EN		VCORE_EN_FORCE
Type	RO	RO	R/W	RO		R/W	R/W	R/W				R/W		R/W		R/W
Reset	0	0	0	0		0	0	0				0		0		0

VCORE_EN_FORCE VCORE LDO Force-Enable Control Signal for MCU write. When being read, this register returns the value of VCORE_STATUS, which is quite different from other LDO's force enable bit

0 Disable

1 Enable

ICALCORE_EN VCORE LDO Bias Current Calibration Code

0 x1

1 x0.5

2 x3

3 x3

VCORE_SEL VCORE LDO Output Voltage Selection Code in monotonic transfer function

00 maximum value

11 minimum value

VCORE_CAL VCORE LDO Output Voltage Calibration Code in monotonic transfer function

0000 maximum value

1111 minimum value

VTCXO_PWRSAVE_EN Power-saving option for VTCXO LDO. If MT6223 is accompanied with MT6139, which only exploit VRF, then the default-on (since SRCLKENA) VTCXO LDO should be turn-off for power saving

0 Power saving disable

1 Power saving enable

VRF_PWRSAVE_EN Power-saving option for VRF LDO. If MT6223 is accompanied with MT6129, which only exploit VTCXO, then the default-on (since SRCLKENA) VRF LDO should be turn-off for power saving

0 Power saving disable

1 Power saving enable

VRTC_STATUS VRTC LDO ON/OFF Status excluding Force-Enable

VRTC_EN_FORCE VRTC LDO Force-Enable Control Signal

0 Disable

1 Enable

VIO_STATUS VIO LDO ON/OFF Status excluding Force-Enable

VM_STATUS VM LDO ON/OFF Status excluding Force-Enable

MIXED+0808h Control LDO of V_{IO} and V_M PMIC_CON2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VM_CAL				ANTIUDSH_M_DN	ICALM_EN		VM_EN_FORCE	VIO_CAL				ANTIUDSH_IO_DN	ICALIO_EN		VIO_EN_FORCE
Type	R/W				R/W	R/W		R/W	R/W				R/W	R/W		R/W
Reset	0				0	0		0	0				0	0		0

VIO_EN_FORCE VIO LDO Force-Enable Control Signal

0 Disable

1 Enable

ICALIO_EN VIO LDO Bias Current Calibration Code

0 x1

1 x0.5

2 x2

3 x3

ANTIUDSH_IO_DN VIO LDO Anti-Undershoot Disable Control Signal

0 Enable function

1 Disable function

VIO_CAL VIO LDO Output Voltage Calibration Code

0000 maximum

1111 minimum

VM_EN_FORCE VM LDO Force-Enable Control Signal

0 Disable

1 Enable

ICALM_EN VM LDO Bias Current Calibration Code

0 x1

1 x0.5

2 x2

3 x3

ANTIUDSH_M_DN VM LDO Anti-Undershoot Disable Control Signal

0 Enable function

1 Disable function

VM_CAL VM LDO Output Voltage Calibration Code in monotonic transfer function

0000 maximum

1111 minimum

MIXED+080Ch Control and Status of LDO of V_{SIM}, Calibration of V_{RTC} PMIC_CON3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VRTC_STEP2_CAL			VRTC_STEP1_CAL			VSIM_CAL				VSIM_PLNMOS_DIS	ANTIUDSH_SIM_DN	ICALSIM_EN		VSIM_EN_FORCE	VSIM_STATUS
Type	R/W			R/W			R/W				R/W	R/W	R/W		R/W	RO
Reset	0			0			0				0	0	0		0	0

VSIM_STATUS VSIM LDO ON/OFF Status excluding Force-Enable

VSIM_EN_FORCE VSIM LDO Force-Enable Control Signal

0 Disable

1 Enable

ICALSIM_EN VSIM LDO Bias Current Calibration Code

0 x1

1 x0.5

2 x2

3 x3

ANTIUDSH_SIM_DN VSIM LDO Anti-Undershoot Disable Control Signal

0 Enable function

1 Disable function

VSIM_PLNMOS_DIS VSIM LDO Pull-low NMOS disable Signal

0 Enable pull low

1 Disable pull low

VSIM_CAL VSIM LDO Output Voltage Calibration Code in monotonic transfer function

0000 maximum value

1111 minimum value

VRTC_STEP1_CAL VRTC LDO1 Output Voltage Calibration Code in 2's complements monotonic transfer function for the 1st step. Configuration of the register must be followed by toggling VRTC_CAL_LATCH_EN (VRTC_STEP1_CAL -> VRTC_CAL_LATCH_EN "TRUE" -> VRTC_CAL_LATCH_EN "FALSE")

000 nominal value

111 minimum value

011 maximum value

VRTC_STEP2_CAL VRTC LDO2 Output Voltage Calibration Code in 2's complement monotonic transfer function for the 2nd step. Configuration of the register must be followed by toggling VRTC_CAL_LATCH_EN(VRTC_STEP2_CAL -> VRTC_CAL_LATCH_EN "TRUE" -> VRTC_CAL_LATCH_EN "FALSE")

000 nominal value

111 minimum value

111 maximum value

MIXED+0810h Control and Status of LDO of V_{CTXO} and V_A PMIC_CON4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VRTC_CAL_LATCH_EN	VA_CAL				VA_EN_SEL	VA_EN_FORCE	VA_STATUS	VTCXO_CAL				VTCXO_PLNMOS_DIS	VTCXO_EN	VTCXO_EN_FORCE	VTCXO_STATUS
Type	R/W	R/W				R/W	R/W	RO	R/W				R/W	R/W	R/W	RO
Reset	0	0				0	0	0	0				0	0	0	0

VCTXP_STATUS VTCXO LDO ON/OFF Status excluding Force-Enable

VCTXO_EN_FORCE VTCXO LDO Force-Enable Control Signal

0 Disable

1 Enable

VCTXO_EN VTCXO LDO Enable Control Signal

0 Disable

1 Enable

VCTXO_PLNMOS_DIS VTCXO LDO Pull-low NMOS disable Signal

0 Enable pull low

1 Disable pull low

VCTXO_CAL VTCXO LDO Output Voltage Calibration Code in monotonic transfer function

0000 maximum value

1111 minimum value

VA_STATUS VA LDO ON/OFF Status excluding Force-Enable

VA_EN_FORCE VA LDO Force-Enable Control Signal

0 Disable

1 Enable

VA_EN_SEL VA LDO Enable Control Selection

VA_CAL VA LDO Output Voltage Calibration Code

0000 maximum value

1111 minimum value

VRTC_CAL_LATCH_EN Latch enable for the VRTC calibration bits. To stabilize the VRTC right after VCORE power-on, analog PMIC unit needs to latch the VRTC_STEP1_CAL and VRTC_STEP2_CAL in advance (before VCORE power off).

0 Disable

1 Enable

MIXED+0814h Driver Control and Charger Status PMIC_CON5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHRG_DIS	CV	AC_DET	BAT_ON	CHR_DET	OVP	VSIM_SEL	VSIM_EN	INT_NODE_MUX			BLED_EN	GLED_EN	RLED_EN	KPLED_EN	VIBR_EN
Type	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0			0	0	0	0	0

VIBR_EN Vibrator Driver Enable Control Signal

0 Disable

1 Enable

KPLED_EN KPLED Driver Enable Control Signal

0 Disable

1 Enable

RLED_EN RLED Driver Enable Control Signal

0 Disable

1 Enable

GLED_EN GLED Driver Enable Control Signal

0 Disable

1 Enable

BLED_EN BLED Driver Enable Control Signal

0 Disable

1 Enable

VSIM_EN Only valid for analog test mode. For normal operation, this LDO enable is actually connected to "simvcc" port of SIM hardware.

0 Disable

1 Enable

VSIM_SEL Only valid for analog test mode. For normal operation, this LDO voltage select is actually connected to "simsel" port of SIM hardware. VSIM LDO voltage selection

0 1.8V

1 1.3V

OVP Charger OV occurred

0 AC<8V

1 AC>8V

CHR_DET Charger detected

0 No charger

1 With charger. The signal is connected to EINT7(active low), acting as an internal interrupt, and can wakeup baseband chip even in sleep mode

BAT_ON Battery is connected

0 Battery is connected

1 Battery is removed

AC_DET AC power detected. Reserved

CV CV mode Indication

0 Not in CV mode

1 In CV mode

CHRG_DIS Not in Charging. Reserved

INT_NODE_MUX MUX the PMU internal nodes, to be monitored by AUXADC

000 ratioed CHRIN voltage

001 ratioed battery voltage

010 ratioed ISENSE voltage

011 internal charger BGR voltage

MIXED+0818h Charger Control PMIC_CON6

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHR_AUX								CHRON_FORCE	CLASS_D			CHOFST			CHR_EN
Type	R/W								R/W	R/W			R/W			R/W
Reset	0								0	0			0			0

CHR_EN Enable Charging (CC and CV mode)

0 Disable

1 Enable

CHOFST Charging Current Offset (for CC mode current calibration)

000 No offset

001 plus 1 step

010 plus 2 step

011 No offset

100 No offset

101 No offset

110 minus 2 step

111 minus 1 step

CLASS_D CC mode charge current level

000 typ : 65mA, min : 30mA, max : 150mA

001 typ : 90mA, min : 45mA, max : 180mA

010 typ : 150mA, min : 105mA, max : 240mA
011 typ : 225mA, min : 180mA, max: 315mA
100 typ : 300mA, min : 240mA, max : 420mA
101 typ : 450mA, min : 380mA, max : 585mA
110 typ : 650mA, min : 585mA, max : 780mA
111 typ : 800mA, min : 720mA, max : 960mA

CHRON_FORCE Charger Force-Enable Control Signal

0 Disable (normal)

1 Enable (force charge on)

CHR_AUX Auxiliary Charger Registers

[7][3]:Thermal shut-down threshold fine tuning

00 : Initial setting

01 : +10˚C

10 : -20˚C

11 : -10˚C

[6:4]:Reference voltage fine tuning according to VBG

000 : initial setting

001 : minus 1 step

010 : minus 2 step

011 : minus 3 step

100 : plus 4 step

101 : plus 3 step

110 : plus 2 step

111 : plus 1 step

[2:0]:Fine tune the CV voltage according to bandgap

000 : VBG=1.2V

001 : VBG=1.205V

010 : VBG=1.210V

011 : VBG=1.215V

100 : VBG=1.18V

101 : VBG=1.185V

110 : VBG=1.190V

111 : VBG=1.195V

MIXED+081Ch Start Up PMIC_CON7

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PWRKEY_DEB		OV_THFREEZE	OV_HYS_ENB	RESET_DRV	VBSSEL		CKSEL	OSCEN	ISEL		RSEL			UV_SEL	
Type	RO		R/W	R/W	R/W	R/W		R/W	R/W	R/W		R/W			R/W	
Reset	0		0	0	0	0		0	0	0		0			0	

UV_SEL UVLO High to Low Threshold Selection

00 2.9CV

01 2.75V

10 2.6V

11 Follow DDLO

RSEL Bandgap T.C. fine tuning

000 initial setting

001 plus 1 step

010 plus 2 step

011 plus 3 step

100 minus 4 step

101 minus 3 step

110 minus 2 step

111 minus 1 step

ISEL Current setting for bandgap and oscillator

00 initial setting

01 plus 1 step

10 minus 2 step

11 minus 1 step

OSCEN Enable the oscillator in bandgap block

0 Disable

1 Enable

CKSEL Setting the clock rate of CKMON

0 ~10kHz

1 ~5kHz

VBSSEL Internal reference current tuning (global bias of PMU)

00 VBG/1200K

01 VBG/1320K

10 VBG/960K

11 VBG/1080K

RESET_DRV Reset Buffer Driving Adjust

OV_HYS_ENB Set the OV threshold when RG_OV_THFREEZE=1

0 Lower

1 Higher

OV_THFREEZE OV threshold freeze at 4.3V

0 OV threshold auto tuning

1 Fixed OV threshold

PWRKEY_DEB Disable PWRKEY Debounce

9.2.10 Reserved

Some registers are reserved for further extensions.

MIXED+0900h Reserved 1 Analog Circuit Control Register 0 RES1_AC_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MIXED+0904h Reserved 1 Analog Circuit Control Register 1 RES1_AC_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MIXED+0A00h Reserved 2 Analog Circuit Control Register 0 RES2_AC_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																

Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MIXED+0A04h Reserved 2 Analog Circuit Control Register 1 RES2_AC_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MIXED+0B00h Reserved 3 Analog Circuit Control Register 0 RES3_AC_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MIXED+0B04h Reserved 3 Analog Circuit Control Register 1 RES3_AC_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MIXED+0C00h Reserved 4 Analog Circuit Control Register 0 RES4_AC_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MIXED+0C04h Reserved 4 Analog Circuit Control Register 1 RES4_AC_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name																
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MIXED+0D00h Reserved 5 Analog Circuit Control Register 0 RES5_AC_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MIXED+0D04h Reserved 5 Analog Circuit Control Register 1 RES5_AC_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MIXED+0E00h Reserved 6 Analog Circuit Control Register 0 RES6_AC_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MIXED+0E04h Reserved 6 Analog Circuit Control Register 1 RES6_AC_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MIXED+0F00h Reserved 7 Analog Circuit Control Register 0 RES7_AC_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MIXED+0F04h Reserved 7 Analog Circuit Control Register 1 RES7_AC_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

9.3 Programming Guide

9.3.1 BBRX Register Setup

The register used to control analog base-band receiver is BBRX_AC_CON.

9.3.1.1 Programmable Biasing Current

To maximize the yield in modern digital process, the receiver features providing 5-bit 32-level programmable current to bias internal analog blocks. The 5-bits registers CALBIAS [4:0] is coded with 2's complement format.

9.3.1.2 Offset / Gain Calibration

The base-band downlink receiver (RX), together with the base-band uplink transmitter (TX) introduced in the next section, provides necessary analog hardware for DSP algorithm to correct the mismatch and offset error. The connection for measurement of both RX/TX mismatch and gain error is shown in **Figure** 78, and the corresponding calibration procedure is described below.

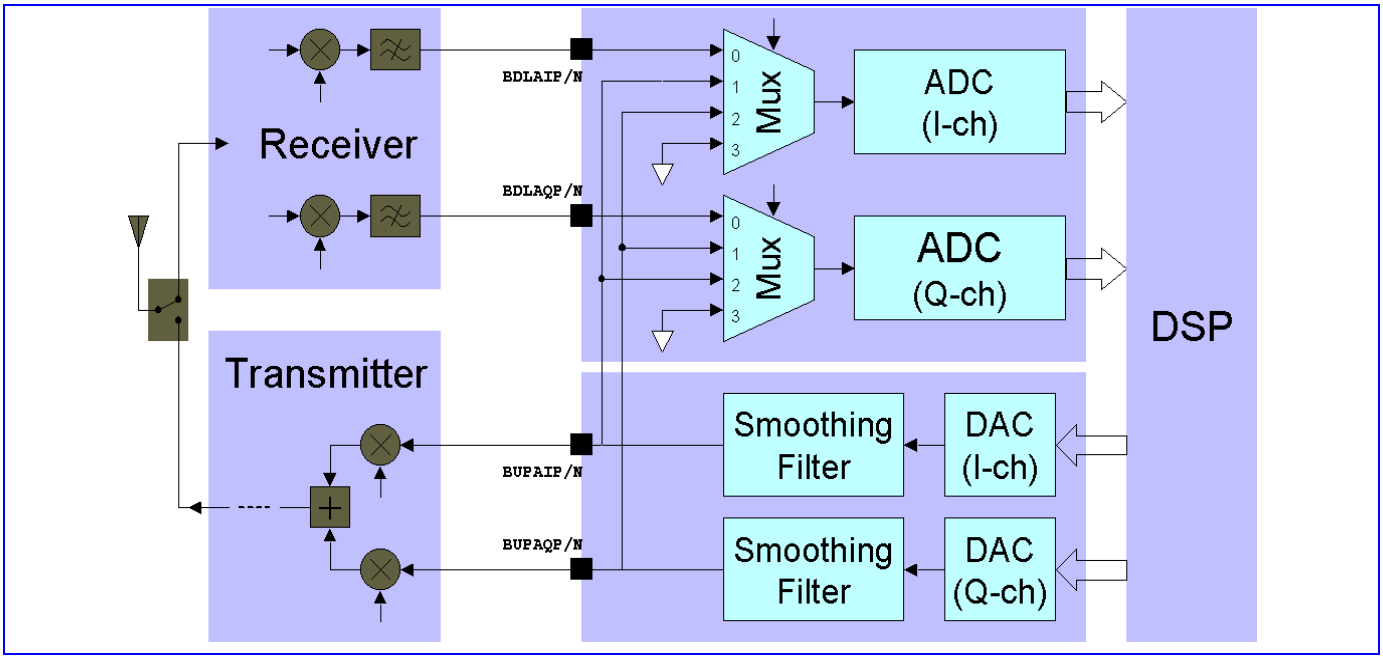


Figure 78 Base-band A/D and D/A Offset and Gain Calibration

9.3.1.3 Downlink RX Offset Error Calibration

The RX offset measurement is achieved by selecting grounded input to A/D converter (set ISEL [1:0] =’11’ and QSEL [1:0] =’11’ to select channel 3 of the analog input multiplexer, as shown in **Figure** 79. The output of the ADC is sent to DSP for further offset cancellation. The offset cancellation accuracy depends on the number of samples being converted. That is, more accurate measurement can be obtained by collecting more samples followed by averaging algorithm.

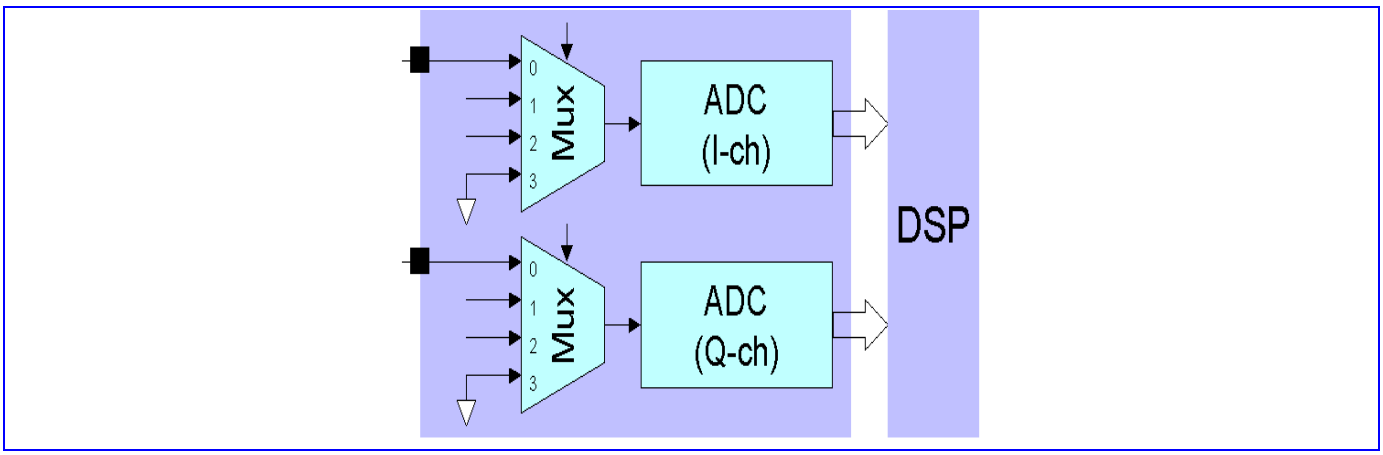


Figure 79 Downlink ADC Offset Error Measurement

9.3.1.4 Downlink RX and Uplink TX Gain Error Calibration

To measure the gain mismatch error, both I/Q uplink TXs should be programmed to produce full-scale pure sinusoidal waves output. Such signals are then fed to downlink RX for A/D conversion, in the following two steps.

A. The uplink I-channel output are connected to the downlink I-channel input, and the uplink Q-channel output are connected to the downlink Q-channel input. This can be achieved by setting ISEL [1:0] =’01’ and QSEL [1:0] =’01’ (shown in **Figure** 80 (A))..

B. The uplink I-channel output are then connected to the downlink Q-channel input, and the uplink Q-channel output are connected to the downlink I-channel input. This can be achieved by setting ISEL [1:0] =’10’ and QSEL [1:0] =’10’ (shown in **Figure** 80 (B)).

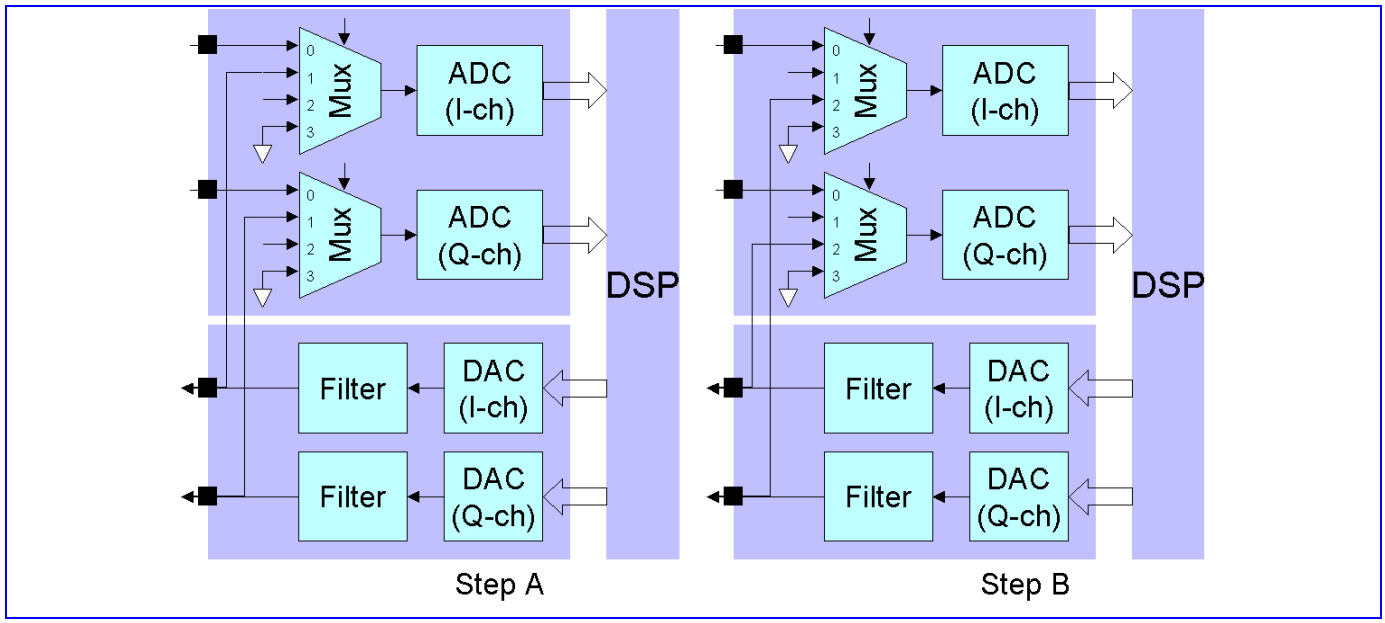


Figure 80 Downlink RX and Up-link TX Gain Mismatch Measurement (A) I/Q TX connect to I/Q RX (B) I/Q TX connect to Q/I RX

Once above successive procedures are completed, RX/TX gain mismatch could be easily obtained because the amplitude mismatch on RX digitized result in step A and B is the sum and difference of RX and TX gain mismatch, respectively.

The gain error of the downlink RX can be corrected in the DSP section and the uplink TX gain error can be corrected by the gain trimming facility that TX block provide.

9.3.1.5 Uplink TX Offset Error Calibration

Once the offset of the downlink RX is known and corrected, the offset of the uplink TX alone could be easily estimated. The offset error of TX should be corrected in the digital domain by means of the programmable feature of the digital GMSK modulator.

Finally, it is important that above three calibration procedures should be exercised in order, that is, correct the RX offset first, then RX/TX gain mismatch, and finally TX offset. This is owing to that analog gain calibration in TX will affect its offset, while the digital offset correction has no effect on gain.

9.3.2 BBTX Register Setup

The register used to control analog base-band transmitter is BBTX_AC_CON0 and BBTX_AC_CON1.

9.3.2.1 Output Gain Control

The output swing of the uplink transmitter is controlled by register GAIN [2:0] coded in 2’s complement with about 2dB step. When TRIMI [3:0] / TRIMQ [3:0] = 0 the swing is listed in **Table** 48, defined to be the difference between positive and negative output signal.

GAIN [2:0]	Output Swing	For AVDD=2.8 (V)
+3 (011)	AVDD*0.900 (+6.02 dB)	2.52

+2 (010)	AVDD*0.720 (+4.08 dB)	2.02
+1 (001)	AVDD*0.576 (+2.14 dB)	1.61
+0 (000)	AVDD*0.450 (+0.00 dB)	1.26
-1 (111)	AVDD*0.360 (-1.94 dB)	1
-2 (110)	AVDD*0.288 (-3.88 dB)	0.81
-3 (101)	AVDD*0.225 (-6.02 dB)	0.63
-4 (100)	AVDD*0.180 (-7.95 dB)	0.5

Table 48 Output Swing Control Table

9.3.2.2 Output Gain Trimming

I/Q channels can also be trimmed separately to compensate gain mismatch in the base-band transmitter or the whole transmission path including RF module. The gain trimming is adjusted in 16 steps spread from –1.18dB to +1.18dB (**Table** 49), compared to the full-scale range set by GAIN [2:0].

TRIMI [3:0] / TRIMQ [3:0]	Gain Step (dB)
+7 (0111)	1.18
+6 (0110)	1.00
+5 (0101)	0.83
+4 (0100)	0.66
+3 (0011)	0.49
+2 (0010)	0.32
+1 (0001)	0.16
+0 (0000)	0.00
-1 (1111)	-0.16
-2 (1110)	-0.31
-3 (1101)	-0.46
-4 (1100)	-0.61
-5 (1011)	-0.75
-6 (1010)	-0.90
-7 (1001)	-1.04
-8 (1000)	-1.18

Table 49 Gain Trimming Control Table

9.3.2.3 Output Common-Mode Voltage

The output common-mode voltage is controlled by CMV [2:0] with about 0.08*AVDD step, as listed in the following table.

CMV [2:0]	Common-Mode Voltage
+3 (011)	AVDD*0.62
+2 (010)	AVDD*0.58
+1 (001)	AVDD*0.54
+0 (000)	AVDD*0.50
-1 (111)	AVDD*0.46
-2 (110)	AVDD*0.42
-3 (101)	AVDD*0.38
-4 (100)	AVDD*0.34

Table 50 Output Common-Mode Voltage Control Table

9.3.2.4 Programmable Biasing Current

The transmitter features providing 5-bit 32-level programmable current to bias internal analog blocks. The 5-bits registers CALBIAS [4:0] is coded with 2's complement format.

9.3.2.5 Smoothing Filter Characteristic

The 2nd –order Butterworth smoothing filter is used to suppress the image at DAC output: it provides more than 40dB attenuation at the 4.44MHz sampling frequency. To tackle with the digital process component variation, programmable cutoff frequency control bits CALRCSEL [2:0] are included. User can directly change the filter cut-off frequency by different CALRCSEL value (coded with 2's complement format and with a default value 0). In addition, an internal calibration process is provided, by setting START CALRC to high and CALRCCNT to an appropriate value (default is 11). After the calibration process, the filter cut-off frequency is calibrated to 350kHz +/- 50 kHz and a new CALRCOUT value is stored in the register. During the calibration process, the output of the cell is high-impedance.

9.3.3 AFC-DAC Register Setup

The register used to control the APC DAC is AFC_AC_CON, which providing 5-bit 32-level programmable current to bias internal analog blocks. The 5-bits registers CALI [4:0] is coded with 2's complement format.

9.3.4 APC-DAC Register Setup

The register used to control the APC DAC is AFC_AC_CON, which providing 5-bit 32-level programmable current to bias internal analog blocks. The 5-bits registers CALI [4:0] is coded with 2's complement format.

9.3.5 Auxiliary A/D Conversion Register Setup

The register used to control the Aux-ADC is AUX_AC_CON. For this register, which providing 5-bit 32-level programmable current to bias internal analog blocks. The 5-bits registers CALI [4:0] is coded with 2's complement format.

9.3.6 Voice-band Blocks Register Setup

The registers used to control AMB are AFE_VAG_CON, AFE_VAC_CON0, AFE_VAC_CON1, and AFE_VAPDN_CON. For these registers, please refer to chapter "Analog Chip Interface"

9.3.6.1 Reference Circuit

The voice-band blocks include internal bias circuits, a differential bandgap voltage reference circuit and a differential microphone bias circuit. Internal bias current could be calibrated by varying VCALI[4:0] (coded with 2's complement format).

The differential bandgap circuit generates a low temperature dependent voltage for internal use. For proper operation, there should be an external 47nF capacitor connected between differential output pins AU_VREFP and AU_VREFN. The bandgap voltage (~1.24V[6], typical) also defines the dBm0 reference level through out the audio mixed-signal blocks**.** The following table illustrates typical 0dBm0 voltage when uplink/downlink programmable gains are unity. For other gain setting, 0dBm0 reference level should be scaled accordingly.

Symbol	Parameter	Min	Typical	Max	Unit
$V_{0dBm0,UP}$	0dBm0 Voltage for Uplink Path, Applied Differentially Between Positive and Negative Microphone Input Pins		0.2V		V-rms
$V_{0dBm0,Dn}$	0dBm0 voltage for Downlink Path, Appeared Differentially Between Positive and Negative Power Amplifier Output Pins		0.6V		V-rms

Table 51 0dBm0 reference level for unity uplink/downlink gain

The microphone bias circuit generates a differential output voltage between AU_MICBIAS_P and AU_MICBIAS_N for external electret type microphone. Typical output voltage is 1.9 V. In singled-ended mode, by set VCFG[3] =1, AU_MICBIAS_N is pull down while output voltage is present on AU_MICBIAS_P, respect to ground. The max current supplied by microphone bias circuit is 2mA.

9.3.6.2 Uplink Path

Uplink path of voice-band blocks includes an uplink programmable gain amplifier and a sigma-delta modulator.

9.3.6.2.1 Uplink Programmable Gain Amplifier

Input to the PGA is a multiplexer controlled by VCFG [3:0], as described in the following table. In normal operation, both input AC and DC coupling are feasible for attenuation the input signal (gain <= 0dB). However, only AC coupling is suggested if amplification of input signal is desired (gain>=0dB).

Control Signal	Function	Descriptions

[6] The bandgap voltage could be calibrated by adjusting control signal VBG_CTRL[1:0]. Its default value is [00]. VBG_CTRL not only adjust the bandgap voltage but also vary its temperature dependence. Optimal value of VBG_CTRL is to be determined.

VCFG [0]	Input Selector	0: Input 0 (From AU_VIN0_P / AU_VIN0_N) Is Selected 1: Input 1 (From AU_VIN1_P / AU_VIN1_N) Is Selected
VCFG [1]	Coupling Mode	0: AC Coupling 1: DC Coupling
VCFG [2]	Gain Mode	0: Amplification Mode (gain >= 0 dB) 1: Attenuation Mode (gain <= 0dB)
VCFG [3]	Microphone Biasing	0: Differential Biasing (Take Bias Voltage Between AU_MICBIAS_P and AU_MICBIAS_N) 1: Signal-Ended Biasing (Take Bias Voltage From AU_MICBIAS_P Respected to Ground. AU_MICBIAS_N Is Connected to Ground)

Table 52 Uplink PGA input configuration setting

The PGA itself provides programmable gain (through VUPG [3:0]) with step of 3dB, as listed in the following table.

VCFG [2] =’0’		VCFG [2] =’1’	
VUPG [3:0]	Gain	VUPG [3:0]	Gain
1111	NA	X111	-21dB
1110	42dB	X110	-18dB
1101	39dB	X101	-15dB
1100	36dB	X100	-12dB
1011	33dB	X011	-9dB
1010	30dB	X010	-6dB
1001	27dB	X001	-3dB
1000	24dB	X000	0dB
0111	21dB		
0110	18dB		
0101	15dB		
0100	12dB		
0011	9dB		
0010	6dB		
0001	3dB		
0000	0dB		

Table 53 Uplink PGA gain setting (VUPG [3:0])

The following table illustrates typically the 0dBm0 voltage applied at the microphone inputs, differentially, for several gain settings.

VCFG [2] =’0’		VCFG [2] =’1’	
VUPG [3:0]	0dBm0 (V-rms)	VUPG [3:0]	0dBm0 (V-rms)
1100	3.17mV	X110	1.59V
1000	12.6mV	X100	0.8V
0100	50.2mV	X010	0.4V
0000	0.2V	X000	0.2V

Table 54 0dBm0 voltage at microphone input pins

9.3.6.2.2 Sigma-Delta Modulator

Analog-to-digital conversion in uplink path is made with a second-order sigma-delta modulator (SDM) whose sampling rate is 4096kHz. Output signals are coded in either one-bit or RSD format, optionally controlled by VRSDON register.

For test purpose, one can set VADCINMODE to HI to form a look-back path from downlink DAC output to SDM input. The default value of VADCINMODE is zero.

9.3.6.3 Downlink Path

Downlink path of voice-band blocks includes a digital to analog converter (DAC) and two programmable output power amplifiers.

9.3.6.3.1 Digital to Analog Converter

The DAC converts input bit-stream to analog signal by sampling rate of 4096kHz. . Besides, it performs a 2^{nd}-order 40kHz butterworth filtering. The DAC receives input signals from MT6223 DSP by set VDACINMODE = 0. It can also take inputs from SDM output by setting VDACINMODE = 1.

9.3.6.3.2 Downlink Programmable Power Amplifier

Voice-band analog blocks include two identical output power amplifiers with programmable gain. Amplifier 0 and amplifier 1 can be configured to either differential or single-ended mode by adjusting VDSEND [0] and VDSEND [1], respectively. In single-ended mode, when VDSEND[0] =1, output signal is present at AU_VOUT0_P pin respect to ground. Same as VDSEND[1] for AU_VOUT1_P pin.

For the amplifier itself, programmable gain setting is described in the following table.

VDPG0 [3:0] / VDPG1 [3:0]	Gain
1111	8dB
1110	6dB
1101	4dB
1100	2dB
1011	0dB

1010	-2dB
1001	-4dB
1000	-6dB
0111	-8dB
0110	-10dB
0101	-12dB
0100	-14dB
0011	-16dB
0010	-18dB
0001	-20dB
0000	-22dB

Table 55 Downlink power amplifier gain setting

Control signal VFLOAT, when set to 'HI', is used to make output nodes totally floating in power down mode. If VFLOAT is set to 'LOW" in power down mode, there will be a resistor of 50k ohm (typical) between AU_VOUT0_P and AU_VOUT0_N, as well as between AU_VOUT0_P and AU_VOUT0_N.

The amplifiers deliver signal power to drive external earphone. The minimum resistive load is 28 ohm and the upper limit of the output current is 50mA. On the basis that 3.14dBm0 digital input signal into downlink path produces DAC output differential voltage of 0.87V-rms (typical), the following table illustrates the power amplifier output signal level (in V-rms) and signal power for an external 32 ohm resistive load.

VDPG	Output Signal Level (V-rms)	Output Signal Power (mW / dBm)
0010	0.11	0.37/-4.3
0110	0.27	2.28/3.6
1010	0.69	14.8/11.7
1110	1.74	94.6/19.8

Table 56 Output signal level/power for 3.14dBm0 input. External resistive load = 32 ohm

The following table illustrates the output signal level and power for different resistive load when VDPG =1110.

RLOAD	Output Signal Level (V-rms)	Output Signal Power (mW / dBm)
30	1.74	101/20
100	1.74	30.3/14.8

600	1.74	5/7

Table 57 Output signal level/power for 3.14dBm0 input, VDPG =1110

9.3.6.4 Power Down Control

Each block inside audio mixed-signal blocks features dedicated power-down control, as illustrated in the following table.

Control Signal	Descriptions
VPDN_BIAS	Power Down Reference Circuits (Active Low)
VPDN_LNA	Power Down Uplink PGA (Active Low)
VPDN_ADC	Power Down Uplink SDM (Active Low)
VPDN_DAC	Power Down DAC (Active Low)
VPDN_OUT0	Power Down Downlink Power Amp 0 (Active Low)
VPDN_OUT1	Power Down Downlink Power Amp 1 (Active Low)

Table 58 Voice-band blocks power down control

9.3.7 Audio-band Blocks Register Setup

The registers used to control audio blocks are AFE_AAG_CON, AFE_AAC_CON, and AFE_AAPDN_CON. For these registers, please refer to chapter “Analog Chip Interface”

9.3.7.1 Output Gain Control

Audio blocks include stereo audio DACs and programmable output power amplifiers. The DACs convert input bit-stream to analog signal by sampling rate of Fs*128 where Fs could be 32kHz, 44.1kHz, or 48kHz. Besides, it performs a 2^{nd}-order butterworth filtering. The two identical output power amplifiers with programmable gain are designed to driving external AC-coupled single-end speaker. The minimum resistor load is 16 ohm and the maximum driving current is 50mA. The programmable gain setting, controlled by APGR[] and APGL[], is the same as that of the voice-band amplifiers.

Unlike voice signals, 0dBFS defines the full-scale audio signals amplitude. Based on bandgap reference voltage again, the following table illustrates the power amplifier output signal level (in V-rms) and signal power for an external 16 ohm resistive load.

APGR[]/ APGL[]	Output Signal Level (V-rms)	Output Signal Power (mW / dBm)
0010	0.055	0.19/-7.2
0110	0.135	1.14/0.6
1010	0.345	7.44/8.7

1110	0.87	47.3/16.7

Table 59 Output signal level/power for 0dBFS input. External resistive load = 16 ohm

9.3.7.2 Mute Function and Power Down Control

By setting AMUTER (AMUTEL) to high, right (Left) channel output will be muted.

Each block inside audio mixed-signal blocks features dedicated power-down control, as illustrated in the following table.

Control Signal	Descriptions
APDN_BIAS	Power Down Reference Circuits (Active Low)
APDN_DACL	Power Down L-Channel DAC (Active Low)
APDN_DACR	Power Down R-Channel DAC (Active Low)
APDN_OUTL	Power Down L-Channel Audio Amplifier (Active Low)
APDN_OUTR	Power Down R-Channel Audio Amplifier (Active Low)

Table 60 Audio-band blocks power down control

9.3.8 Multiplexers for Audio and Voice Amplifiers

The audio/voice amplifiers feature accepting signals from various signal sources including AU_FMINR/AU_FMINL pins, that aimed to receive stereo AM/FM signal from external radio chip:

1) Voice-band amplifier 0 accepts signals from voice DAC output only.
2) Voice-band amplifier 1 accepts signal from either voice DAC, audio DAC, or AM/FM radio input pins (controlled by register VBUF1SEL[]). For the last two cases, left and right channel signals will be summed together to form a mono signal first.
3) Audio left/right channel amplifiers receive signals from either voice DAC, audio DAC, or AM/FM radio input pins (controlled by registers ABUFSELL[] and ABUFSELR[]), too. Left and right channel amplifiers will produce identical output waveforms when receiving mono signals from voice DAC.

9.3.9 Preferred Microphone and Earphone Connections

In this section, preferred microphone and earphone connections are discussed.

Differential connection of microphone is shown below. This is the preferred method to obtain the possible best performance. C1 and Rin form an AC coupling and high-pass network. C1*Rin should be chosen such that the in-band signal will not be attenuated too much. For differential minimum resistance of 13k ohm, minimum value of C1 is 170nF for less than 1dB attenuation at 300Hz. R2 is determined by microphone sensitivity. C2 and R2 form another low-pass filter to filtering noise coming from microphone bias pins. Pole frequency less than 50Hz is recommended.

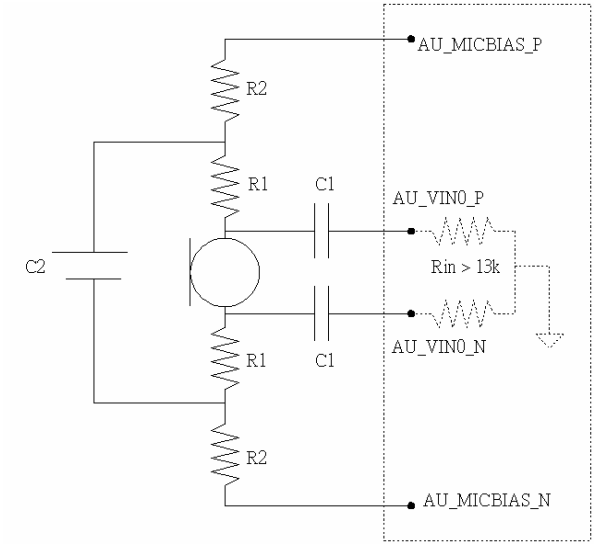


Figure 6 Differential Microphone Connection

For reference, single-ended connection method of microphone is shown below. R1 and R3 are chosen based on microphone sensitivity requirement. C1 and Rin form an AC coupling and high-pass network. R2 and C2 constitute a low-pass network for filtering out noise from microphone bias pins.

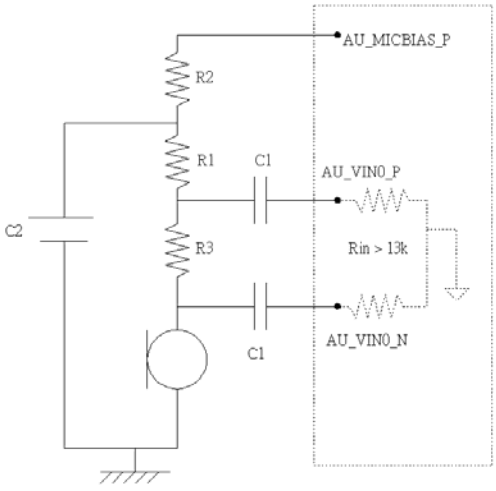


Figure 7 Single-ended Microphone Connection

For earphone, both differential and single-ended connections can be used. Advantage of differential connection includes lower cost and better click-noise immunity. For single-ended connection, an additional AC-coupling capacitor is necessary to not provide DC voltage to earphone. The high-pass cut-off frequency formed by AC-coupling capacitor and earphone equivalent load should be low enough (e.g. < 300 Hz).

9.3.10 Clock Squarer Register Setup

The register used to control clock squarer is CLK_CON. For this register, please refer to chapter “Clocks”

CLKSQ_PLD is used to bypass the clock squarer.

9.3.11 Phase-Locked Loop Register Setup

For registers control the PLL, please refer to chapter “Clocks” and “Software Power Down Control”

9.3.11.1 Frequency Setup

The DSP/MCU PLL itself could be programmable to output either 52MHz or 78MHz clocks. Accompanied with additional digital dividers, 13/26/39/52/65/78 MHz clock outputs are supported.

9.3.11.2 Programmable Biasing Current

The PLLs feature providing 5-bit 32-level programmable current to bias internal analog blocks. The 5-bits registers CALI [4:0] is coded with 2's complement format.

9.3.12 32-khz Crystal Oscillator Register Setup

For registers that control the oscillator, please refer to chapter "Real Time Clock" and "Software Power Down Control".

XOSCCALI[4:0] is the calibration control registers of the bias current, and is coded with 2's complement format.

[1]CL is the parallel combination of C1 and C2 in the block diagram.

10 MT6223 Camera Preview Application Note

10.1 Hardware architecture and software programming

To achieve high frame rate for camera preview, LCD controller provides hardware acceleration for camera preview.

To utilize this feature, bit 16 of **LCD_PCNF0** shall be set to 1 to disable data output from baseband to LCM. After that, by set 1 to bit 14 of **ACIF_CON1**, the sensor is enabled and output onto data bus connected between LCM, sensor, and baseband. Note that related GPIO should be correctly configured. Please refer to Table 61 for the setting of pin selection for pixel clock and hsync.

As for camera capture, the generic DMA provides hardware acceleration with bit 12 of ACIF_CON1 being set, the DMA requests are enabled along with external HSYNC and PIXEL clock.

GPIO programming for hardware acceleration and for IO control

CONFG +0704h LCD/CAM I/O driving strength control ACIF_CON1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIF_PCLK_SEL	CIF_LCD_TRIG	CIF_DMA_DREQ_SEL	CIF_DMA_TRIG	CIF_PCLK_INV	PLCD_SR	PLCD_E2	PLCD_E4	PLCD_E8	CIF_INT30_INV			CLKO345_DRV	CLKO012_DRV	BPI3_E2	BP3I_E4
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0			0	0	0	0

PLCD _E8 The driving strength control of the parallel LCM control interface

PLCD _E4 The driving strength control of the parallel LCM control interface

PLCD _E2 The driving strength control of the parallel LCM control interface

PLCD_SR The slew rate control of the parallel LCM control interface

BPI3_E2 The driving strength control of the BPI3

BPI3_E4 The driving strength control of the BPI3

CLKO012_DRV The driving strength control of CLK_OUT0 ~ CLK_OUT3

0 2mA

1 14mA

CLKO345_DRV The driving strength control of CLK_OUT3 ~ CLK_OUT5

0 2mA

1 14mA

CIF_INT30_INV Select inversion of LCD_CS1_B (GPIO14 mode 2) as INT30 of CIRQ

0 Inversion disabled

1 Inversion enabled

CIF_PCLK_INV Select the polarity of PIXEL_CLOCK input (LCD_CS1_B or ECS3_B, depending on CIF_PCLK_SEL)

0 Non-inversions

1 Select the inverted pixel clock

CIF_DMA_TRIG Enable the hardware DMA DREQ for CIF

0 Disabled

1 Enabled

CIF_DMA_DREQ_SEL Select the source of DMA DREQ for CIF

0 DREQ comes from “ECS3_B(HSYNC) & LCD_CS1_B(PCLK)”

1 DREQ comes from “EINT2(HSYNC) & LCD_CS1_B(PCLK)” or from “EINT2(HSYNC) & ECS_B(PCLK), ”depending on CIF_PCLK_SEL

CIF_LCD_TRIG Enable the hardware LCD DREQ for CIF

0 Disabled

1 Enabled

CIF_PCLK_SEL Select the source of PIXEL clock

0 ECS3_B(GPIO52)

1 LCD_CS1_B(GPIO14)

	PCLK	HSYNC	ACIF_CON[31:28]	ACIF_CON[27]	ACIF_CON[22]	Interrupt source
GPIO set 1	ECS3_B(GPIO52 @ mode 1)	LCD_CS1_B(GPIO14 @ mode3)	01 01	Invert of PCLK	Invert of INT30	INT30
GPIO set 2	ECS3_B(GPIO52 @ mode 1)	EINT2(GPIO14 @ mode2)	0 111	Invert of PCLK	X	MIRQ
GPIO set 3	LCD_CS1_B(GPIO14 @ mode3)	EINT2(GPIO14 @ mode2)	1 111	Invert of PCLK	X	MIRQ
GPIO set 4	EINT2(GPIO14 @ mode2)	LCD_CS1_B(GPIO14 @ mode3)	1 111	X	Invert of INT30	INT30

Table 61

Note of LCD-Sensor direct couple:

1. The image size of camera should be exactly the same with LCD size.
2. The color format of camera output data shall be the same with LCD, must be RGB type rather than YCbCr.
3. If the sensor fails the 2 compatibilities described above, software should use “generic DMA acceleration” for both preview and capture.
1. When enabling hardware-accelerated path from sensor to LCM, using LCD controller’s DMA engine is prohibited. In addition, control register **LCD_WROIDADD** indicates which LCM is destinated

Note of generic DMA acceleration:

1. In view of transfer efficiency, the hardware acceleration occupies master 19 of generic DMA channel 1 through software programming, and slow-down mechanism of this channel should be disabled too.
2. Considering transfer efficiency and scenario concurrency, the baseband should not be accompanied with too low-end external memory, such like non-page memory